Simulator Lab

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Introduction

This lab will enable the user to finish creating the WATCH project using the Foundation Schematic Editor. Once the design is finished, most of the nodes between macrofunctions will have to be appropriately named so simulation is easier. Finally, the designs functionality will be verified with the Foundation simulator. By using the simulator effectively, small and large projects can be designed and verified quickly.

Objectives

In this lab, it will be shown:

- How to finish creating the WATCH top-level schematic
- How to appropriately name nodes for simulation
- How to insert nodes from the schematic into the simulator
- How to group/ungroup busses during verification
- How to control stimuli with a keyboard
- How to functionally simulate the WATCH project

Procedure

Finishing the WATCH Project

1) Open the Foundation Schematic Editor from within the Foundation Project Manager by clicking on the icon.

2) Once the program has started, click on the "**Symbols Toolbox**" icon on the vertical toolbar. This will open the "**SC Symbols**" box. Find and enter the **OSC4**,

IPAD, **IBUF**, **INV** and **BUFG** symbols into the WATCH schematic.

3) After placing the necessary symbols, make the **TENTHS[9:0]**, **ONES[3:0]** , **ONEOUTS[6:0]** , **TENS[3:0]** , and **TENOUTS[6:0]** busses. Click on the "**Draw Buses**" icon on the vertical toolbar. Locate the pointer, and click on the left

mouse button to start drawing. Move the pointer to the bus destination, and click again.

4) Enter the remaining wires by clicking on the "**Draw Wires**" icon on the vertical toolbar. Connect symbols with wires by clicking on a symbols' node once,

dragging the mouse to the destination, and then clicking on the wires' destination once. Whenever a node connects to more than one destination, connect two of the ports with a wire first. To add an additional destination to the node, first click on the port needing to be added, and then click on the wire. Wire up the circuit according to the schematic in the appendix. After adding all the necessary wires, enter "**Select and Drag**" mode by clicking on its icon.

5) Make the necessary pin assignments to the RESET and STRSTP input signals as shown in the schematic.

Naming busses and nodes in the Foundation Schematic Editor

1) To name the busses, double-click on the bus. This action will cause the "**Edit Bus**" dialog box to open (see Figure 1). Enter the name of the bus, and enter the bus width. After this is completed, click on "**OK**". The bus name should now appear in the schematic.

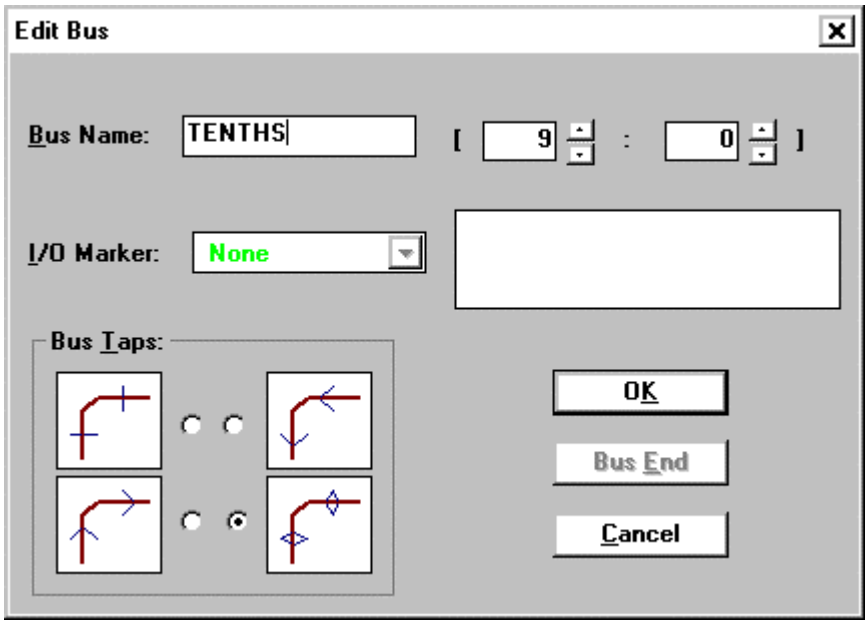


Figure 1. The Edit Bus dialog box.

2) To name the wires, double-click on the wire. This action will cause the "**Net Name**" dialog box to open (see Figure 2). Enter the name of the node and click on "**OK**". The bus name should now appear in the schematic. Name the **CLK**, **RESET**, **STRSTP**, **CLKOUT, TERM** and **RST** nodes in the schematic.

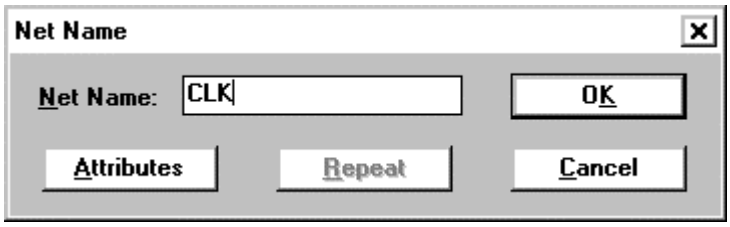
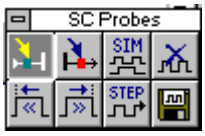


Figure 2. The Net Name dialog box.

Inserting nodes and busses into the Foundation Simulator

1) In the Foundation Schematic Editor, click on the "**Simulation Toolbox**" icon.

This will cause the "**SC Probes**" box to open. Click on the "**Probe**



Tool" button, in the "**SC Probes**" box to select nodes for entry into the

Simulator. Click on the following node names entered into the WATCH schematic: **CLK**, **RESET**, **STRSTP**, **CLKOUT**, **RST**, **TERM**, **TENTHS[9:0]**, **ONES[3:0]**, **TENS[3:0]**, **ONEOUTS[6:0]**, and **TENOUTS[6:0]**. After clicking on each name, a little probe box should appear next to each name.

2) To enter the simulator and have your probes loaded into the simulator click on the "**Simulator"** button in the "**SC Probes**" box. After the simulator has loaded,

the simulator should look similar to Figure 3.

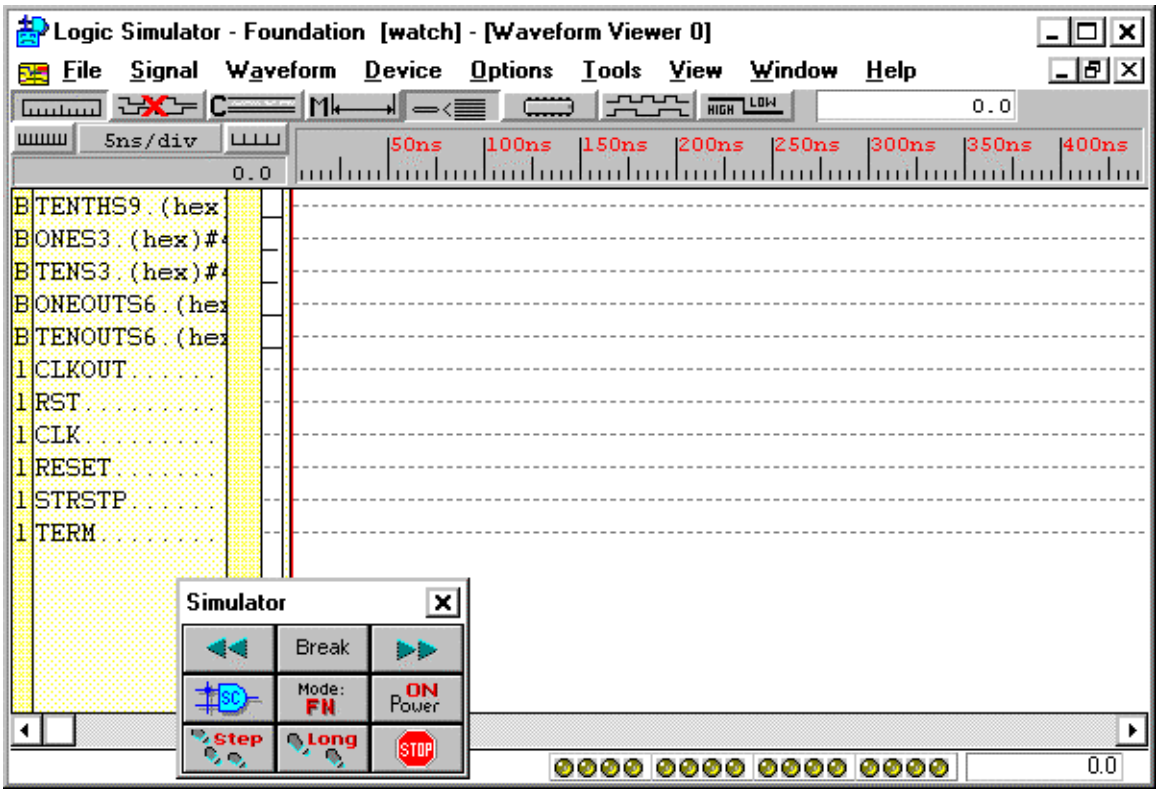


Figure 3. The Foundation Logic Simulator.

3) The simulator has been initialized when the "**Waveform Viewer**" and the "**Simulator**" box have opened. The waveform viewer should now contain all the signals that have a probe attached to them. To move signals and busses in the waveform viewer, select-and-drag the signal to a different row in the viewer. Place all of the designs inputs at the top and the output busses at the bottom of the viewer as in Figure 4.

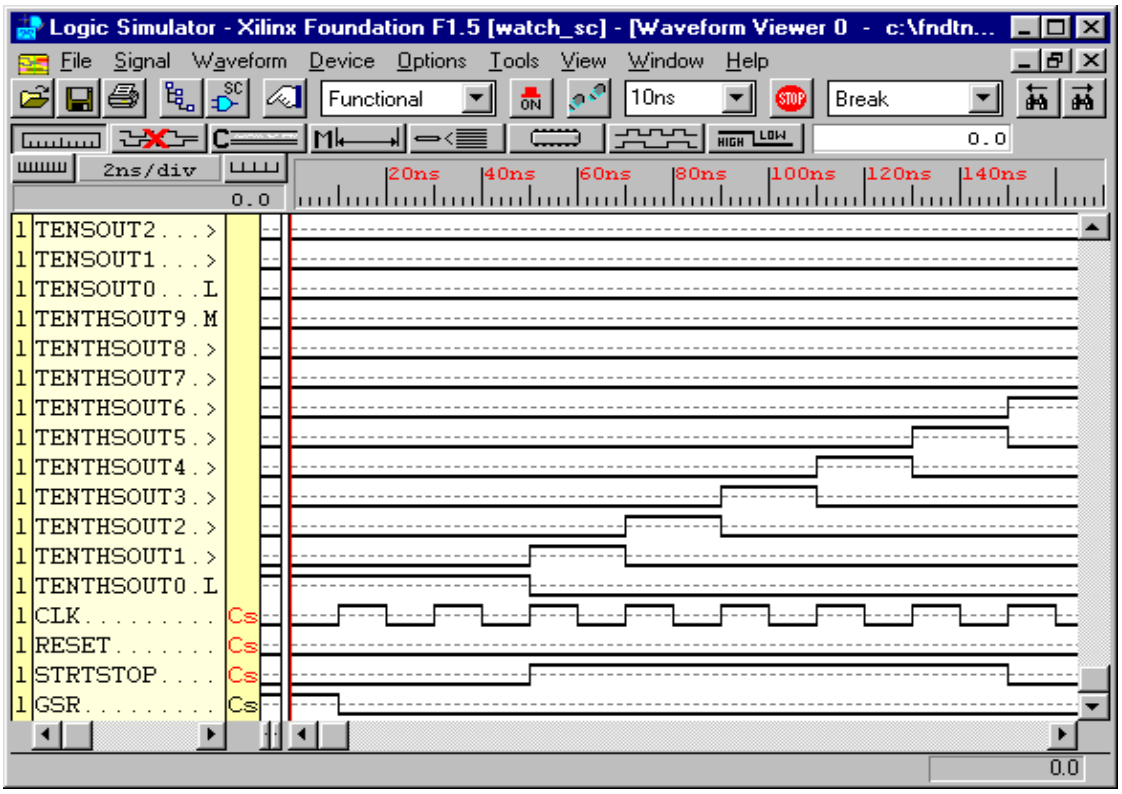


Figure 4. The Waveform Viewer with the signals placed in a new order.

Grouping and ungrouping busses

1) To ungroup the **TENTHS** bus, select the TENTHS9 line in the waveform viewer, the line should turn blue, and click on ***Signal>Bus>Flatten***. The busses 10 bits should now be on separate lines in the waveform viewer. This can also be accomplished by using the Flatten icon.

2) It is also useful to know that when a bus is flattened, the MSB of a bus has a "**&**" placed next to it in the simulator. Likewise, the LSB has a "*****" placed next to it. These features enable a user to arrange the order of the bits contained in any bus. If a bus has already been grouped the menu command ***Signal>Bus>Change Direction*** can be used to quickly rearrange the order of bits in a bus.

3) To regroup the **TENTHS** bus, select the TENTHS0 line, hold down the shift key, move the pointer to the TENTHS9 line and click. This action selects all the elements to be combined into a single bus, and colors them blue. After selecting the elements, click on the menu command **Signal>Bus>Combine** to make the bus.

4) Once a bus has been added to the waveform viewer, it can be displayed in Binary, Octal, Decimal, or Hexadecimal by selecting the bus, clicking on **Signal>Bus>Display…**.

Connecting stimuli to the WATCH inputs

1) To add stimuli to an input, click on the input in the waveform viewer and bring up the "**Stimulator Selection**" box by clicking on its icon, or by clicking on the menu command ***Signal>Add Stimulators***. Select the RESET input by selecting it in the waveform viewer and click on the menu command ***Signal>Add Stimulators***. Once the Stimulator Selection box opens, it should look like Figure 5. Click on the "R" key to set the RESET input to the R key of the keyboard. Likewise, connect the STRSTP input to the "S" key of the keyboard.

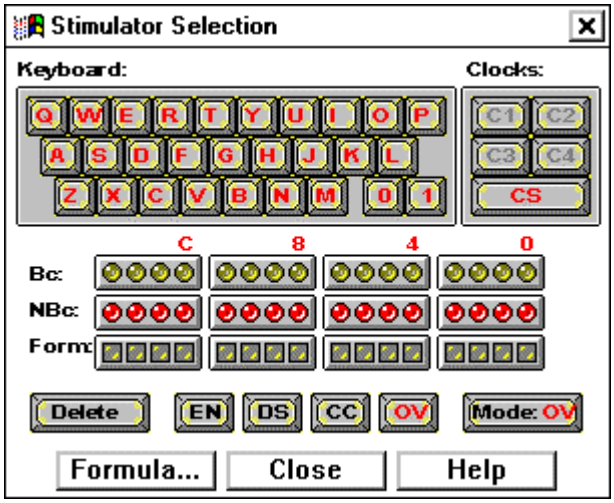


Figure 5. The Stimulator Selection box.

2) To attach a clock signal, select the **CLK** line of the waveform viewer, and then click on the yellow circle below the "**Bc0**" in the Stimulator Selection box. Close the Stimulator Selection box.

3) Once the inputs have been connected, the asynchronous inputs **RESET** and **STRSTP** can be toggled by pressing the appropriate key on the keyboard. The clock signal will be generated and the output signals determined after simulation has begun.

4) After starting the simulation, output waveforms should appear in the waveform viewer.

Functionally simulating the STOPWTCH state machine

1) To simplify the waveform viewer, remove all signals not attached to the STOPWTCH state machine from the viewer (see Figure 6). This is done by selecting the signal and clicking on the menu command ***Signal>Delete Signals>Selected***.

2) Since verification is best done incrementally through the design flow, checking the STOPWTCH macros functionality is easily done by observing the outputs of **RST** and **CLKOUT** while toggling the inputs **RESET** and **STRSTP** through the state machine. By referring to the State Machine Laboratory's diagram, step through the state machine by toggling the inputs and pressing the "**Step**" button to verify the outputs. Remember that the **STRSTP** input was inverted in the top-level schematic, so to begin counting the simulator voltage must be set low. After sufficient simulation, the waveform viewer should look similar to Figure 6.

3) During simulation the Waveform Viewer will continue adding simulation results to the right of the workspace as long as desired by the user. If at any time it is desired to relocate the cursor to the beginning of the workspace, click on the "**Power On**" icon in the Simulator box. This will allow the user to overwrite the results that have already been generated in the Waveform Viewer. Otherwise, inputs can be toggled and new data can continually be generated to the right of the current workspace.

4) From Figure 6, it is easy to see that all the states in the **STOPWTCH** state machine were cycled through. However, not all transitions were checked in Figure 6. Make sure that all transitions are checked during the laboratory.

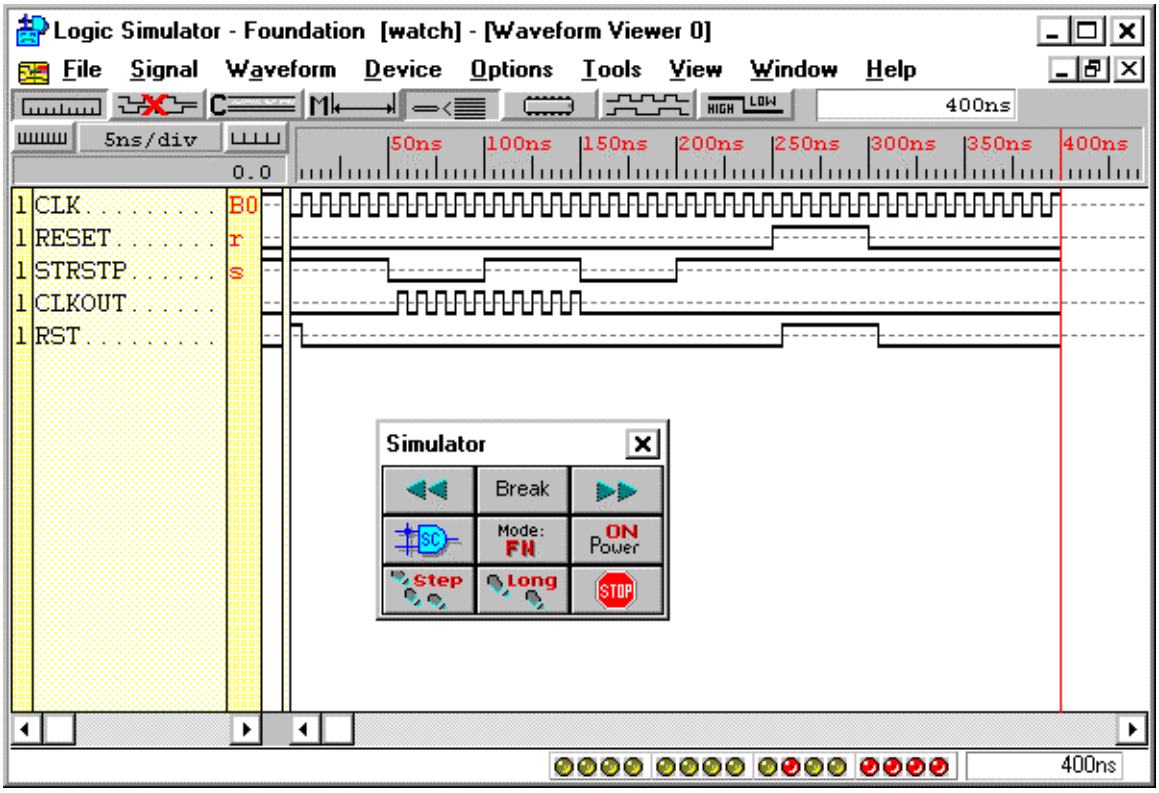
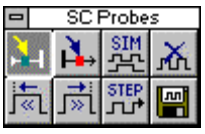


Figure 6. Verifying the STOPWTCH state machine.

Functionally simulating the TENTHS macro

1) To simplify the waveform viewer, **CLK**, **RESET**, and **STRSTP** signals will be deleted from the simulator and the **RST** and **CLKOUT** will be connected to inputs on the keyboard. This will enable verification of just the **TENTHS** macrofunction. Enter the top-level schematic and delete the probes on the **CLK**, **RESET**, and **STRSTP** signals by clicking on their probes. Likewise, place probes on the **TERM** and **TENTHS[9:0]** signals. In the "**SC Probes**" box, click on the "**SIM**" button to reinitialize the simulator.



2) After the appropriate signals have been loaded into the simulator, reset the Waveform Viewer if necessary, and flatten the **TENTHS[9:0]** bus by selecting the bus and using the menu command: ***Signal>Bus>Flatten***.

3) Assign the **CLKOUT** signal to the "**Bc0**" clock signal and connect the **RST** signal to the"**R**" key of the keyboard.

4) Verify the functionality of the **TENTHS** macro by toggling the **RST** signal and observing the behavior of the **TERM** and the **TENTHS** bus. The results obtained should resemble Figure 7. Note that the **TENTHS0** signal is used to denote a counter value of zero. This was caused by choosing the **TENTHS** macro to be one-hot encoded.

Functionally simulating the HEX2LED macrofunction

1) To simplify the waveform viewer, enter the top-level schematic and enter probes on the **ONES[3:0]** and **ONEOUTS[6:0]** busses. Delete the remaining probes from the top-level schematic and click on the "**SIM**" button in the "**SC Probes**" box.

2) Once the simulator has started, reset the Waveform Viewer if necessary. After the buses are loaded, flatten the input bus **ONES[3:0]** and assign each bit to a key on the keyboard. To better view the outputs, display the outputs in a binary format by selecting **ONEOUTS[6:0]** and using the menu command: ***Signal>Bus>Display Binary*** (see Figure 8).

3) Verify the functionality of the HEXTOLED macrofunction by asserting bits of the **ONES[3:0]** bus by toggling their corresponding keys, and clicking on the "**Step**" button in the "**Simulator**" box. Remember to compare the results with the text file created in Laboratory 3.

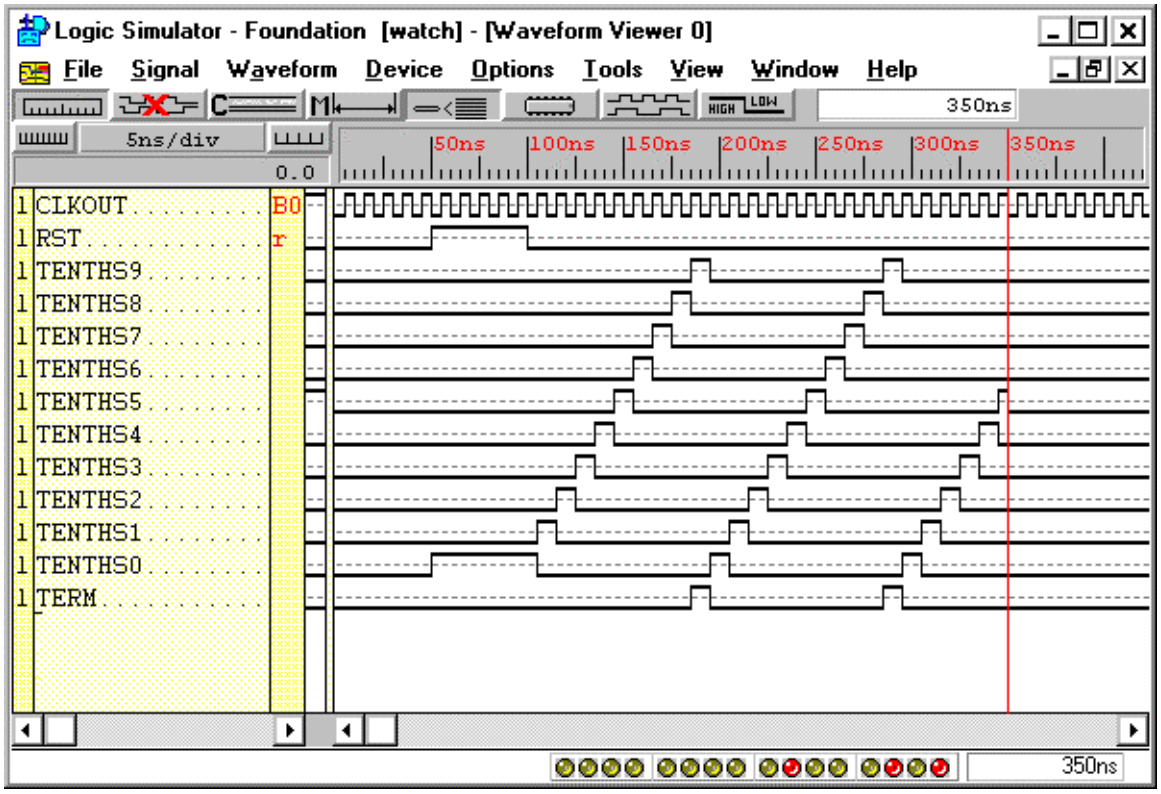


Figure 7. Verifying the TENTHS macrofunction.

Final functional simulation of the WATCH Project.

1) Insert probes on the **CLK, RESET**, **STRSTP**, **TENTHS[9:0]**, **ONES[3:0]**, and **TENS[3:0]** signals. Enter the simulator, flatten the necessary busses, and choose the appropriate display format for the remaining busses (see Figure 9). Since the **HEX2LED** macro is purely combinatorial, it is not necessary to verify its functionality with the rest of the project.

2) After the waveform viewer has been edited correctly, reset the Waveform Viewer if necessary, and use the **RESET** and **STRSTP** controls to verify the functionality performs as expected.

3) Make certain to verify the functionality when the circuit starts operation, resets, and reaches its maximum count value of 59.9 seconds (see Figures 9, 10, and 11).

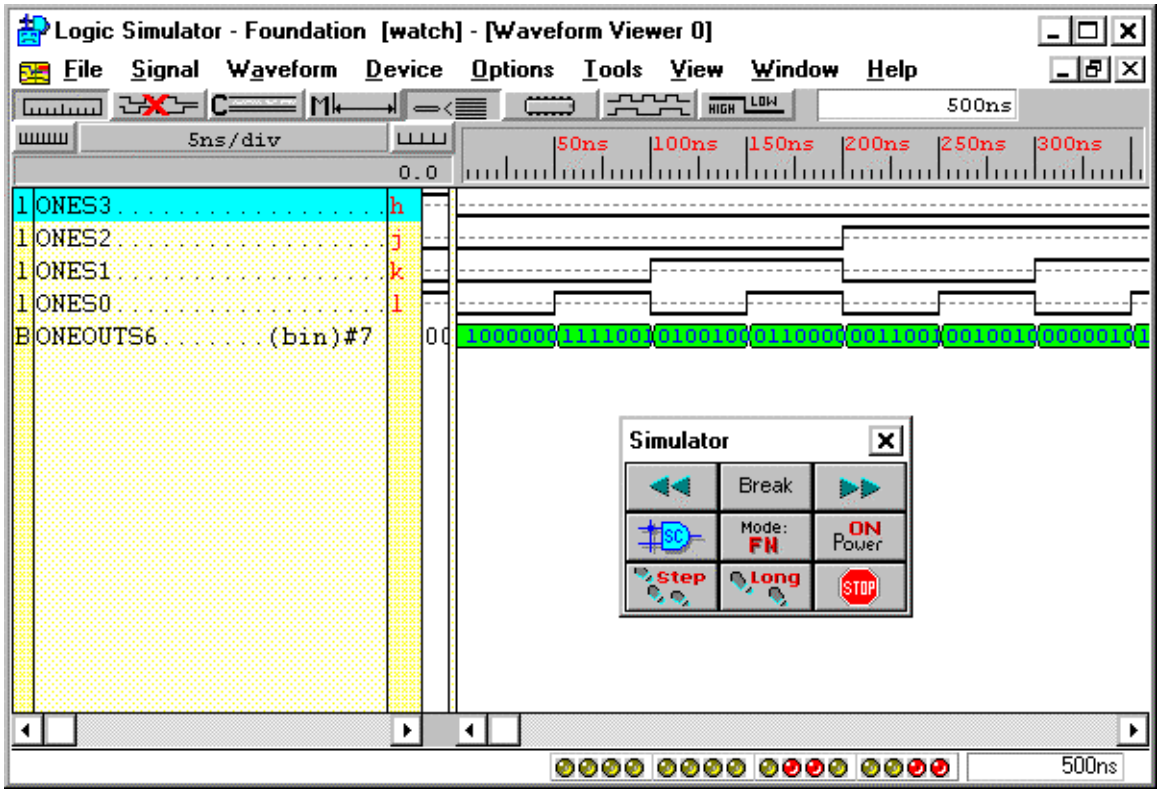


Figure 8. Verifying the HEXTOLED macrofunction.

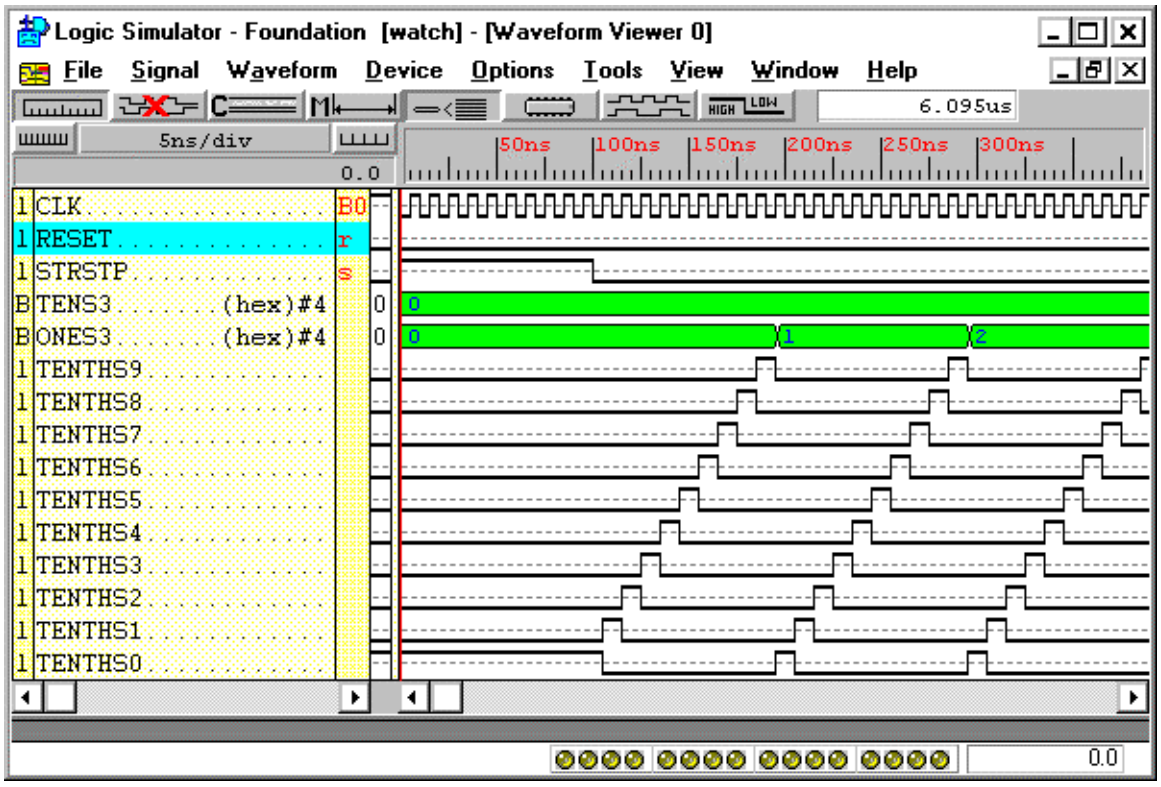


Figure 9. Checking the starting operation of the WATCH Project.

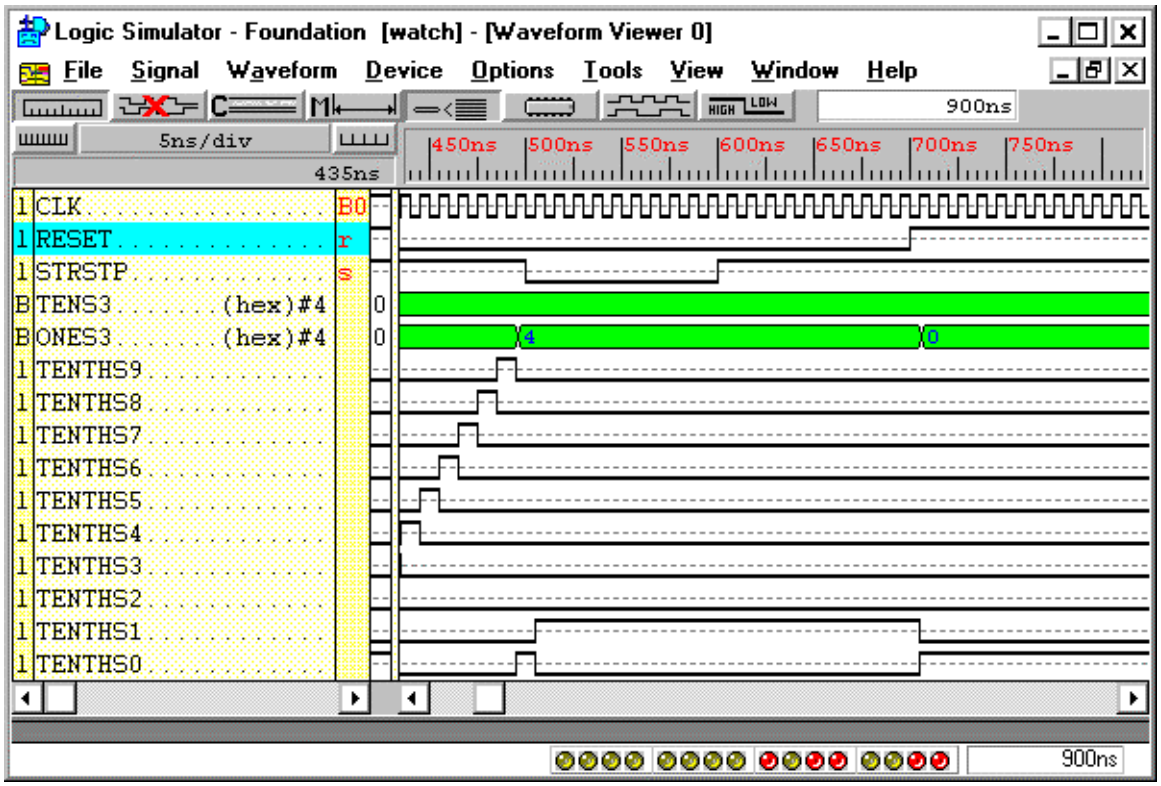


Figure 10. Checking the reset circuitry.

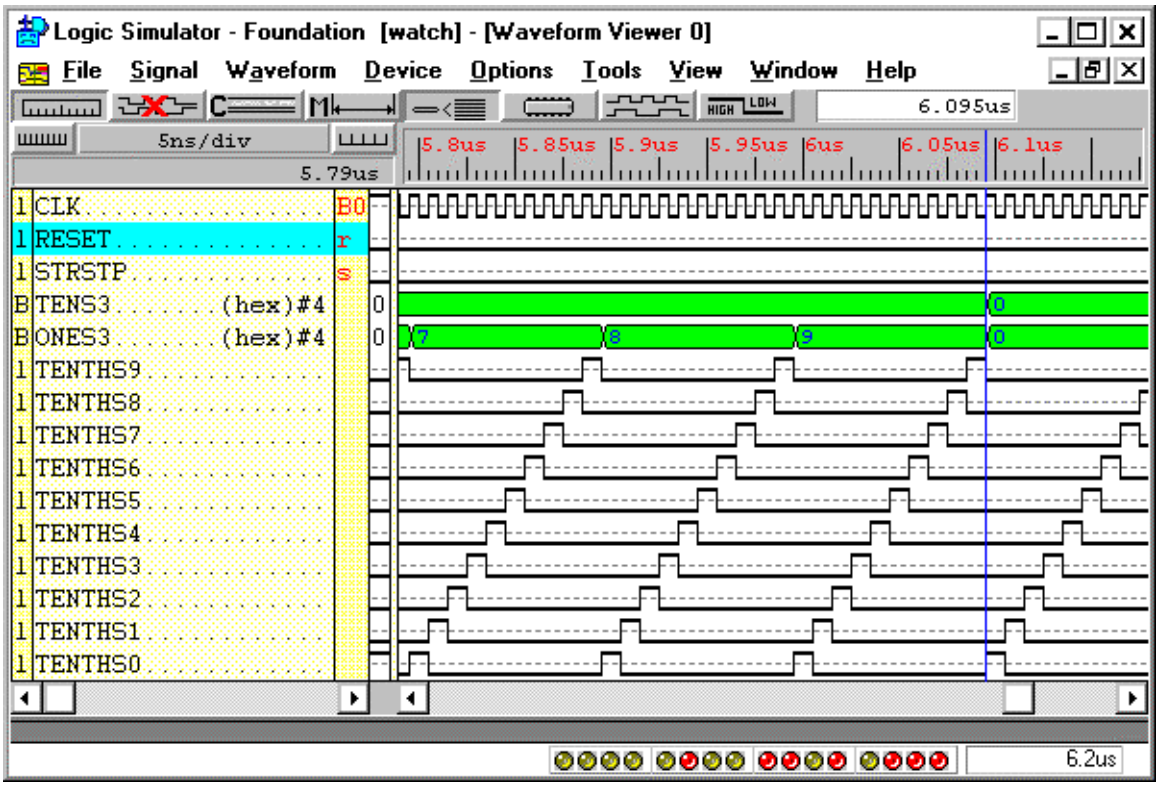


Figure 11. Checking the reset at the maximum count value.

Conclusion

From this laboratory, it was shown:

- Creating and displaying buses is an effective tool for understanding simulation results.
- Naming nodes and buses is essential for viewing in the simulator.
- Inserting probes in a schematic is an easy way to load the Waveform Viewer.
- Connecting stimuli via the Stimulator Selector is simple and effective.

Questions

1) Why should nodes be named in a schematic?

2) Why is it not necessary to name all nodes in a design?