
Macro Library Guide

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Introduction

Definitions

Hard Macros

The Hard Macro library consists of logic elements constructed of one or more ACT family modules. Modules may be of type sequential or combinatorial. Please refer to the ACT Family Field Programmable Gate Array Databook for definitions of ACT family modules. The relative placement of two module-macros is predefined. The timing characteristics are a function of the fanout on the output of the macro.

ACTgen Macro

ACTgen macros are described in Actel's publication, "A Guide to ACTgen Macros."

Combinability

For information on combinability, refer to the *Designer Series Development Tool User's Guide*.

How to Use this Guide

Family Inclusion Indicator

On the side of each data page are tabs indicating whether the cell is a member of the ACT 1, ACT 2/1200XL, 3200DX, ACT 3, 40MX, 42MX, or 54SX library.

Guidelines

These Guidelines are applicable to Hard macros only.

1. All input pin loading is assumed to be a single load except macros that are built using two combinatorial modules or one sequential and

one combinatorial module. These macros are assumed to have a load of two on some of their input pins.

2. All macros have output pin loading of zero except for the sequential macros that are built using two combinatorial modules only. These macros have an output pin loading of one.

3. All hard macros have logic levels equal to one except cells with pin delays of two. A "2" is added to the corresponding symbol in the Hard Macro section of this manual.

Truth Table Nomenclature

Truth tables are arranged with *Inputs* before *Outputs*. The following symbol definitions apply.

↑	denotes rising edge clock
↓	denotes falling edge clock
X	in an input column denotes a 'don't care' or logic simulation state 'unknown'
!Q	denotes Q not

Pin Delay Annotation

Two-module combinatorial macros contain extra delay on some or all of the pins. If a macro symbol in this guide displays a "2" on a pin, then two levels of logic delay exist on the input to output path.

Note: Many two-level logic functions in one family are implemented in a single module in another family, hence the "2" may apply to specific families only.

Restrictions

Special I/Os

Some I/O pins are able to connect to global control signals such as clock or clear. These I/O pins may be used as “normal” data input/output buffers or they may be used as “special” pins. The following constraints apply to I/O pins used as “special” pins.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX register cells may be clocked by either of the two global clock networks by connecting their CLK input to the output of a CLKBUF, CLKBIBUF, or CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX register cells may be globally preset, reset or enabled by connecting the PRE, CLR, or E input to the output of a CLKBUF, CLKBIBUF, CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX I/O three-state buffers may be globally enabled by connecting their E input to the output of a CLKBUF, CLKBIBUF, OR CLKINT macro.

All ACT 3 and 54SX register cells composed of sequential modules may be clocked by high speed clock buffer network by connecting their CLK input to the output of a HCLKBUF macro.

ACT 3 registered I/O macros may *only* be clocked by the IOCLKBUF macro.

ACT 3 registered I/O macros may *only* be asynchronously set or preset by the IOPCL macro.

Advanced Application Notes

For Advanced Application notes, please refer to Actel’s *Databook*.

HDL Instantiation of Macros

Individual macros can be instantiated in your Verilog or VHDL Code.

In Verilog, an instantiation is performed within a module with the following syntax:

```
macro_name instance_name  
(.macro_pin_name(net_name), ...);
```

For example, an instantiation of an AND3 macro could be entered as:

```
AND3 U12 (.A(SIG1), .B(SIG2), .C(SIG3),  
          .Y(SIG4));
```

In VHDL, an instantiation is performed within an architecture with the following syntax:

```
instance_name: macro_name PORT MAP  
(macro_pin_name=>signal_name, ...);
```

For example, an instantiation of an AND3 macro could be entered as:

```
U12: AND3 PORT MAP (A=>SIG1, B=>SIG2,  
                    C=>SIG3, Y=>SIG4);
```

In either language, connection by name rather than by position is shown and is the recommended practice.

Migration Between Families

Actel provides the capability of migrating a netlist created for one family to another family in some cases. Macros listed in this manual as being available in the old family will not be shown as available in the new family when the new macro is inefficient or when the function can be better implemented with different macros, however, the macro may be available in the new family. Such macros are not recommended for new designs.

In all cases, if an HDL description is available, it is best to resynthesize, targeting the new family.

If an HDL description is not available, it is still generally best to do gate level retargeting to the new family.

If neither of the above is done, a netlist created for one family may be used in another family as follows: No special procedures are needed

to use the netlist in Designer, but a migration library must be enabled in CAE environments as explained in individual CAE interface guides.

	Target Family			
Original Family	ACT 1/40MX	ACT 2/1200XL/ 3200DX/42MX	ACT 3	54SX
ACT 1 or 40MX	X	YES	YES	NO
ACT 2, 1200XL, 3200DX, 42MX	NO	X	YES**	YES**
ACT 3	NO	NO	X	YES*
54SX	NO	NO	NO	X

* Except registered I/O, IOCLK, and IOPCL

** Except QCLK and RAM

Hard Combinational Macros

AND2	3	AO3	21
AND2A	3	AO3A	22
AND2B	4	AO3B	22
AND3	4	AO3C	23
AND3A	5	AO4A	23
AND3B	5	AO5A	24
AND3C	6	AO6	24
AND4	6	AO6A	25
AND4A	7	AO7	25
AND4B	7	AO8	26
AND4C	8	AO9	26
AND4D	8	AOI1	27
AND5A	9	AOI1A	27
AND5B	9	AOI1B	28
AND5C	10	AOI1C	28
AO1	11	AOI1D	29
AO10	11	AOI2A	29
AO11	12	AOI2B	30
AO12	12	AOI3A	30
AO13	13	AOI4	31
AO14	13	AOI4A	31
AO15	14	AOI5	32
AO16	14	AX1	32
AO17	15	AX1A	33
AO18	15	AX1B	33
AO1A	16	AX1C	34
AO1B	16	AX1D	34
AO1C	17	AX1E	35
AO1D	17	AXO1	35
AO1E	18	AXO2	36
AO2	18	AXO3	36
AO2A	19	AXO5	37
AO2B	19	AXO6	37
AO2C	20	AXOI1	38
AO2D	20	AXOI2	39
AO2E	21	AXOI3	39

AXOI4	40	GOR2	134
AXOI5	40	GXOR2	135
AXOI7	41	HA1	136
BUFA	42	HA1A	136
BUFF	42	HA1B	137
CLKINT	43	HA1C	137
CM7	44	INVA	138
CM8	45	INV	138
CM8A	46	MAJ3	145
CM8F	47	MAJ3X	145
CM8INV	48	MX2	148
CMB7	49	MX2A	148
CMBB	50	MX2B	149
CMBF	51	MX2C	149
CMEB	52	MX4	150
CMEE	53	MXC1	150
CMEF	54	MXT	151
CMF3	55	NAND2	151
CMF5	56	NAND2A	152
CMF6	57	NAND2B	152
CMF7	58	NAND3	153
CMF9	59	NAND3A	153
CMFA	60	NAND3B	154
CMFB	61	NAND3C	154
CMFC	62	NAND4	155
CMFD	63	NAND4A	155
CMFE	64	NAND4B	156
CS1	65	NAND4C	156
CS2	65	NAND4D	157
CY2A	66	NAND5C	158
CY2B	66	NOR2	158
DXAND7	128	NOR2A	159
DXAX7	128	NOR2B	159
DXNAND7	129	NOR3	160
FA1	129	NOR3A	160
FA1A	130	NOR3B	161
FA1B	130	NOR3C	161
FA2A	131	NOR4	162
GAND2	132	NOR4A	162
GMX4	132	NOR4B	163
GNAND2	133	NOR4C	163
GND	133	NOR4D	164
GNOR2	134	NOR5B	164

NOR5C	165	XO1A	187
OA1	165	XOR2	188
OA1A	166	XOR3	188
OA1B	166	ZOR3	189
OA1C	167	ZOR3I	189
OA2	167		
OA2A	168		
OA3	168		
OA3A	169		
OA3B	169		
OA4	170		
OA4A	170		
OA5	171		
OAI1	171		
OAI2A	172		
OAI3	172		
OAI3A	173		
OR2	173		
OR2A	174		
OR2B	174		
OR3	175		
OR3A	175		
OR3B	176		
OR3C	176		
OR4	177		
OR4A	177		
OR4B	178		
OR4C	178		
OR4D	179		
OR5A	179		
OR5B	180		
OR5C	180		
QCLKINT	181		
VCC	182		
XA1	183		
XA1A	183		
XA1B	184		
XA1C	184		
XAI1	185		
XAI1A	185		
XNOR2	186		
XNOR3	186		
XO1	187		

Hard Sequential Macros

DF1	67	DFM3	86
DF1B	68	DFM3B	87
DF1C	68	DFM3E	87
DFC1	69	DFM3F	88
DFC1A	69	DFM3G	88
DFC1B	70	DFM4	89
DFC1C	70	DFM4A	89
DFC1D	71	DFM4B	90
DFC1E	71	DFM4C	90
DFC1F	72	DFM4D	91
DFC1G	72	DFM4E	91
DFE	73	DFM5A	92
DFE1B	73	DFM5B	92
DFE1C	74	DFM6A	93
DFE2D	74	DFM7A	94
DFE3A	75	DFM7B	95
DFE3B	75	DFM8A	96
DFE3C	76	DFM8B	97
DFE3D	76	DFMA	98
DFE4	77	DFMB	98
DFE4A	77	DFME1A	99
DFE4B	78	DFP1	99
DFE4C	78	DFP1A	100
DFE4F	79	DFP1B	100
DFE4G	79	DFP1C	101
DFEA	80	DFP1D	101
DFEB	80	DFP1E	102
DFEC	81	DFP1F	102
DFED	81	DFP1G	103
DFEG	82	DFPC	103
IODFE	83	DFPCA	104
IODFEC	83	DFPCB	104
IODFEP	84	DFPCC	105
DFM	85	DL1	105
DFM1B	85	DL1A	106
DFM1C	86	DL1B	106

DL1C	107	JKF2B	140
DL2A	107	JKF2C	141
DL2B	108	JKF2D	141
DL2C	108	JKF3A	142
DL2D	109	JKF3B	142
DLC	109	JKF3C	143
DLC1	110	JKF3D	143
DLC1A	110	JKF4B	144
DLC1F	111	JKFPC	144
DLC1G	111	TF1A	181
DLCA	112	TF1B	182
DLE	112		
DLE1D	113		
DLE2A	113		
DLE2B	114		
DLE2C	114		
DLE3A	115		
DLE3B	115		
DLE3C	116		
DLEA	116		
DLEB	117		
DLEC	117		
DLM	118		
DLM2	118		
DLM2A	119		
DLM2B	119		
DLM3	120		
DLM3A	120		
DLM4	121		
DLM4A	121		
DLM8A	122		
DLM8B	123		
DLMA	124		
DLME1A	124		
DLP1	125		
DLP1A	125		
DLP1B	126		
DLP1C	126		
DLP1D	127		
DLP1E	127		
JKF	139		
JKF1B	139		
JKF2A	140		

CC-Module Flip Flops

DF1_CC	193
DF1A_CC	193
DF1B_CC	194
DF1C_CC	194
DFC1_CC	195
DFC1A_CC	195
DFC1B_CC	196
DFC1D_CC	196
DFE_CC	197
DFE1B_CC	197
DFE1C_CC	198
DFEA_CC	198
DFM_CC	199
DFMA_CC	199
DFM1B_CC	200
DFM1C_CC	200
DFP1_CC	201
DFP1A_CC	201
DFP1B_CC	202
DFP1D_CC	202
DFPCA_CC	203
DFPC_CC	203

RAM Macros

RAM4FA	207
RAM4FF	208
RAM4FR	209
RAM4RA	210
RAM4RF	211
RAM4RR	212
RAM8FA	213
RAM8FF	214
RAM8FR	215
RAM8RA	216
RAM8RF	217
RAM8RR	218

I/O Macros

BIBUF	221	DEPETL	241
CLKBIBUF	222	FECTH	241
CLKBUF	222	FECTL	242
HCLKBUF	223	FEPTH	242
INBUF	223	FEPTL	243
OUTBUF	224	FECTMH	243
TRIBUFF	224	FECTML	244
BBDLHS	225	FEPTMH	244
BBHS	226	FEPTML	245
IBDL	226	IBUF	245
IR	227	IOCLKBUF	246
IRI	227	IOPCLBUF	246
OBDLHS	228	IREC	247
OBHS	228	IREP	247
ORH	229	OBUFTH	248
ORIH	229	OBUFTL	248
ORITH	230	ORECTH	249
ORTH	230	ORECTL	249
QCLKBUF	231	OREPTH	250
TBDLHS	231	OREPTL	250
TBHS	232		
BBHSA	233		
BBLSA	234		
BBUFTH	234		
BBUFTL	235		
BIECTH	235		
BIECTL	236		
BIEPH	236		
BIEPTL	237		
BRECTH	237		
BRECTL	238		
BREPTH	238		
BREPTL	239		
DECETH	239		
DECETL	240		
DEPETH	240		

Alphabetical List of Macros

AND2	3	AO3	21
AND2A	3	AO3A	22
AND2B	4	AO3B	22
AND3	4	AO3C	23
AND3A	5	AO4A	23
AND3B	5	AO5A	24
AND3C	6	AO6	24
AND4	6	AO6A	25
AND4A	7	AO7	25
AND4B	7	AO8	26
AND4C	8	AO9	26
AND4D	8	AOI1	27
AND5A	9	AOI1A	27
AND5B	9	AOI1B	28
AND5C	10	AOI1C	28
AO1	11	AOI1D	29
AO10	11	AOI2A	29
AO11	12	AOI2B	30
AO12	12	AOI3A	30
AO13	13	AOI4	31
AO14	13	AOI4A	31
AO15	14	AOI5	32
AO16	14	AX1	32
AO17	15	AX1A	33
AO18	15	AX1B	33
AO1A	16	AX1C	34
AO1B	16	AX1D	34
AO1C	17	AX1E	35
AO1D	17	AXO1	35
AO1E	18	AXO2	36
AO2	18	AXO3	36
AO2A	19	AXO5	37
AO2B	19	AXO6	37
AO2C	20	AXOI1	38
AO2D	20	AXOI2	39
AO2E	21	AXOI3	39

AXOI4	40	CMFE	64
AXOI5	40	CS1	65
AXOI7	41	CS2	65
BBDLHS	225	CY2A	66
BBHS	226	CY2B	66
BBHSA	233	DECETH	239
BBLSA	234	DECETL	240
BBUFTH	234	DEPETH	240
BBUFTL	235	DEPETL	241
BIBUF	221	DF1	67
BIECTH	235	DF1_CC	193
BIECTL	236	DF1A_CC	193
BIEPH	236	DF1B	68
BIEPTL	237	DF1B_CC	194
BRECTH	237	DF1C	68
BRECTL	238	DF1C_CC	194
BREPTH	238	DFC1	69
BREPTL	239	DFC1_CC	195
BUFA	42	DFC1A	69
BUFF	42	DFC1A_CC	195
CLKBIBUF	222	DFC1B	70
CLKBUF	222	DFC1B_CC	196
CLKINT	43	DFC1C	70
CM7	44	DFC1D	71
CM8	45	DFC1D_CC	196
CM8A	46	DFC1E	71
CM8F	47	DFC1F	72
CM8INV	48	DFC1G	72
CMB7	49	DFE	73
CMBB	50	DFE_CC	197
CMBF	51	DFE1B	73
CMEB	52	DFE1B_CC	197
CMEE	53	DFE1C	74
CMEF	54	DFE1C_CC	198
CMF3	55	DFE2D	74
CMF5	56	DFE3A	75
CMF6	57	DFE3B	75
CMF7	58	DFE3C	76
CMF9	59	DFE3D	76
CMFA	60	DFE4	77
CMFB	61	DFE4A	77
CMFC	62	DFE4B	78
CMFD	63	DFE4C	78

DFE4F	79	DFP1D	.101
DFE4G	79	DFP1D_CC	.202
DFEA	80	DFP1E	.102
DFEA_CC	.198	DFP1F	.102
DFEB	80	DFP1G	.103
DFEC	81	DFPC	.103
DFED	81	DFPC_CC	.203
DFEG	82	DFPCA	.104
DFM	85	DFPCA_CC	.203
DFM_CC	.199	DFPCB	.104
DFM1B	85	DFPCC	.105
DFM1B_CC	.200	DL1	.105
DFM1C	86	DL1A	.106
DFM1C_CC	.200	DL1B	.106
DFM3	86	DL1C	.107
DFM3B	87	DL2A	.107
DFM3E	87	DL2B	.108
DFM3F	88	DL2C	.108
DFM3G	88	DL2D	.109
DFM4	89	DLC	.109
DFM4A	89	DLC1	.110
DFM4B	90	DLC1A	.110
DFM4C	90	DLC1F	.111
DFM4D	91	DLC1G	.111
DFM4E	91	DLCA	.112
DFM5A	92	DLE	.112
DFM5B	92	DLE1D	.113
DFM6A	93	DLE2A	.113
DFM7A	94	DLE2B	.114
DFM7B	95	DLE2C	.114
DFM8A	96	DLE3A	.115
DFM8B	97	DLE3B	.115
DFMA	98	DLE3C	.116
DFMA_CC	.199	DLEA	.116
DFMB	98	DLEB	.117
DFME1A	99	DLEC	.117
DFP1	99	DLM	.118
DFP1_CC	.201	DLM2	.118
DFP1A	.100	DLM2A	.119
DFP1A_CC	.201	DLM2B	.119
DFP1B	.100	DLM3	.120
DFP1B_CC	.202	DLM3A	.120
DFP1C	.101	DLM4	.121

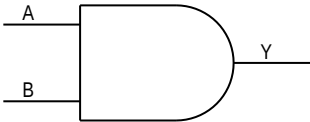
DLM4A	121	IOCLKBUF.	246
DLM8A	122	IODFE	83
DLM8B	123	IODFEC	83
DLMA	124	IODFEP	84
DLME1A	124	IOPCLBUF.	246
DLP1	125	IR	227
DLP1A	125	IREC	247
DLP1B	126	IREP	247
DLP1C	126	IRI.	227
DLP1D	127	JKF	139
DLP1E	127	JKF1B	139
DXAND7	128	JKF2A	140
DXAX7	128	JKF2B	140
DXNAND7	129	JKF2C	141
FA1	129	JKF2D	141
FA1A	130	JKF3A	142
FA1B	130	JKF3B	142
FA2A	131	JKF3C	143
FECTH	241	JKF3D	143
FECTL	242	JKF4B	144
FECTMH	243	JKFPC	144
FECTML	244	MAJ3	145
FEPTH.	242	MAJ3X	145
FEPTL	243	MX2	148
FEPTMH	244	MX2A	148
FEPTML.	245	MX2B	149
GAND2	132	MX2C	149
GMX4	132	MX4	150
GNAND2	133	MXC1	150
GND	133	MXT	151
GNOR2	134	NAND2	151
GOR2	134	NAND2A	152
GXOR2	135	NAND2B	152
HA1	136	NAND3	153
HA1A	136	NAND3A	153
HA1B	137	NAND3B	154
HA1C	137	NAND3C	154
HCLKBUF	223	NAND4	155
IBDL	226	NAND4A	155
IBUF	245	NAND4B	156
INBUF.	223	NAND4C	156
INV	138	NAND4D	157
INVA	138	NAND5C	158

NOR2	158	OR4B	178
NOR2A	159	OR4C	178
NOR2B	159	OR4D	179
NOR3	160	OR5A	179
NOR3A	160	OR5B	180
NOR3B	161	OR5C	180
NOR3C	161	ORECTH	249
NOR4	162	ORECTL	249
NOR4A	162	OREPTH	250
NOR4B	163	OREPTL	250
NOR4C	163	ORH	229
NOR4D	164	ORIH	229
NOR5B	164	ORITH	230
NOR5C	165	ORTH	230
OA1	165	OUTBUF	224
OA1A	166	QCLKBUF	231
OA1B	166	QCLKINT	181
OA1C	167	RAM4FA	207
OA2	167	RAM4FF	208
OA2A	168	RAM4FR	209
OA3	168	RAM4RA	210
OA3A	169	RAM4RF	211
OA3B	169	RAM4RR	212
OA4	170	RAM8FA	213
OA4A	170	RAM8FF	214
OA5	171	RAM8FR	215
OAI1	171	RAM8RA	216
OAI2A	172	RAM8RF	217
OAI3	172	RAM8RR	218
OAI3A	173	TBDLHS	231
OBDLHS	228	TBHS	232
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OBUFTH	248	TF1B	182
OBUFTL	248	TRIBUFF	224
OR2	173	VCC	182
OR2A	174	XA1	183
OR2B	174	XA1A	183
OR3	175	XA1B	184
OR3A	175	XA1C	184
OR3B	176	XA1I	185
OR3C	176	XA1IA	185
OR4	177	XNOR2	186
OR4A	177	XNOR3	186

XO1	187
XO1A	187
XOR2	188
XOR3	188
ZOR3	189
ZOR3I	189

Hard Macros

AND2



Function

2 Input AND

Truth Table

A	B	Y
X	0	0
0	X	0
1	1	1

Inputs

A, B

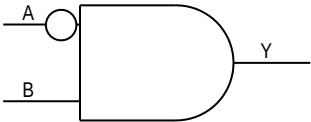
Outputs

Y

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

AND2A



Function

2 Input AND with active low A-Input

Truth Table

A	B	Y
X	0	0
0	1	1
1	X	0

Inputs

A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 1

ACT 2/1200XL

ACT 3

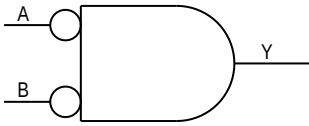
3200DX

40MX

42MX

54SX

AND2B



Function

2 Input AND with active low Inputs

Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

Inputs

A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

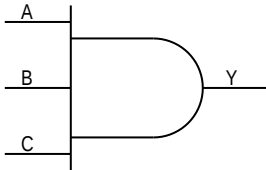
3200DX

40MX

42MX

54SX

AND3



Function

3 Input AND

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Inputs

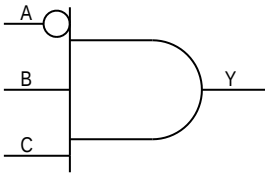
A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

AND3A



Function

3 Input AND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

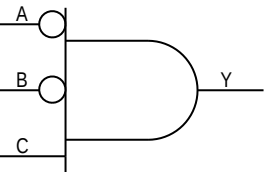
3200DX

40MX

42MX

54SX

AND3B



Function

3 Input AND with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 1

ACT 2/1200XL

ACT 3

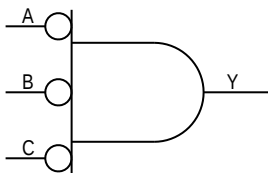
3200DX

40MX

42MX

54SX

AND3C



Function

3 Input AND with active low Inputs

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

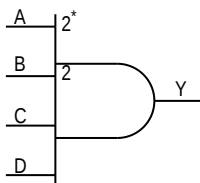
3200DX

40MX

42MX

54SX

AND4



Function

4 Input AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Inputs

A, B, C, D

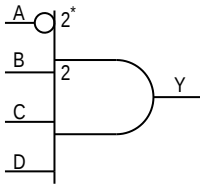
Outputs

Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1/40MX.

AND4A

**Function**

4 Input AND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	1	1	1	1
1	X	X	X	0

Inputs

A, B, C, D

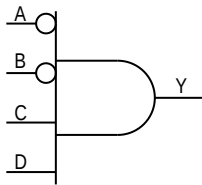
Outputs

Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

AND4B

**Function**

4 Input AND with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	1	1	1
X	1	X	X	0
1	X	X	X	0

Inputs

A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 1

ACT 2/1200XL

ACT 3

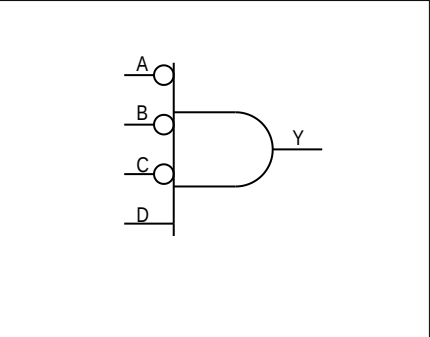
3200DX

40MX

42MX

54SX

AND4C



Inputs
A, B, C, D

Outputs
Y

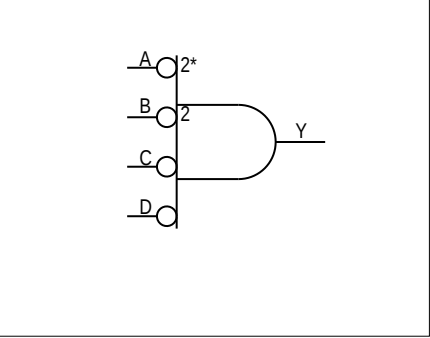
Function
4 Input AND with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	1	1
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
All		1

AND4D



Inputs
A, B, C, D

Outputs
Y

Function
4 Input AND with active low Inputs

Truth Table

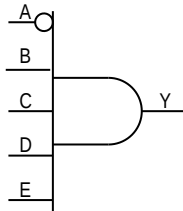
A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except 54SX.

AND5A

54SX



Function

5 Input AND with active low A input

Truth Table

A	B	C	D	E	Y
0	1	1	1	1	1
1	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Inputs

A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

AND5B

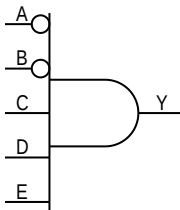
ACT 2/1200XL

ACT 3

3200DX

42MX

54SX



Function

5 Input AND with active low A- and B-Inputs

Truth Table

A	B	C	D	E	Y
X	X	X	X	0	0
X	X	X	0	X	0
X	X	0	X	X	0
0	0	1	1	1	1
X	1	X	X	X	0
1	X	X	X	X	0

Inputs

A, B, C, D, E

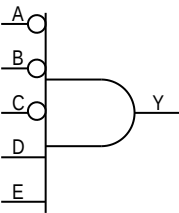
Outputs

Y

Family	Modules	
	Seq	Comb
All		1

54SX

AND5C



Function
5 Input AND with active low A-, B-, and C-inputs

Truth Table

A	B	C	D	E	Y
0	0	0	1	1	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Inputs

A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

AO1

```
graph LR; A --- AND1[AND]; B --- AND1; AND1 --- OR1[OR]; C --- OR1; OR1 --- Y
```

Function

3 Input AND-OR

Truth Table

A	B	C	Y
X	0	0	0
X	X	1	1
0	X	0	0
1	1	X	1

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

AO10

```
graph LR; A --- AND1[AND]; B --- AND1; C --- AND1; AND1 --- OR1[OR]; D --- OR1; E --- OR1; OR1 --- AND2[AND]; A --- AND2; AND2 --- Y
```

Function

5 Input AND-OR-AND

Truth Table

A	B	C	D	E	Y
X	X	X	0	0	0
X	0	0	X	X	0
X	X	1	X	1	1
X	X	1	1	X	1
0	X	0	X	X	0
1	1	X	X	1	1
1	1	X	1	X	1

Inputs

A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

ACT 2/1200XL

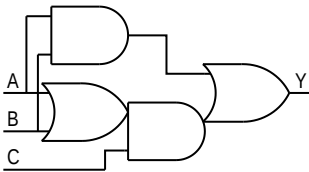
ACT 3

3200DX

42MX

54SX

AO11



Function

3 Input AND-OR

Truth Table

A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Inputs

A, B, C

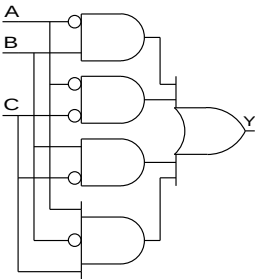
Outputs

Y

Family	Modules	
	Seq	Comb
All		1

54SX

AO12



Function

3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Inputs

A, B, C

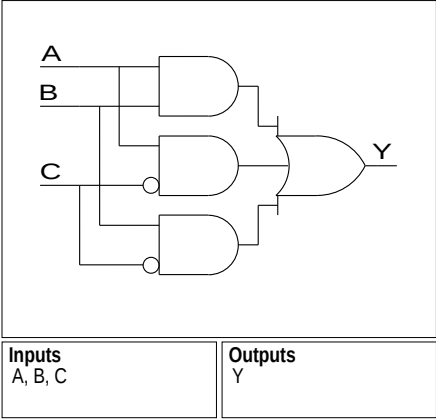
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AO13



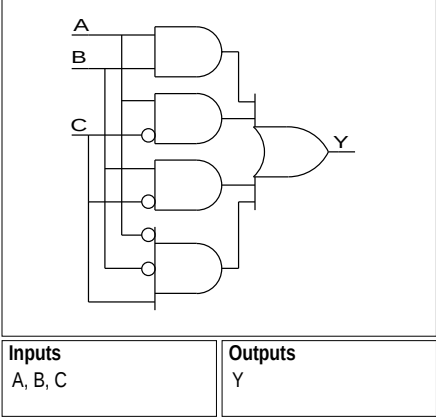
Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

AO14



Function
3 Input AND-OR

Truth Table

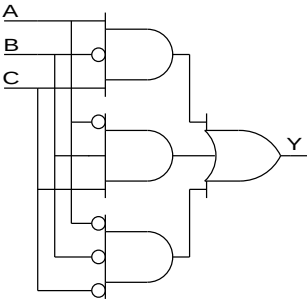
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

54SX

Family	Modules	
	Seq	Comb
54SX		1

54SX

AO15



Function
3 Input AND-OR

Truth Table

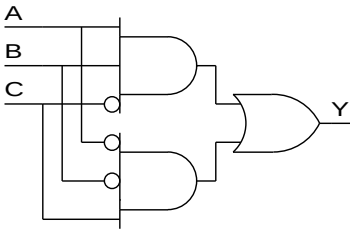
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Inputs	Outputs
A, B, C	Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AO16



Function
3 Input AND-OR

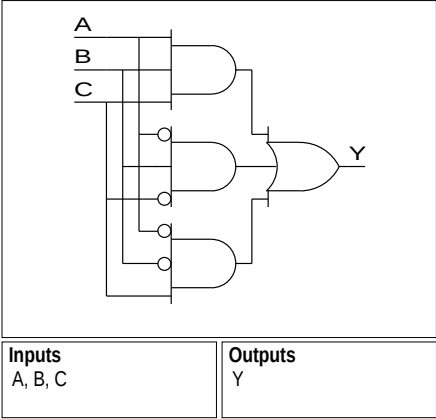
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Inputs	Outputs
A, B, C	Y

Family	Modules	
	Seq	Comb
54SX		1

AO17



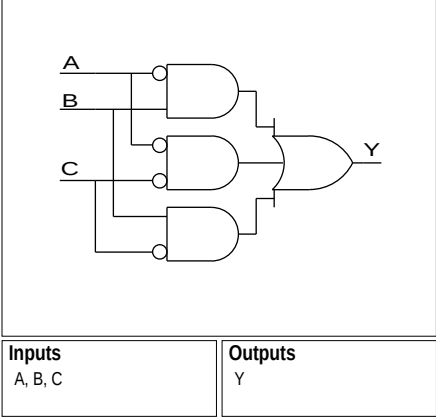
Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

AO18



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

ACT 1

ACT 2/1200XL

ACT 3

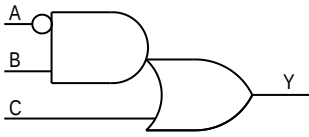
3200DX

40MX

42MX

54SX

AO1A

**Function**

3 Input AND-OR with active low A-Input

A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

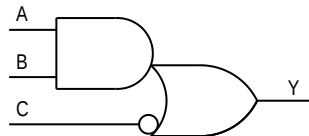
3200DX

40MX

42MX

54SX

AO1B

**Function**

3 Input AND-OR with active low C-Input

Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

AO1C

```
graph LR; A((A)) --- AND1[AND]; B((B)) --- AND1; AND1 --- OR1[OR]; C((C)) --- OR1; OR1 --- Y((Y))
```

Function

3 Input AND-OR with active low A- and C-Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

AO1D

```
graph LR; A((A)) --- AND1[AND]; B((B)) --- AND1; AND1 --- OR1[OR]; C((C)) --- OR1; OR1 --- Y((Y))
```

Function

3 Input AND-OR with active low A- and B-Inputs

Truth Table

A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

ACT 2/1200XL

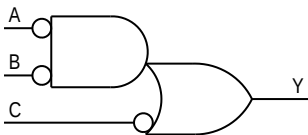
ACT 3

3200DX

42MX

54SX

AO1E



Function

3 Input AND-OR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

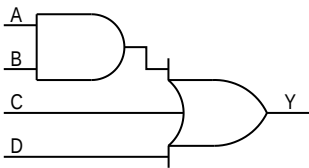
3200DX

40MX

42MX

54SX

AO2



Function

4 Input AND-OR

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	X	0	0	0
1	1	X	X	1

Inputs

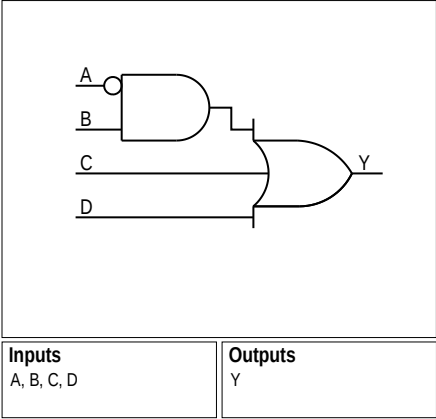
A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

AO2A



Function
4 Input AND-OR with active low A-Input

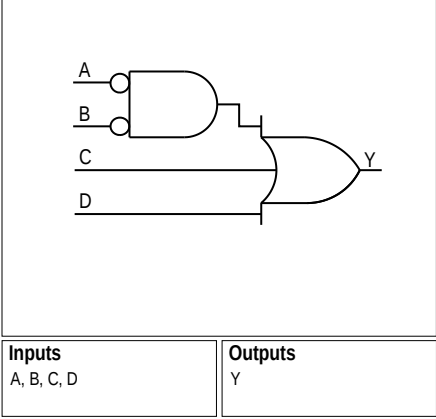
Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	1	X	X	1
1	X	0	0	0

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

AO2B



Function
4 Input AND-OR with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

ACT 2/1200XL

ACT 3

3200DX

42MX

54SX

AO2C

Inputs
A, B, C, D

Outputs
Y

Function
4 Input AND-OR with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
1	X	1	0	0
X	0	1	0	0
0	1	X	X	1
X	X	0	X	1
X	X	X	1	1

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL

ACT 3

3200DX

42MX

54SX

AO2D

Inputs
A, B, C, D

Outputs
Y

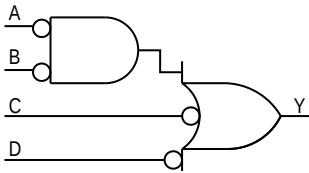
Function
4 Input AND-OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	1
0	0	X	X	1
X	1	1	0	0
X	X	X	1	1
1	X	1	0	0

Family	Modules	
	Seq	Comb
All		1

AO2E



Inputs
A, B, C, D

Outputs
Y

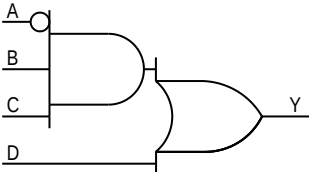
Function
4 Input AND-OR with active low Inputs

Truth Table				
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

AO3



Inputs
A, B, C, D

Outputs
Y

Function
4 Input AND-OR with active low A Input

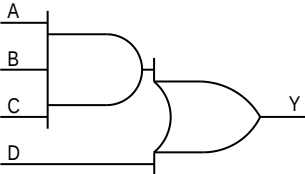
Truth Table				
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	1	1	X	1
1	X	X	0	0

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 2/1200XL

AO3A



Inputs
A, B, C, D

Outputs
Y

Function
4 Input AND-OR

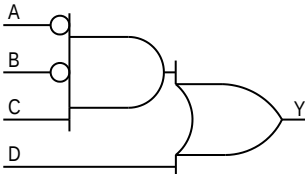
Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	X	X	0	0
1	1	1	X	1

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL

AO3B



Inputs
A, B, C, D

Outputs
Y

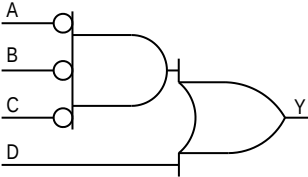
Function
4 Input AND-OR with active low A-, B- Inputs

Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
0	0	1	X	1
X	1	X	0	0
1	X	X	0	0

Family	Modules	
	Seq	Comb
All		1

AO3C



Inputs
A, B, C, D

Outputs
Y

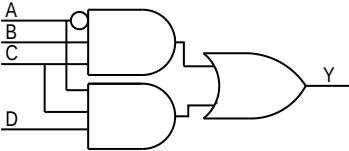
Function
4 Input AND-OR with active low A-, B-, C- Inputs

Truth Table				
A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

AO4A



Inputs
A, B, C, D

Outputs
Y

Function
4 Input AND-OR

Truth Table				
A	B	C	D	Y
X	X	0	X	0
X	0	X	0	0
0	0	X	X	0
0	1	1	X	1
1	X	1	1	1
1	X	X	0	0
X	1	1	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 1

AO5A

ACT 2/1200XL

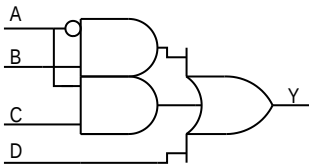
ACT 3

3200DX

40MX

42MX

54SX



Function
4 Input AND-OR

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
0	0	X	0	0
0	1	X	X	1
1	X	1	X	1
1	X	0	0	0
X	1	1	X	1

Inputs

A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL

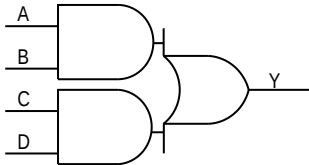
ACT 3

3200DX

42MX

54SX

AO6



Function
2-wide 4-Inputs AND-OR

Truth Table

A	B	C	D	Y
X	0	X	0	0
X	0	0	X	0
X	X	1	1	1
0	X	X	0	0
0	X	0	X	0
1	1	X	X	1

Inputs

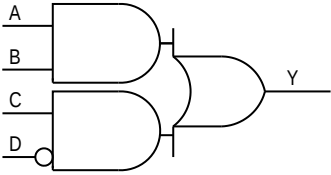
A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

AO6A



Inputs
A, B, C, D

Outputs
Y

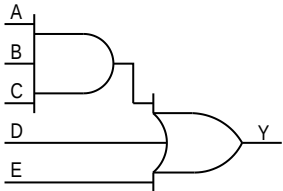
Function
2-wide 4-inputs AND-OR with active low D-Input

Truth Table				
A	B	C	D	Y
X	0	0	X	0
X	X	1	0	1
X	0	X	1	0
0	X	0	X	0
0	X	X	1	0
1	1	X	X	1

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

AO7



Inputs
A, B, C, D, E

Outputs
Y

Function
5 Input AND-OR

A	B	C	D	E	Y
X	X	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	0	X	0	0	0
0	X	X	0	0	0
1	1	1	X	X	1

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

ACT 2/1200XL

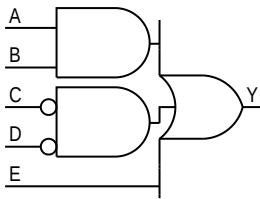
ACT 3

3200DX

42MX

54SX

AO8

**Function**

5 Input AND-OR with active low C- and D-Inputs

Truth Table

A	B	C	D	E	Y
X	X	0	0	X	1
X	0	X	1	0	0
X	X	X	X	1	1
X	0	1	X	0	0
0	X	X	1	0	0
0	X	1	X	0	0
1	1	X	X	X	1

Inputs

A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL

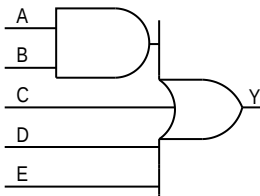
ACT 3

3200DX

42MX

54SX

AO9

**Function**

5 Input AND-OR

Truth Table

A	B	C	D	E	Y
X	0	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
0	X	0	0	0	0
1	1	X	X	X	1

Inputs

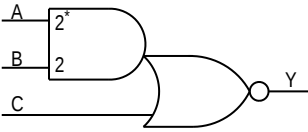
A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

AOI1



Inputs
A, B, C

Outputs
Y

Function
3 Input AND-OR-INVERT

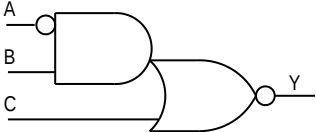
Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	X	0	1
1	1	X	0

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

AOI1A



Inputs
A, B, C

Outputs
Y

Function
3 Input AND-OR-INVERT with active low A-Input

Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

AOI1B

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

Inputs
A, B, C

Outputs
Y

Function
3 Input AND-OR-INVERT with active low C-Input

Truth Table

A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

Family	Modules	
	Seq	Comb
All		1

AOI1C

ACT 2/1200XL

ACT 3

3200DX

42MX

54SX

Inputs
A, B, C

Outputs
Y

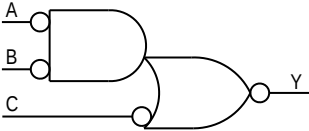
Function
3 Input AND-OR-INVERT with active low A- and B-Inputs

Truth Table

A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Family	Modules	
	Seq	Comb
All		1

AOI1D



Inputs
A, B, C

Outputs
Y

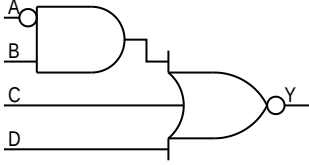
Function
3 Input AND-OR-INVERT with active low Inputs

Truth Table			
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

AOI2A



Inputs
A, B, C, D

Outputs
Y

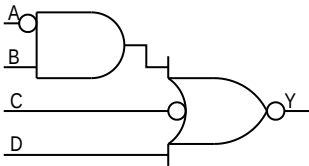
Function
4 Input AND-OR-INVERT with active low A-Input

Truth Table				
A	B	C	D	Y
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
0	1	X	X	0
1	X	0	0	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

AOI2B



Function
4 Input AND-OR-INVERT with active low A- and C-Inputs

Truth Table

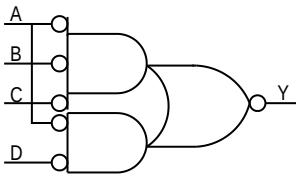
A	B	C	D	Y
X	X	0	X	0
X	0	1	0	1
X	X	X	1	0
0	1	X	X	0
1	X	1	0	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AOI3A



Function
4 Input AND-OR-INVERT with active low Inputs

Truth Table

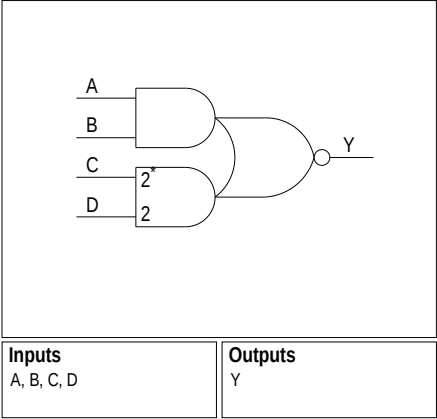
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AOI4



Function
2-wide 4-Inputs AND-OR-INVERT

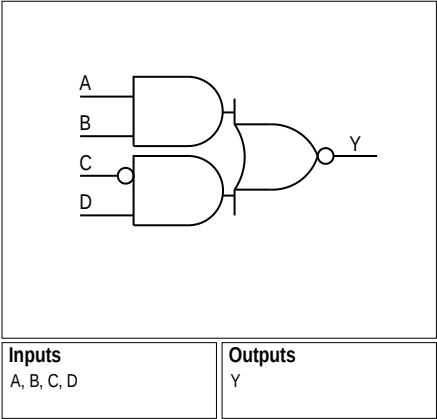
Truth Table

A	B	C	D	Y
X	0	X	0	1
X	0	0	X	1
X	X	1	1	0
0	X	X	0	1
0	X	0	X	1
1	1	X	X	0

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except 54SX.

AOI4A



Function
2-wide 4-Inputs AND-OR-INVERT with active low C-Input

Truth Table

A	B	C	D	Y
X	0	X	0	1
X	X	0	1	0
X	0	1	X	1
0	X	X	0	1
0	X	1	X	1
1	1	X	X	0

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 2/1200XL

ACT 3

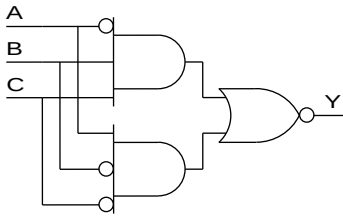
3200DX

42MX

54SX

54SX

AOI5



Function
3-Input AND-OR-INVERT

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0

Inputs

A, B, C

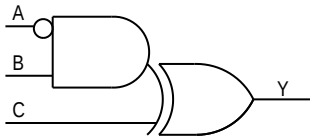
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 1

AX1



Function
3 Input AND-XOR with active low A-Input

Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	1	0	1
0	1	1	0
1	X	0	0
1	X	1	1

Inputs

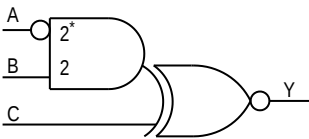
A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

AX1A



Inputs
A, B, C

Outputs
Y

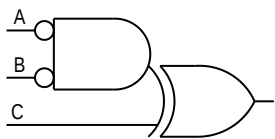
Function
3 Input AND-XOR-INVERT with active low A-Input

Truth Table			
A	B	C	Y
X	0	0	1
X	0	1	0
0	1	0	0
0	1	1	1
1	X	0	1
1	X	1	0

Family	Modules	
	Seq	Comb
ACT 1/40MX/54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except ACT 1, 40MX, and 54SX.

AX1B



Inputs
A, B, C

Outputs
Y

Function
3 Input AND-XOR with active low A- and B-Inputs

Truth Table			
A	B	C	Y
0	0	0	1
0	0	1	0
X	1	0	0
X	1	1	1
1	X	0	0
1	X	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 2/1200XL

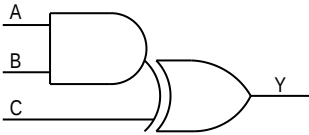
ACT 3

3200DX

42MX

54SX

AX1C



Inputs
A, B, C

Outputs
Y

Function
3 Input AND-XOR

Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	X	0	0
0	X	1	1
1	1	0	1
1	1	1	0

Family	Modules	
	Seq	Comb
All		1

AX1D



Inputs
A, B, C

Outputs
Y

Function
3 Input AND-XOR

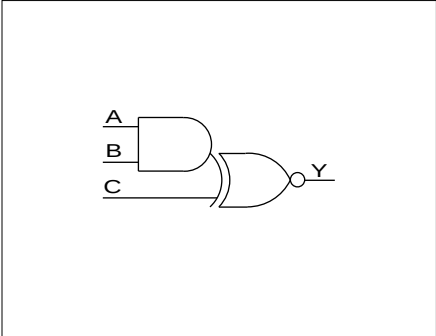
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

54SX

AX1E



Function
3 Input AND-XNOR

Truth Table

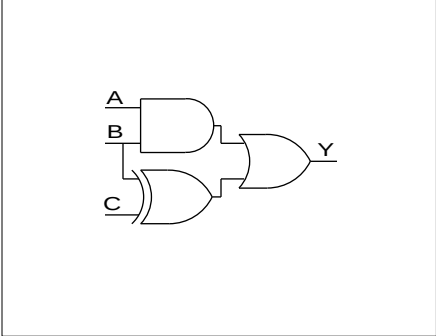
A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXO1



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

Inputs
A, B, C

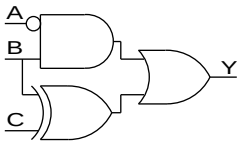
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

54SX

AXO2



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

Inputs

A, B, C

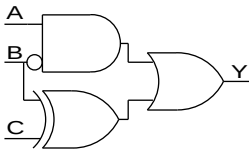
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXO3



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Inputs

A, B, C

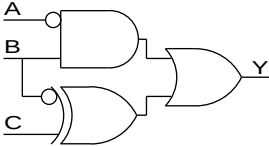
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXO5



Inputs
A, B, C

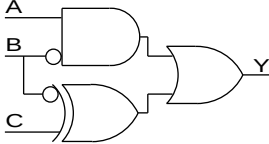
Outputs
Y

Function
3-Input Gate

Truth Table			
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

AXO6



Inputs
A, B, C

Outputs
Y

Function
3-Input Gate

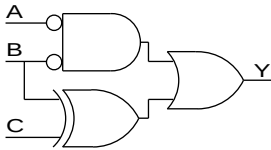
Truth Table			
A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

54SX

54SX

AXO7



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Inputs

A, B, C

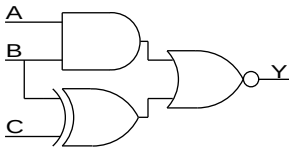
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXOI1



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI2

```
graph LR; A((A)) --> NOT1[NOT]; NOT1 --> AND1[AND]; B((B)) --> AND1; AND1 --> OR1[OR]; C((C)) --> OR1; OR1 --> Y((Y))
```

Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI3

```
graph LR; A((A)) --> NOT1[NOT]; NOT1 --> AND1[AND]; B((B)) --> AND1; AND1 --> OR1[OR]; C((C)) --> OR1; OR1 --> Y((Y))
```

Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

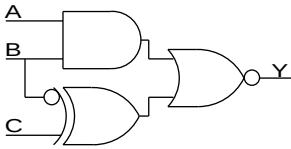
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXOI4



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Inputs

A, B, C

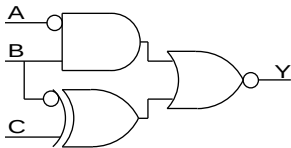
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXOI5



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI7

```
graph LR; A((A)) --- AND1[AND]; B((B)) --- AND1; B --- AND2[AND]; C((C)) --- AND2; AND1 --- OR[OR]; AND2 --- OR; OR --- Y((Y))
```

Function
3-Input Gate

Truth Table

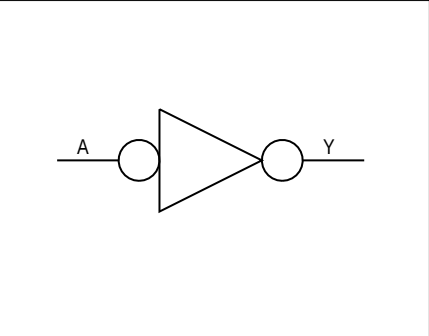
A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

BUFA



Function
Buffer, with active low Input and Output

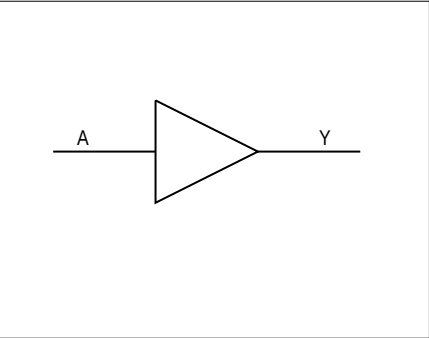
Truth Table

A	Y
0	0
1	1

Inputs	Outputs
A	Y

Family	Modules	
	Seq	Comb
All		1

BUFF



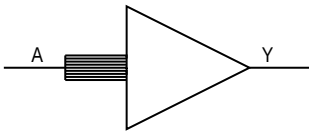
Function
Buffer

Truth Table

A	Y
0	0
1	1

Inputs	Outputs
A	Y

Family	Modules	
	Seq	Comb
All		1

CLKINT**Function**

Internal Clock Interface

A	Y
0	0
1	1

Inputs

A

Outputs

Y

NOTE: CLKINT does not use any modules.
For more information on the Global Clock Network, refer to Actel's Databook.

ACT 2/1200XL

3200DX

42MX

54SX

ACT 2/1200XL

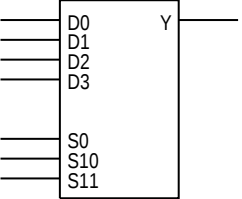
ACT 3

3200DX

42MX

54SX

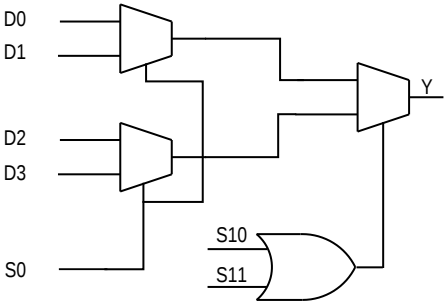
CM7



Inputs
D0, D1, D2, D3, S0, S10,
S11

Outputs
Y

Function
Full Combinational Module

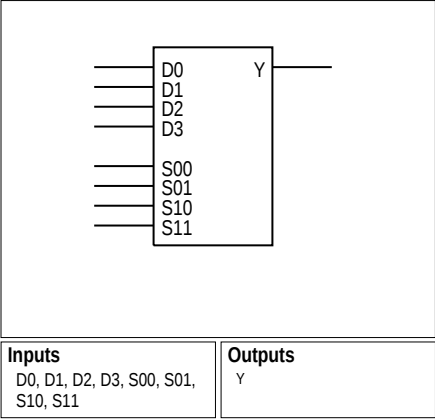


Truth Table

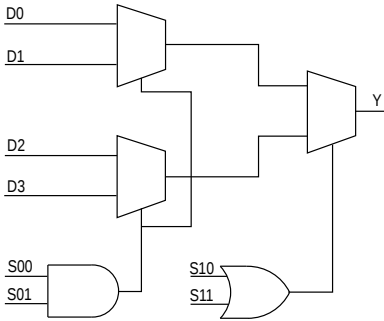
S11	S10	S0	Y
0	0	0	D0
0	0	1	D1
X	1	0	D2
1	X	0	D2
X	1	1	D3
1	X	1	D3

Family	Modules	
	Seq	Comb
All		1

CM8



Function
Full Combinational Module



Truth Table

S11	S10	S01	S00	Y
0	0	X	0	D0
0	0	0	X	D0
0	0	1	1	D1
X	1	X	0	D2
X	1	0	X	D2
1	X	X	0	D2
1	X	0	X	D2
X	1	1	1	D3
1	X	1	1	D3

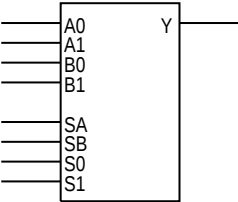
Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

ACT 1

40MX

CM8A



Inputs

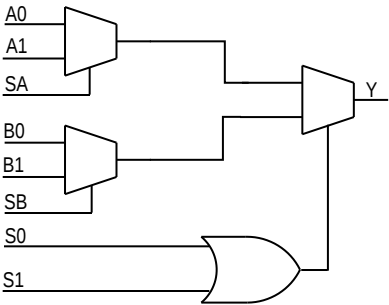
A0, A1, B0, B1, SA, SB, S0, S1

Outputs

Y

Function

Full Combinational Module

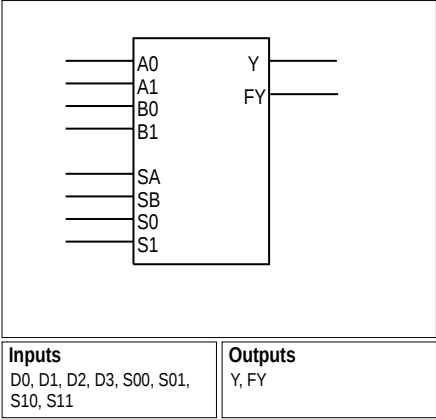


Truth Table

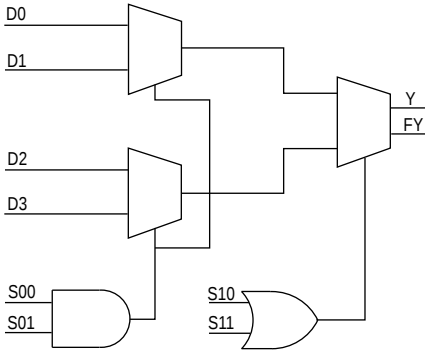
S0	S1	SA	SB	Y
0	0	0	X	A0
0	0	1	X	A1
1	X	X	0	B0
X	1	X	0	B0
1	X	X	1	B1
X	1	X	1	B1

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

CM8F



Function
Full Combinational Module with fast output



Truth Table

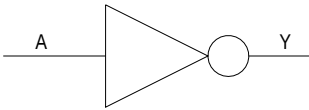
S11	S10	S01	S00	Y	FY
0	0	X	0	D0	D0
0	0	0	X	D0	D0
0	0	1	1	D1	D1
X	1	X	0	D2	D2
X	1	0	X	D2	D2
1	X	X	0	D2	D2
1	X	0	X	D2	D2
X	1	1	1	D3	D3
1	X	1	1	D3	D3

Family	Modules	
	Seq	Comb
54SX		1

NOTE: FY is a fast output that has a maximum fanout of 1.

54SX

CM8INV



Function
Inverter with active low output

Truth Table

A	Y
0	1
1	0

Inputs

A

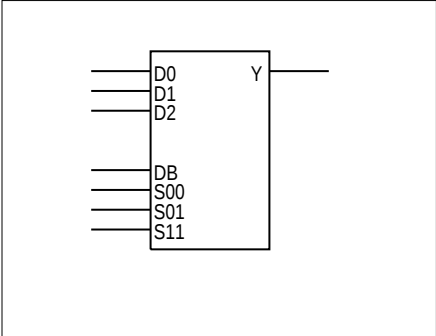
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		0

NOTE: This macro can drive any number of CM8 pins and will be absorbed into that module

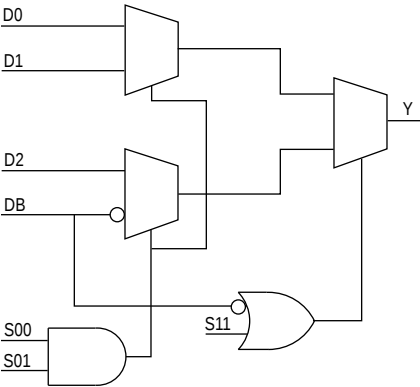
CMB7



Inputs
D0, D1, D2, DB, S00, S01, S11

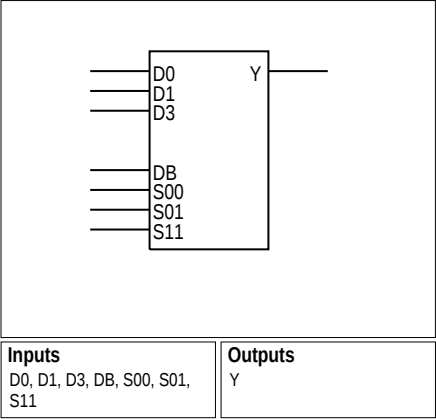
Outputs
Y

Function
Full Combinational Module

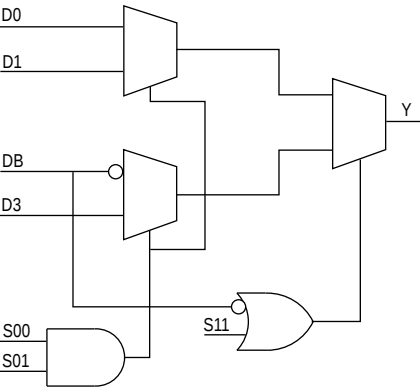


Family	Modules	
	Seq	Comb
54SX		1

CMBB

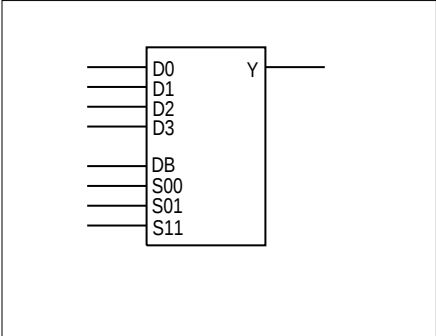


Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

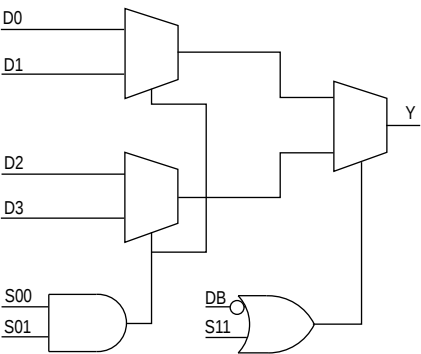
CMBF



Inputs
D0, D1, D2, D3, DB, S00,
S01, S11

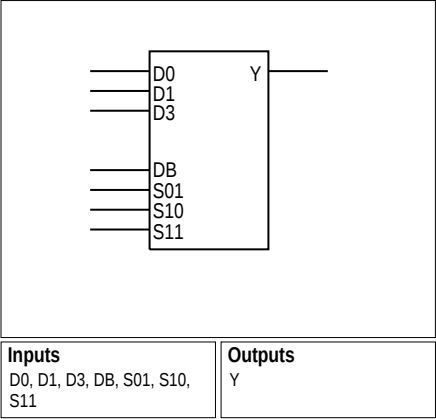
Outputs
Y

Function
Full Combinational Module

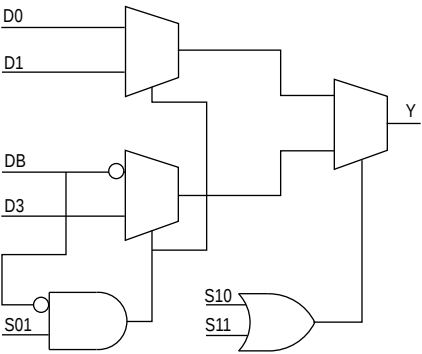


Family	Modules	
	Seq	Comb
54SX		1

CMEB

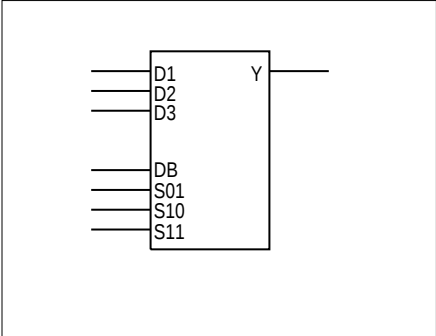


Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

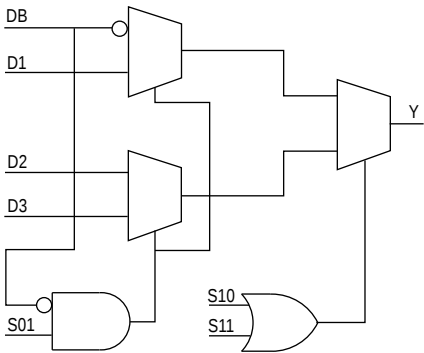
CMEE



Inputs
D1, D2, D3, DB, S01, S10, S11

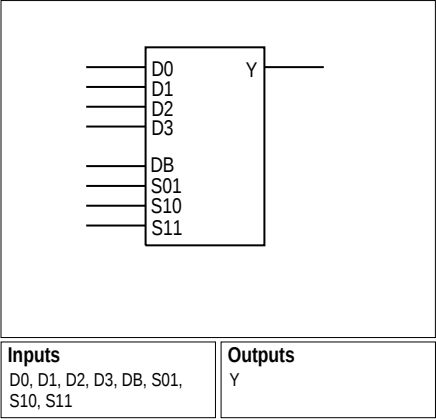
Outputs
Y

Function
Full Combinational Module

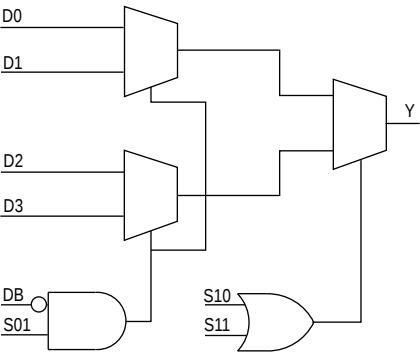


Family	Modules	
	Seq	Comb
54SX		1

CMEF

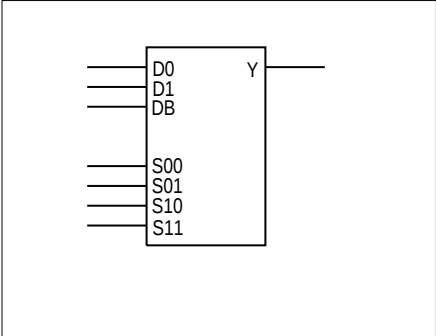


Function
Full Combinational Module



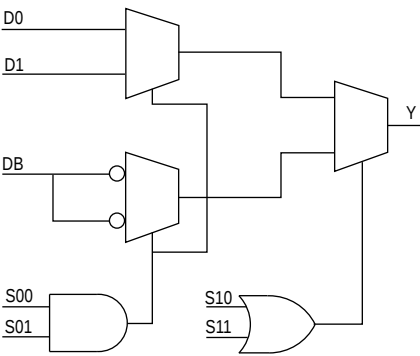
Family	Modules	
	Seq	Comb
54SX		1

CMF3



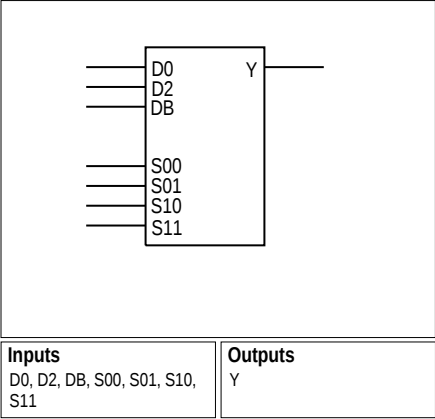
Inputs	Outputs
D0, D1, DB, S00, S01, S10, S11	Y

Function
Full Combinational Module

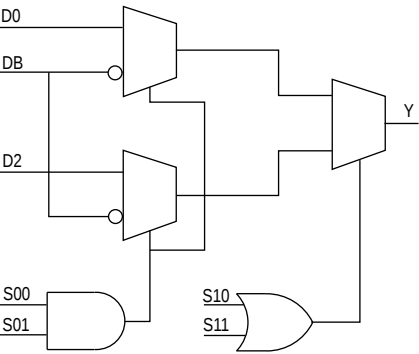


Family	Modules	
	Seq	Comb
54SX		1

CMF5

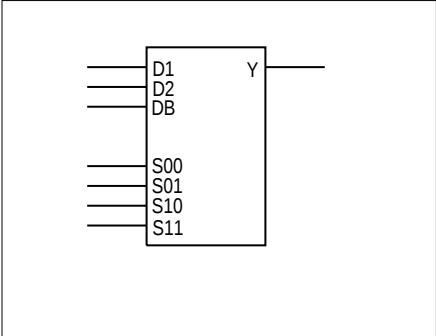


Function
Full Combinational Module

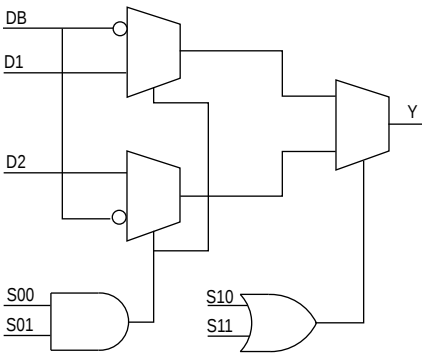


Family	Modules	
	Seq	Comb
54SX		1

CMF6



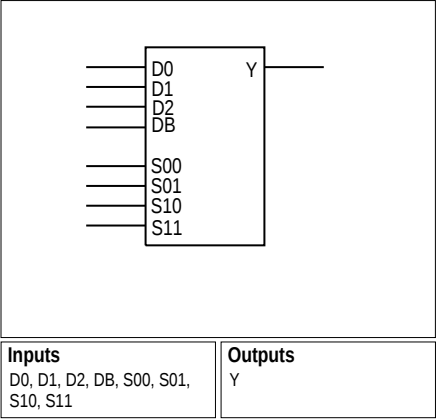
Function
Full Combinational Module



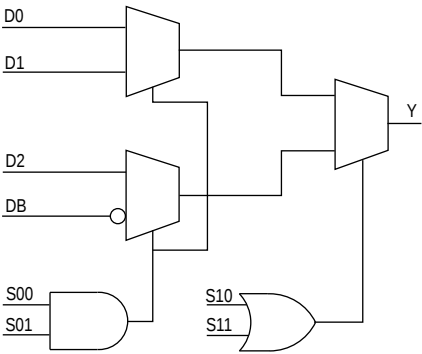
Inputs	Outputs
D1, D2, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
54SX		1

CMF7

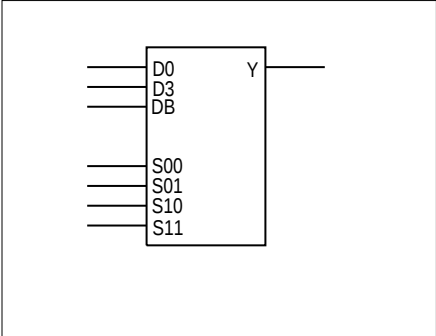


Function
Full Combinational Module

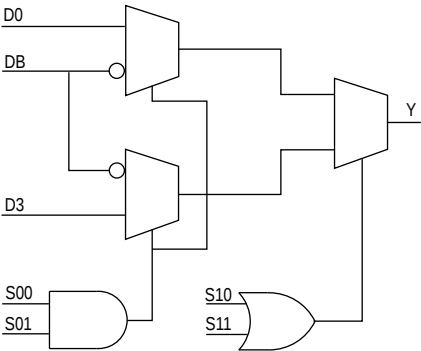


Family	Modules	
	Seq	Comb
54SX		1

CMF9



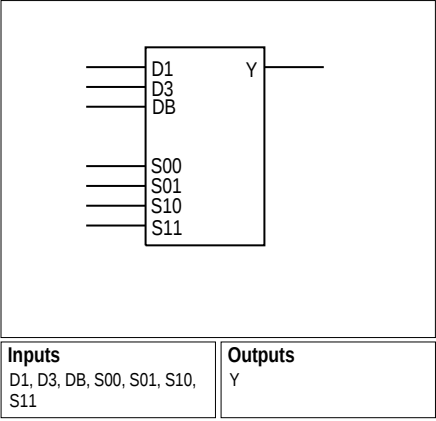
Function
Full Combinational Module



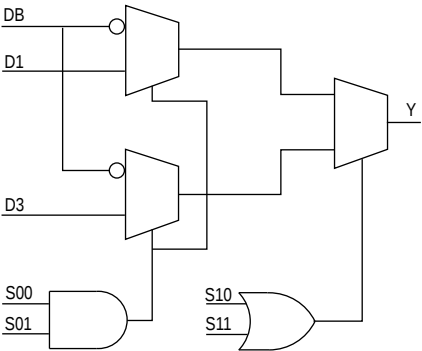
Inputs	Outputs
D0, D3, DB, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
54SX		1

CMFA



Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

CMFB

D0

D1

D3

DB

S00

S01

S10

S11

Y

Inputs

D0, D1, D3, DB, S00, S01, S10, S11

Outputs

Y

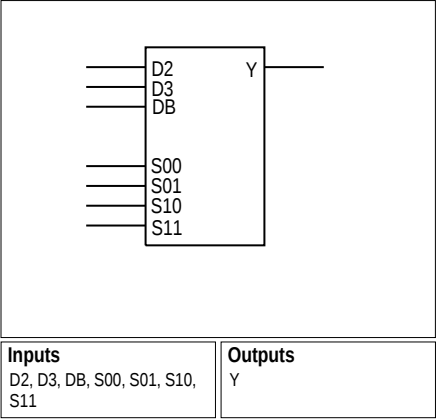
Function

Full Combinational Module

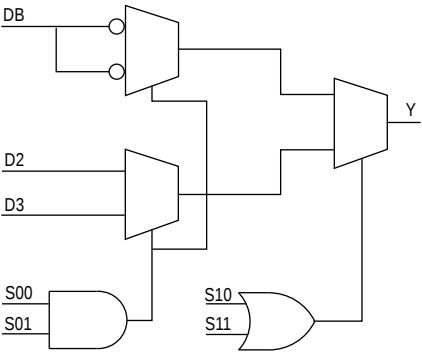
```
graph LR
    D0 --- AND1[AND]
    D1 --- AND1
    DB --- AND2[AND]
    D3 --- AND2
    S00 --- AND3[AND]
    S01 --- AND3
    S10 --- OR1[OR]
    S11 --- OR1
    AND1 --- AND4[AND]
    AND2 --- AND4
    AND3 --- AND4
    OR1 --- AND4
    AND4 --- Y
```

Family	Modules	
	Seq	Comb
54SX		1

CMFC

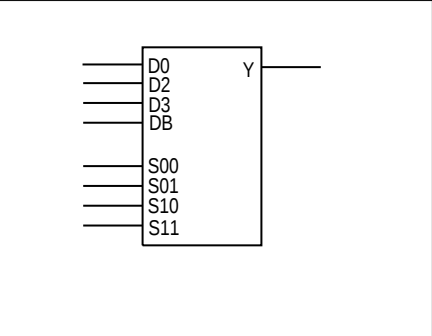


Function
Full Combinational Module

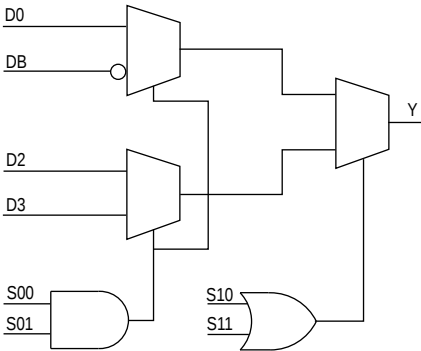


Family	Modules	
	Seq	Comb
54SX		1

CMFD



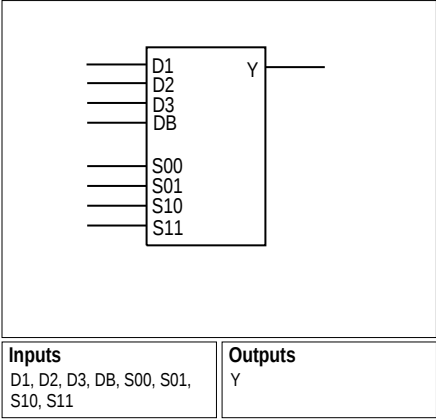
Function
Full Combinational Module



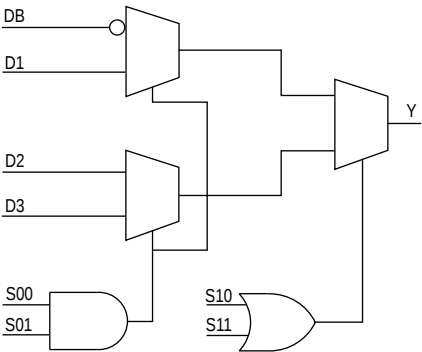
Inputs	Outputs
D0, DB, D2, D3, S00, S01, S10, S11	Y

Family	Modules	
	Seq	Comb
54SX		1

CMFE

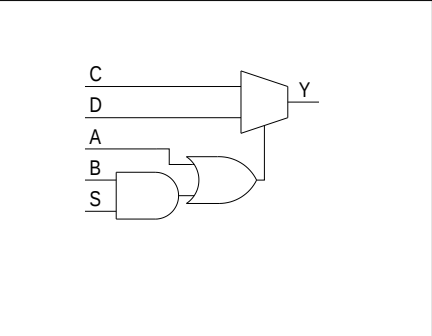


Function
Full Combinational Module



Family	Modules	
	Seq	Comb
54SX		1

CS1



Inputs
A, S, B, C, D

Outputs
Y

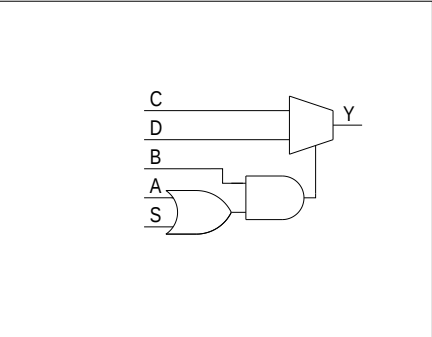
Function
Carry Select for Implementing High Speed Adders

Truth Table					
A	S	B	C	D	Y
X	X	X	0	0	0
0	X	0	0	X	0
0	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	X	X	1	1
1	X	X	X	0	0
X	X	X	1	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

CS2



Inputs
A, S, B, C, D

Outputs
Y

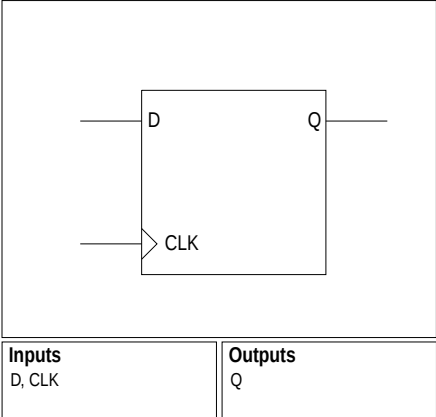
Function
Carry Select for Implementing High Speed Adders

Truth Table					
A	S	B	C	D	Y
X	X	X	0	0	0
X	X	0	0	X	0
X	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	1	X	1	1
1	X	1	X	0	0
X	X	X	1	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

DF1



Function
D-Type Flip-Flop

Truth Table

CLK	Q _{n+1}
↑	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

ACT 2/1200XL

ACT 3

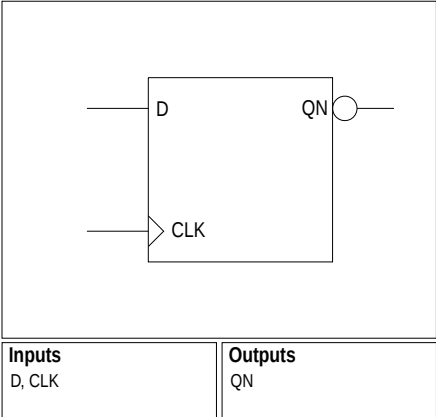
3200DX

40MX

42MX

54SX

DF1A



Function
D-Type Flip-Flop with active low Output

Truth Table

CLK	QN _{n+1}
↑	!D

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

ACT 1

DF1B

ACT 2/1200XL

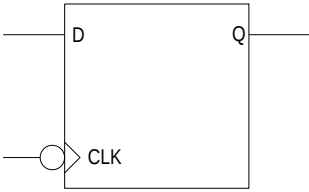
ACT 3

3200DX

40MX

42MX

54SX



Function
D-Type Flip-Flop with active low Clock

Truth Table

CLK	Q_{n+1}
↓	D

Inputs

D, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

DF1C

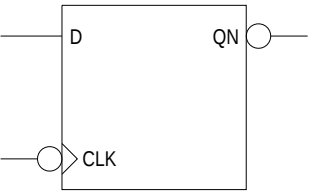
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX



Function
D-Type Flip-Flop with active low Clock and Output

Truth Table

CLK	QN_{n+1}
↓	!D

Inputs

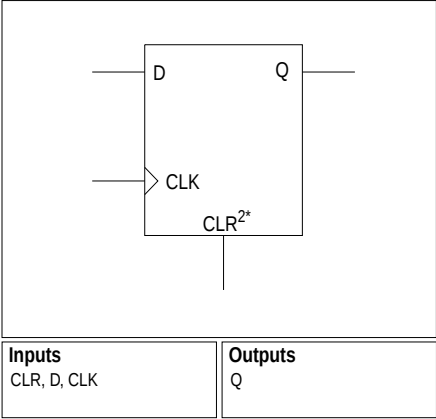
D, CLK

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFC1



Function
D-Type Flip-Flop, with active high Clear

Truth Table

CLR	CLK	Q _{n+1}
1	X	0
0	↑	D

Inputs CLR, D, CLK	Outputs Q
------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

ACT 1

ACT 2/1200XL

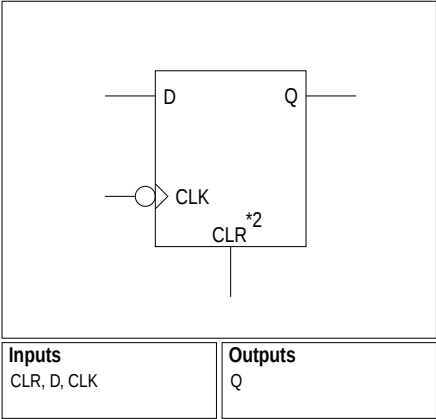
ACT 3

3200DX

40MX

42MX

DFC1A



Function
D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

CLR	CLK	Q _{n+1}
1	X	0
0	↓	D

Inputs CLR, D, CLK	Outputs Q
------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

ACT 1

ACT 2/1200XL

ACT 3

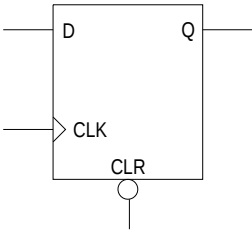
3200DX

40MX

42MX

54SX

DFC1B



Function
D-Type Flip-Flop, with active low Clear

Truth Table

CLR	CLK	Q_{n+1}
0	X	0
1	$\uparrow$	D

Inputs

CLR, D, CLK

Outputs

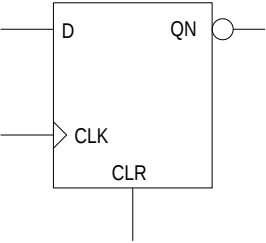
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

40MX

DFC1C



Function
D-Type Flip-Flop, with active high Clear and Clock

Truth Table

CLR	CLK	QN_{n+1}
1	X	1
0	$\uparrow$	!D

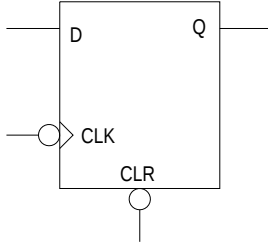
Inputs

CLR, D, CLK

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFC1D**Function**

D-Type Flip-Flop, with active low Clear and Clock

Truth Table

CLR	CLK	Q_{n+1}
0	X	0
1	↓	D

Inputs

CLR, D, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

ACT 2/1200XL

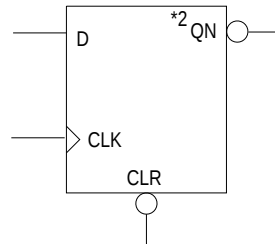
ACT 3

3200DX

40MX

42MX

54SX

DFC1E**Function**

D-Type Flip-Flop, with active low Clear and Output

Truth Table

CLR	CLK	QN_{n+1}
0	X	1
1	↑	!D

Inputs

CLR, D, CLK

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

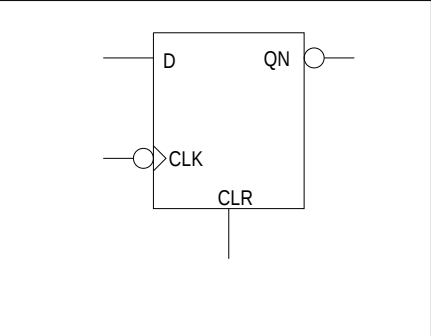
42MX

* A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

ACT 1

40MX

DFC1F



Function
D-Type Flip-Flop, with active high Clear, active low Clock and Output

Truth Table

CLR	CLK	Q _{N+1}
1	X	1
0	↓	!D

Inputs CLR, D, CLK	Outputs QN
------------------------------	----------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

ACT 2/1200XL

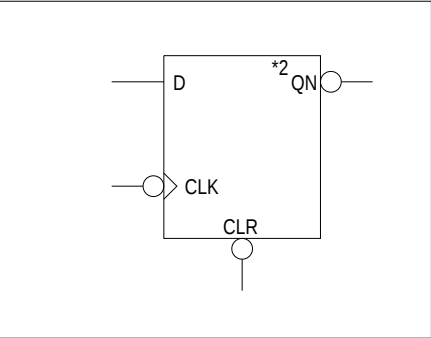
ACT 3

3200DX

40MX

42MX

DFC1G



Function
D-Type Flip-Flop, with active low Clear, Clock and Output

Truth Table

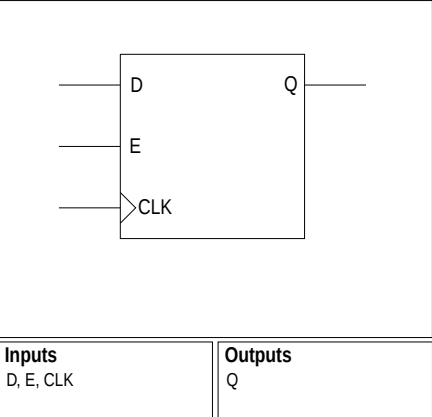
CLR	CLK	Q _{n+1}
0	X	1
1	↓	!D

Inputs CLR, D, CLK	Outputs QN
------------------------------	----------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

DFE



Function
D-Type Flip-Flop, with active high Enable

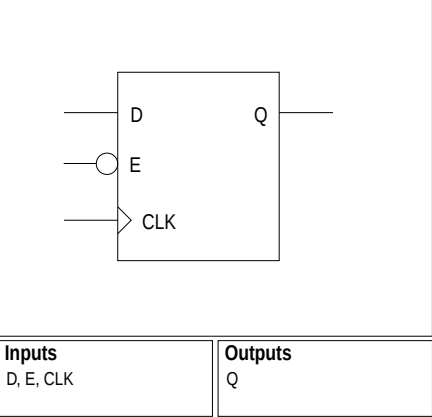
Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↑	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFE1B



Function
D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↑	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 1

ACT 2/1200XL

ACT 3

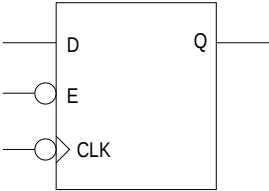
3200DX

40MX

42MX

54SX

DFE1C



Function
D-Type Flip-Flop, with active low Enable and Clock

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↓	D

Inputs

D, E, CLK

Outputs

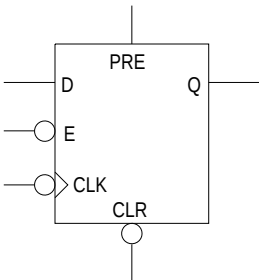
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

40MX

DFE2D



Function
D-Type Flip-Flop, with active high Preset, active low Enable, Clear, and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↓	D
0	1	X	X	*

Inputs

CLR, D, E, PRE, CLK

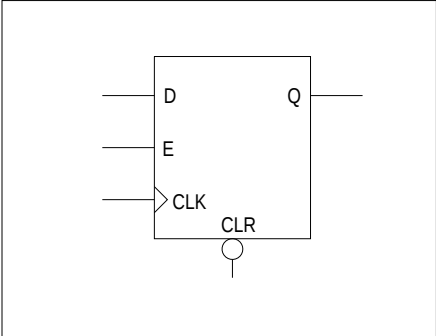
Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFE3A



Function
D-Type Flip-Flop, with Enable and active low Clear

Truth Table

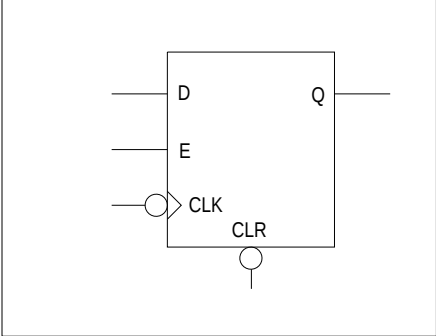
CLR	E	CLK	Q _{n+1}
0	X	X	0
1	0	X	Q
1	1	↑	D

Inputs	Outputs
CLR, D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFE3B



Function
D-Type Flip-Flop, with Enable and active low Clear and Clock

Truth Table

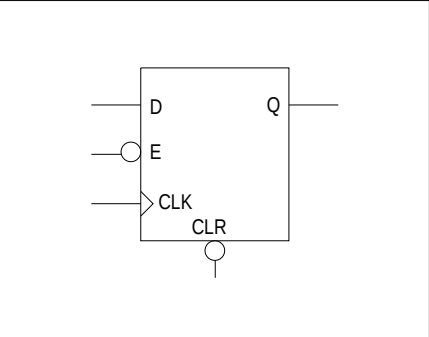
CLR	E	CLK	Q _{n+1}
0	X	X	0
1	0	X	Q
1	1	↓	D

Inputs	Outputs
CLR, D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFE3C



Function
D-Type Flip-Flop, with active low Enable, and Clear

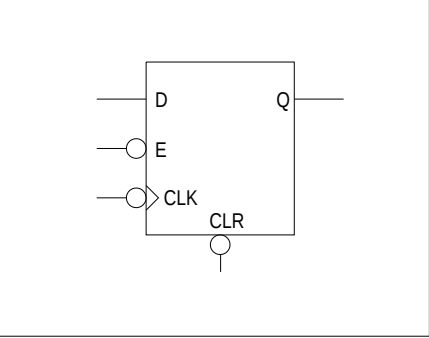
Truth Table

CLR	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Inputs	Outputs
CLR, D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE3D



Function
D-Type Flip-Flop, with active low Enable, Clear and Clock

Truth Table

CLR	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↓	D

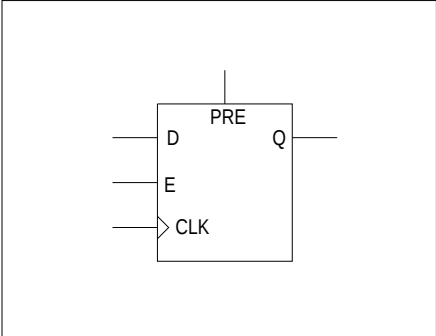
Inputs	Outputs
CLR, D, E, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

40MX

DfE4



Function
D-Type Flip-Flop, with active high Enable and Preset

Truth Table

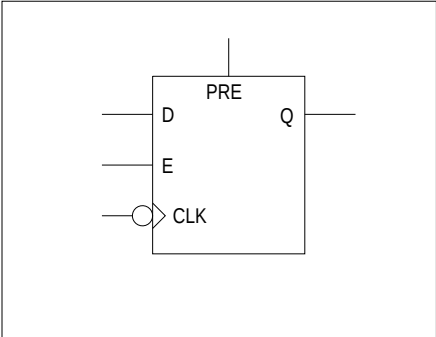
PRE	E	CLK	Q _{n+1}
1	X	X	1
0	0	X	Q
0	1	↑	D

Inputs
D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DfE4A



Function
D-Type Flip-Flop, with active high Enable and Preset, and active low Clock

Truth Table

PRE	E	CLK	Q _{n+1}
1	X	X	1
0	0	X	Q
0	1	↓	D

Inputs
D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

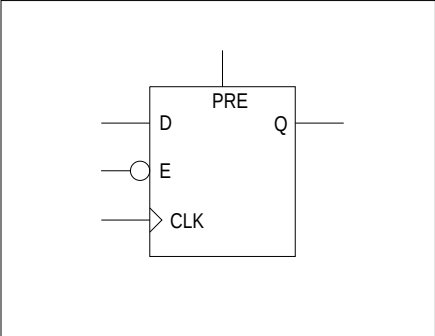
ACT 1

40MX

ACT 1

40MX

DFE4B



Function
D-Type Flip-Flop, with active low Enable, and active high Preset

Truth Table

PRE	E	CLK	Q _{n+1}
1	X	X	1
0	1	X	Q
0	0	↑	D

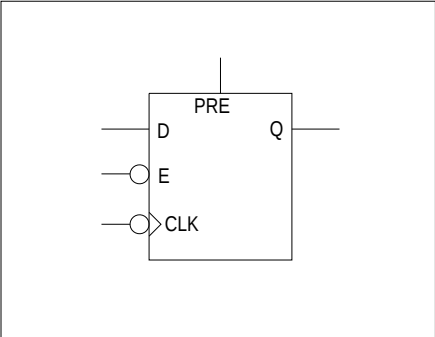
Inputs D, E, PRE, CLK	Outputs Q
---------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

DFE4C



Function
D-Type Flip-Flop, with active low Enable and Clock, and active high Preset

Truth Table

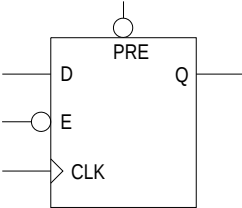
PRE	E	CLK	Q _{n+1}
1	X	X	1
0	1	X	Q
0	0	↓	D

Inputs D, E, PRE, CLK	Outputs Q
---------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

54SX

DFE4F



Inputs
D, E, PRE, CLK

Outputs
Q

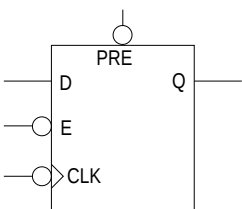
Function
D-Type Flip-Flop, with active low Enable, and active low Preset

PRE	E	CLK	Q _{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Family	Modules	
	Seq	Comb
54SX	1	

54SX

DFE4G



Inputs
D, E, PRE, CLK

Outputs
Q

Function
D-Type Flip-Flop, with active low Enable and Clock, and active low Preset

Truth Table

PRE	E	CLK	Q _{n+1}
0	X	X	1
1	1	X	Q
1	0	↓	D

Family	Modules	
	Seq	Comb
54SX	1	

ACT 1

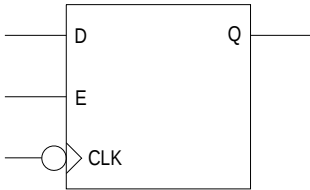
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

DFEA**Function**

D-Type Flip-Flop, with Enable, and active low Clock

Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↓	D

Inputs

D, E, CLK

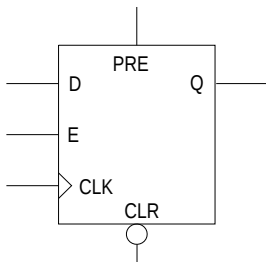
Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

40MX

DFEB**Function**

D-Type Flip-Flop, with Enable, Preset, and active low Clear

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↑	D
0	1	X	X	*

Inputs

CLR, D, E, PRE, CLK

Outputs

Q

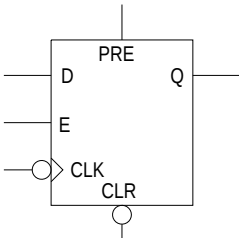
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

ACT 1

40MX

DFEC



Function
D-Type Flip-Flop, with Enable, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↓	D
0	1	X	X	*

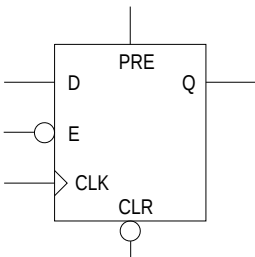
Inputs
CLR, D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFED



Function
D-Type Flip-Flop, with active low Enable and Clear, and active high Preset

Truth Table

CLR	PRE	E	CLK	Q _{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↑	D
0	1	X	X	*

Inputs
CLR, D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

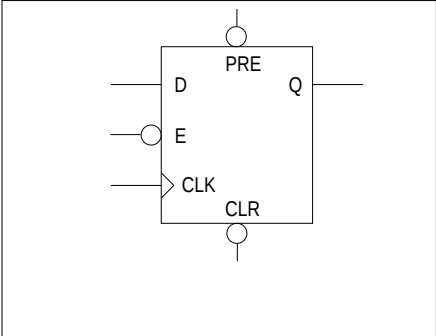
ACT 1

40MX

* You design should not allow both PRE and CLR to be asserted at the same time.

54SX

DFEG



Function
D-Type Flip-Flop with Enable and active low Preset Clear and Clock

Truth Table

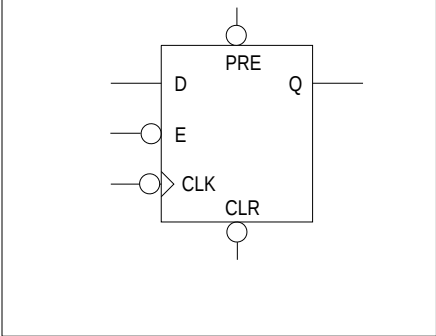
CLR	PRE	E	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	1	Q
1	1	0	↑	D

Inputs CLK, CLR, D, E, PRE	Outputs Q
--------------------------------------	---------------------

Family	Modules	
	Seq	Comb
54SX	1	

54SX

DFEH



Function
D-Type Flip-Flop with active low Enable and Clear and Preset

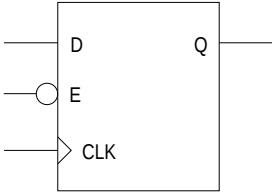
Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↓	D

Inputs CLK, CLR, D, E, PRE	Outputs Q
--------------------------------------	---------------------

Family	Modules	
	Seq	Comb
54SX	1	

IODFE



Function

D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q _{n+1}
1	X	Q
0	↑	D

Inputs

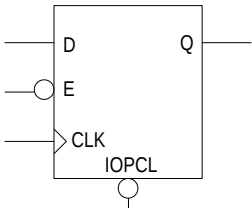
D, E, CLK

Outputs

Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
WARNING: Using the IODFE macro will disable the IOPCLBUF clock network.
NOTE 2: Uses an I/O module.

IODFEC



Function

D-Type Flip-Flop, with active low Enable and Clear

Truth Table

IOPCL	E	CLK	Q _{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

Inputs

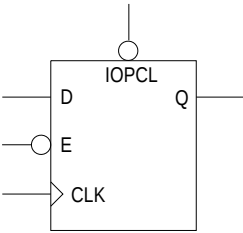
IOPCL, D, E, CLK

Outputs

Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.
NOTE 3: Uses an I/O module.

IODFEP



Function
D-Type Flip-Flop, with active low Enable and Preset

Truth Table

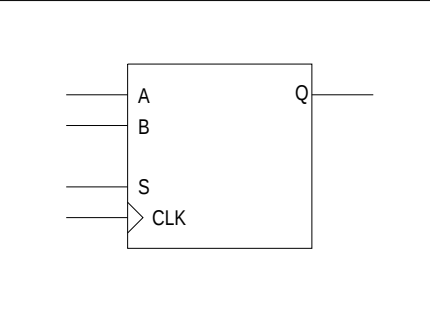
IOPCL	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Inputs
CLK, D, E, IOPCL

Outputs
Q

- NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.
NOTE 3: Uses an I/O module.

DFM



Inputs
A, B, S, CLK

Outputs
Q

Function
D-Type Flip-Flop with 2-input Multiplexed Data

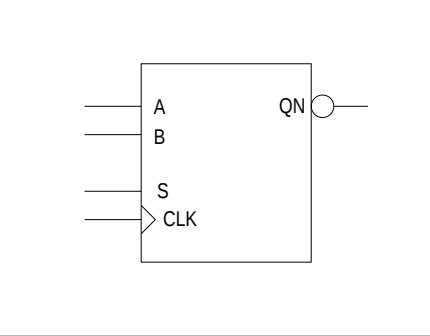
Truth Table

S	CLK	Q_{n+1}
0	↑	A
1	↑	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFM1B



Inputs
A, B, S, CLK

Outputs
QN

Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

S	CLK	QN_{n+1}
0	↑	!A
1	↑	!B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

ACT 1

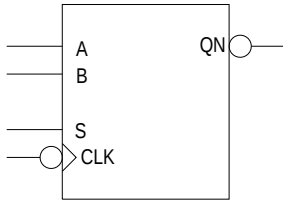
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

DFM1C**Function**

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

S	CLK	Q_{n+1}
0	↓	!A
1	↓	!B

Inputs

A, B, S, CLK

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

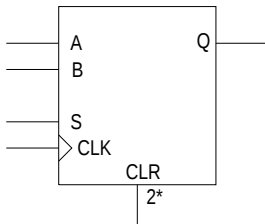
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

DFM3**Function**

D-Type Flip-Flop with 2-input Multiplexed Data, and active high Clear

Truth Table

CLR	S	CLK	Q_{n+1}
0	0	↑	A
0	1	↑	B

Inputs

A, B, CLR, S, CLK

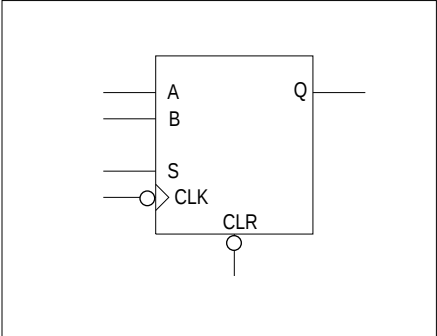
Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX.

DFM3B



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear and Clock

Truth Table

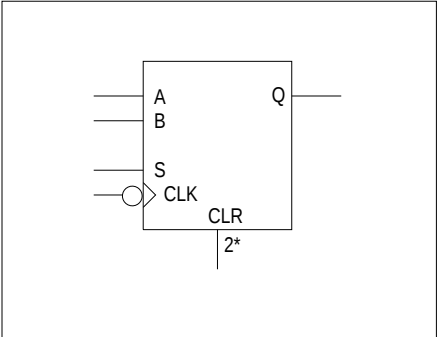
CLR	S	CLK	Q _{n+1}
0	X	X	0
1	0	↓	A
1	1	↓	B

Inputs A, B, CLR, S, CLK	Outputs Q
------------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFM3E



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock

Truth Table

CLR	S	CLK	Q _{n+1}
1	X	X	0
0	0	↓	A
0	1	↓	B

Inputs A, B, CLR, S, CLK	Outputs Q
------------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

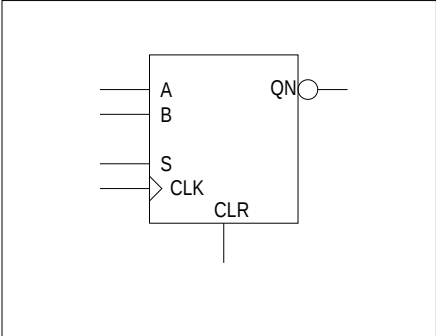
- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX.

ACT 1

40MX

DFM3F



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Output

Truth Table

CLR	S	CLK	Q _N _{n+1}
1	X	X	1
0	0	↑	!A
0	1	↑	!B

Inputs
A, B, CLR, S, CLK

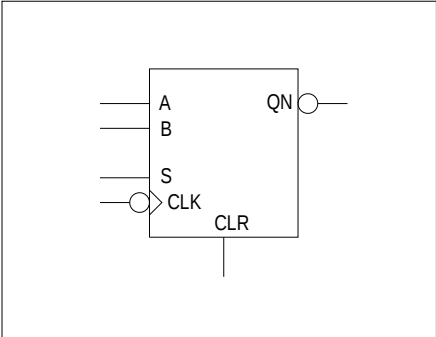
Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

DFM3G



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock and Output

Truth Table

CLR	S	CLK	Q _N _{n+1}
1	X	X	1
0	0	↓	!A
0	1	↓	!B

Inputs
A, B, CLR, S, CLK

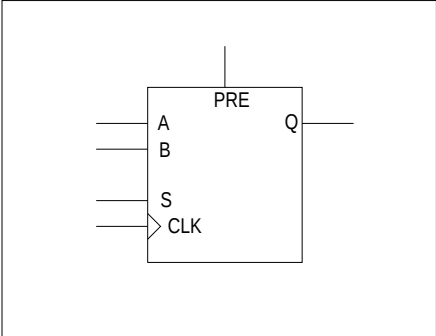
Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

DFM4



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active high Preset

Truth Table

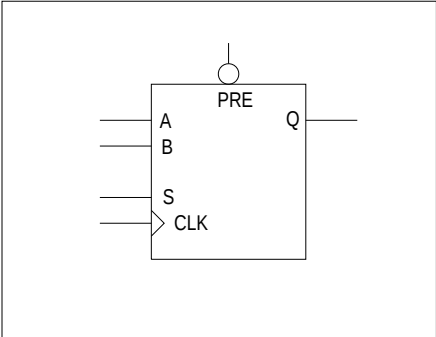
PRE	S	CLK	Q _{n+1}
1	X	X	1
0	0	↑	A
0	1	↑	B

Inputs
A, B, PRE, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM4A



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset

Truth Table

PRE	S	CLK	Q _{n+1}
0	X	X	1
1	0	↑	A
1	1	↑	B

Inputs
A, B, PRE, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

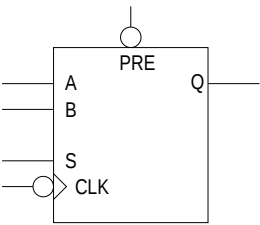
ACT 1

40MX

ACT 1

40MX

DFM4B



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Clock

Truth Table

PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	↓	A
1	1	↓	B

Inputs

A, B, PRE, S, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

ACT 2/1200XL

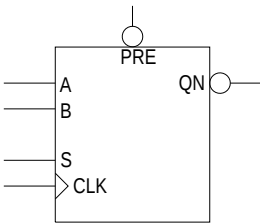
ACT 3

3200DX

40MX

42MX

DFM4C



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Output

Truth Table

PRE	S	CLK	QN_{n+1}
0	X	X	0
1	0	↑	!A
1	1	↑	!B

Inputs

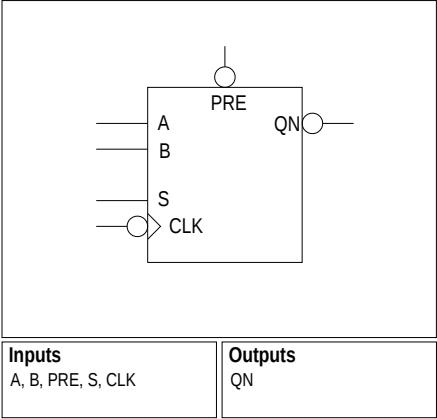
A, B, PRE, S, CLK

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM4D



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset, Clock and Output

Truth Table

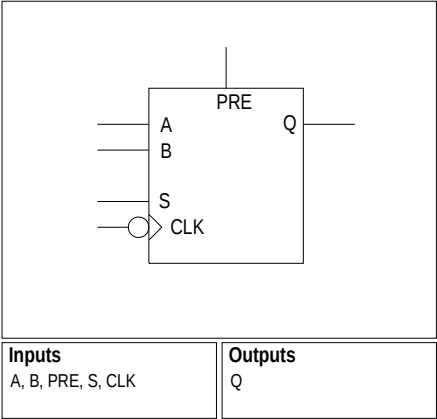
PRE	S	CLK	QN _{n+1}
0	X	X	0
1	0	↓	!A
1	1	↓	!B

Inputs	Outputs
A, B, PRE, S, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFM4E



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clock

Truth Table

PRE	S	CLK	Q _{n+1}
1	X	X	1
0	0	↓	A
0	1	↓	B

Inputs	Outputs
A, B, PRE, S, CLK	Q

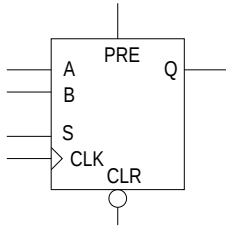
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

- ACT 1
- 40MX

ACT 1

40MX

DFM5A

**Function**

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear

Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	$\uparrow$	A
1	0	1	$\uparrow$	B
0	1	X	X	*

Inputs

A, B, CLR, PRE, S, CLK

Outputs

Q

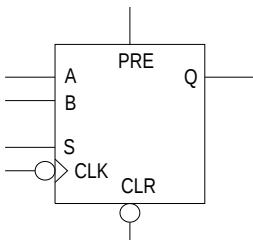
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

ACT 1

40MX

DFM5B

**Function**

D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	$\downarrow$	A
1	0	1	$\downarrow$	B
0	1	X	X	*

Inputs

A, B, CLR, PRE, S, CLK

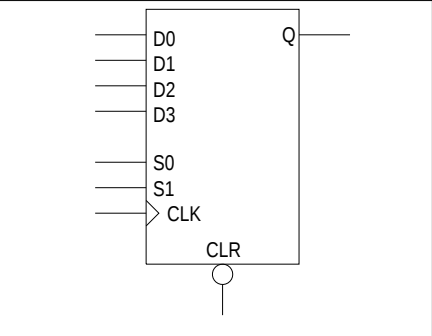
Outputs

Q

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFM6A



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

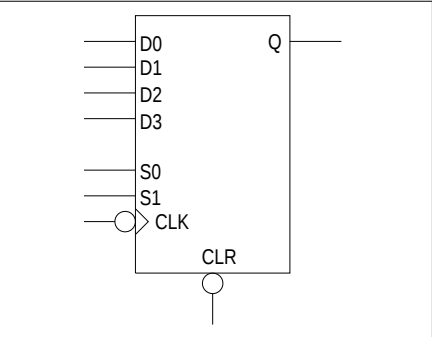
CLR	S1	S0	CLK	Q _{n+1}
0	X	X	X	0
1	0	0	↑	D0
1	0	1	↑	D1
1	1	0	↑	D2
1	1	1	↑	D3

Inputs	Outputs
D0, D1, D2, D3, S0, S1, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All	1	

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

DFM6B



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and Clock

Truth Table

CLR	S1	S0	CLK	Q _{n+1}
0	X	X	X	0
1	0	0	↓	D0
1	0	1	↓	D1
1	1	0	↓	D2
1	1	1	↓	D3

Inputs	Outputs
D0, D1, D2, D3, S0, S1, CLK, CLR	Q

Family	Modules	
	Seq	Comb
All	1	

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

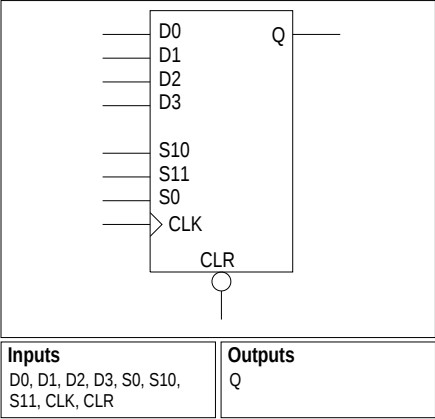
ACT 2/1200XL

ACT 3

3200DX

42MX

DFM7A



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

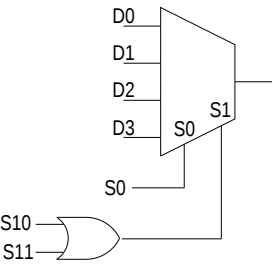
Truth Table

CLR	S11	S10	S0	CLK	Q _{n+1}
0	X	X	X	X	0
1	0	0	0	↑	D0
1	0	0	1	↑	D1
1	1	X	0	↑	D2
1	X	1	0	↑	D2
1	1	X	1	↑	D3
1	X	1	1	↑	D3

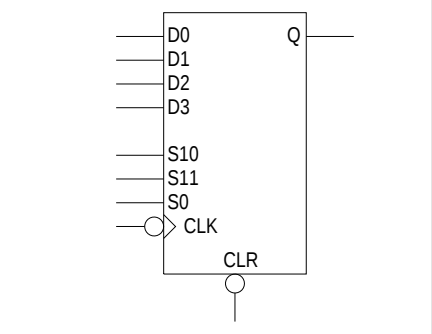
Inputs D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Outputs Q
---	---------------------

Family	Modules	
	Seq	Comb
All	1	

NOTE 1: The DFM7A macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.



DFM7B



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

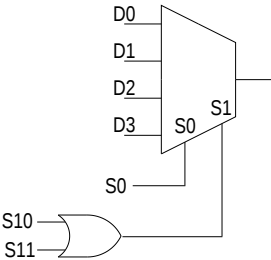
Truth Table

CLR	S11	S10	S0	CLK	Q _{n+1}
0	X	X	X	X	0
1	0	0	0	↓	D0
1	0	0	1	↓	D1
1	1	X	0	↓	D2
1	X	1	0	↓	D2
1	1	X	1	↓	D3
1	X	1	1	↓	D3

Inputs D0, D1, D2, D3, S0, S10, S11, CLK, CLR	Outputs Q
---	---------------------

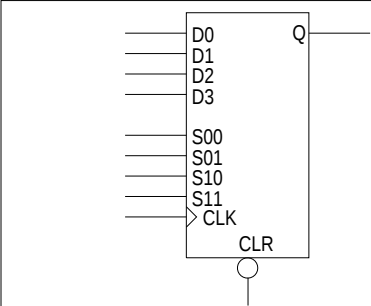
Family	Modules	
	Seq	Comb
All	1	

NOTE 1: The DFM7B macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.



- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

DFM8A



Inputs

D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

Outputs

Q

Function

D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

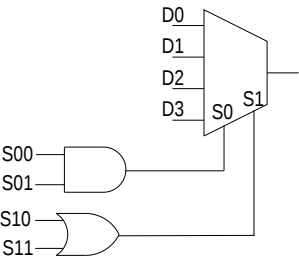
Truth Table

CLR	S11	S10	S01	S00	CLK	Q _{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↑	D0
1	0	0	X	0	↑	D0
1	0	0	1	1	↑	D1
1	1	X	0	X	↑	D2
1	X	1	0	X	↑	D2
1	1	X	X	0	↑	D2
1	X	1	X	0	↑	D2
1	1	X	1	1	↑	D3
1	X	1	1	1	↑	D3

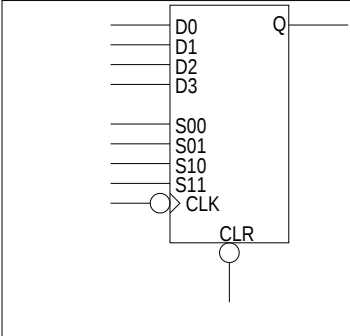
Family	Modules	
	Seq	Comb
ACT 3	1	

NOTE 1: The DFM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8B



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

Truth Table						
CLR	S11	S10	S01	S00	CLK	Q _{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↓	D0
1	0	0	X	0	↓	D0
1	0	0	1	1	↓	D1
1	1	X	0	X	↓	D2
1	X	1	0	X	↓	D2
1	1	X	X	0	↓	D2
1	X	1	X	0	↓	D2
1	1	X	1	1	↓	D3
1	X	1	1	1	↓	D3

Inputs

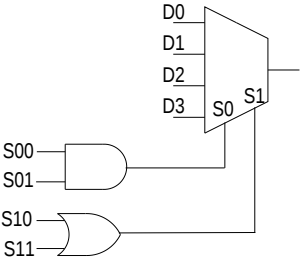
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 3	1	

NOTE 1:DFM8B macro represents the full ACT 3 S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.



ACT 3

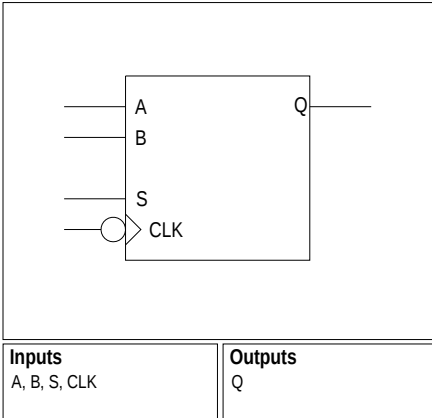
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

DFMA**Function**

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

S	CLK	Q_{n+1}
0	↓	A
1	↓	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1

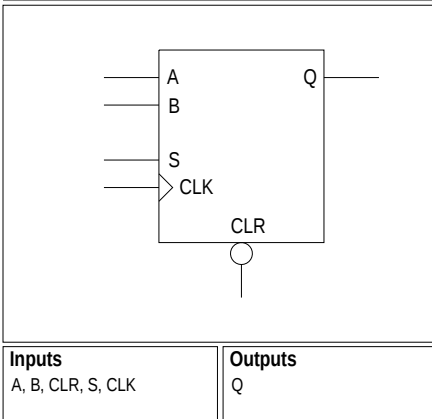
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

DFMB**Function**

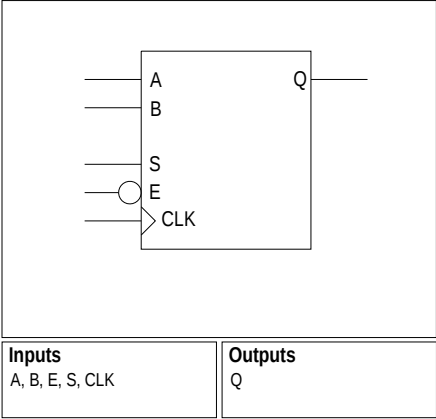
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear

Truth Table

CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↑	A
1	1	↑	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFME1A



Function
2-bit D-Type Flip-Flop with Multiplexed Data, and active low Enable

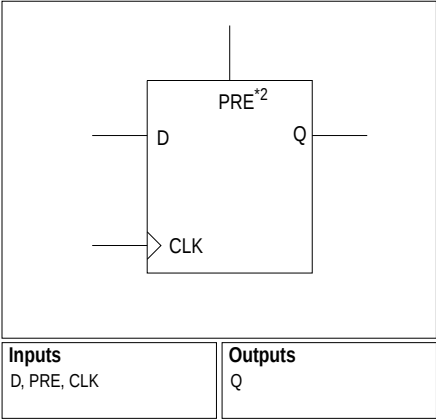
Truth Table

E	S	CLK	Q _{n+1}
1	X	X	Q
0	0	↑	A
0	1	↑	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFP1



Function
D-Type Flip-Flop with active high Preset

Truth Table

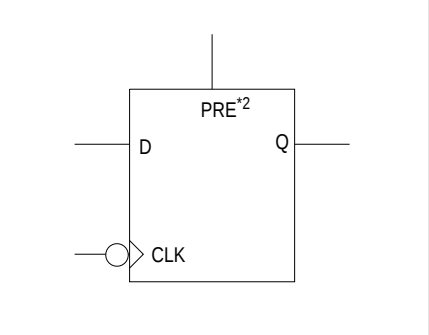
PRE	CLK	Q _{n+1}
1	X	1
0	↑	D

Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

* A 2 on the symbol implies 2 logic module delays only for 54SX.

DFP1A



Function
D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

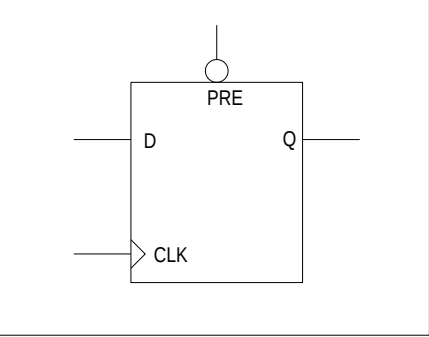
PRE	CLK	Q _{n+1}
1	X	1
0	↓	D

Inputs D, PRE, CLK	Outputs Q
------------------------------	---------------------

Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX.

DFP1B



Function
D-Type Flip-Flop with active low Preset

Truth Table

PRE	CLK	Q _{n+1}
0	X	1
1	↑	D

Inputs D, PRE, CLK	Outputs Q
------------------------------	---------------------

Family	Modules	
	Seq	Comb
54SX	1	
Others		2

DFP1C

Function

D-Type Flip-Flop with active high Preset, and active low Output

Truth Table

PRE	CLK	Q _{n+1}
1	X	0
0	↑	!D

Inputs

D, PRE, CLK

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT 1 and 40MX.

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DFP1D

Function

D-Type Flip-Flop with active low Preset and Clock

Truth Table

PRE	CLK	Q _{n+1}
0	X	1
1	↓	D

Inputs

D, PRE, CLK

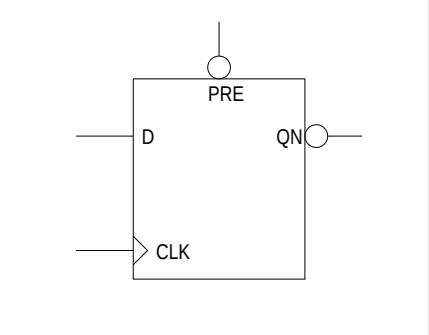
Outputs

Q

Family	Modules	
	Seq	Comb
54SX	1	
Others		2

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

DFP1E



Function
D-Type Flip-Flop with active low Preset and Output

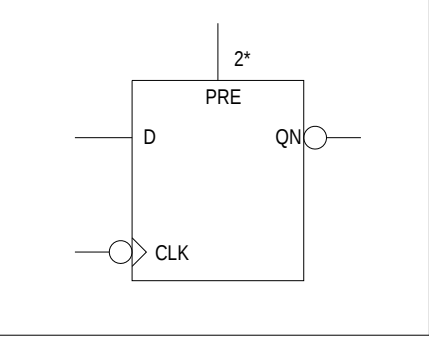
Truth Table

PRE	CLK	Q _N _{n+1}
0	X	0
1	↑	!D

Inputs D, PRE, CLK	Outputs QN
------------------------------	----------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFP1F



Function
D-Type Flip-Flop with active high Preset, and active low Clock and Output

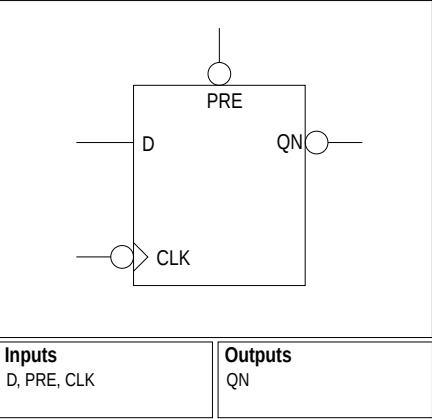
Truth Table

PRE	CLK	Q _N _{n+1}
1	X	0
0	↓	!D

Inputs D, PRE, CLK	Outputs QN
------------------------------	----------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

DFP1G



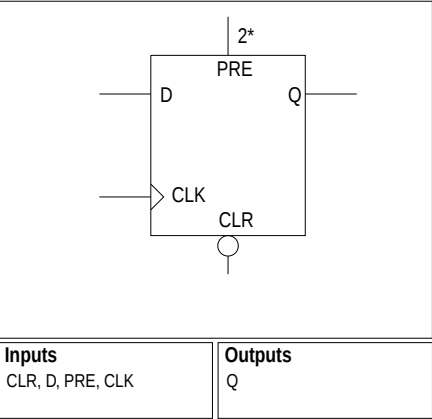
Function
D-Type Flip-Flop with active low Preset, Clock and Output

Truth Table

PRE	CLK	QN _{n+1}
0	X	0
1	↓	!D

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFPC



Function
D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	↑	D
0	1	X	**

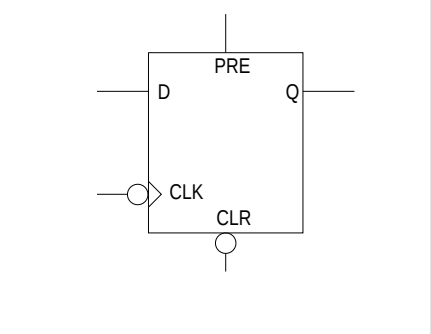
Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX.
** In ACT 1/40MX, your design should not allow both PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

DFPCA



Function
D-Type Flip-Flop with active high Preset, active low Clear, and Clock

Truth Table

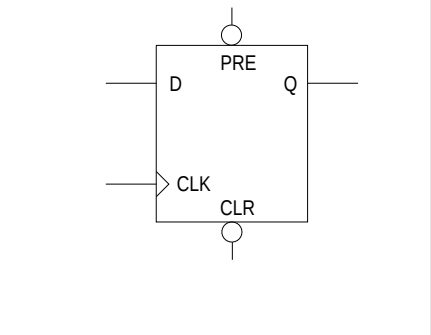
CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	*

Inputs CLR, D, PRE, CLK	Outputs Q
-----------------------------------	---------------------

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFPCB



Function
D-Type Flip-Flop, with active low Clear, and Preset

Truth Table

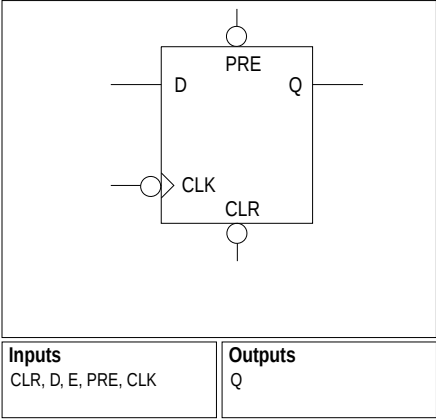
CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	0	X	1
1	1	↑	D

Inputs CLR, D, E, PRE, CLK	Outputs Q
--------------------------------------	---------------------

Family	Modules	
	Seq	Comb
54SX	1	

54SX

DFPCC



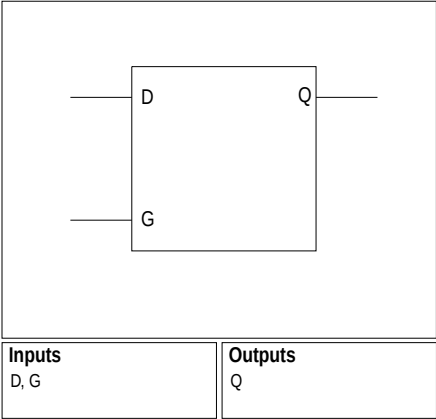
Function
D-Type Flip-Flop, with active low Preset, Clear and Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	X	X	0
1	0	X	1
1	1	↓	D

Family	Modules	
	Seq	Comb
54SX	1	

DL1



Function
Data Latch

Truth Table

G	Q _{n+1}
0	Q
1	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

ACT 1

ACT 2/1200XL

ACT 3

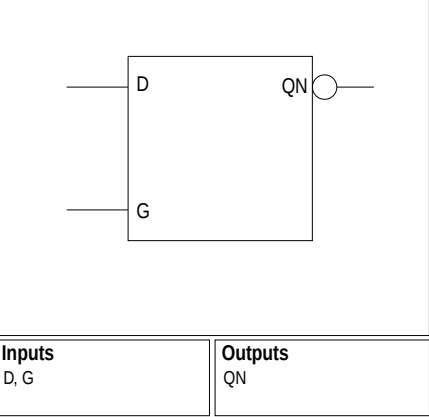
3200DX

40MX

42MX

54SX

DL1A



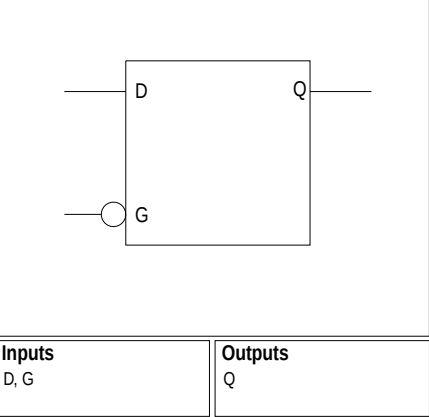
Function
Data Latch, with active low Output

Truth Table

G	QN _{n+1}
0	QN
1	!D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DL1B



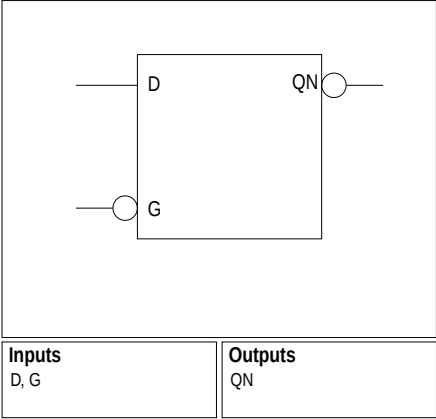
Function
Data Latch, with active low Clock

Truth Table

G	Q _{n+1}
1	Q
0	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

DL1C



Function
Data Latch, with active low Clock, and Output

G	QN _{n+1}
1	QN
0	!D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1

ACT 2/1200XL

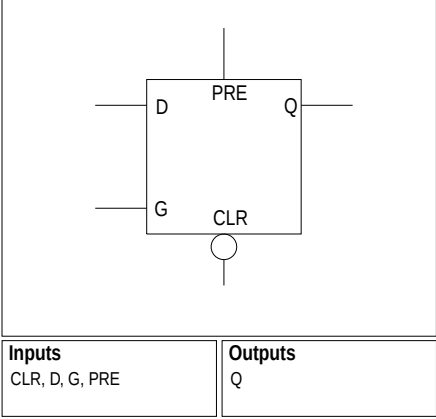
ACT 3

3200DX

40MX

42MX

DL2A



Function
Data Latch with active low Clear, and active high Preset

Truth Table			
CLR	PRE	G	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	0	Q
1	0	1	D
0	1	X	*

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

ACT 1

ACT 2/1200XL

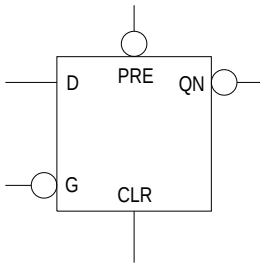
ACT 3

3200DX

40MX

42MX

DL2B

**Function**

Data Latch with active high Clear, and active low Preset, Clock and Output

CLR	PRE	G	Q_{n+1}
1	1	X	1
0	0	X	0
0	1	1	QN
0	1	0	!D
1	0	X	*

Inputs

CLR, D, G, PRE

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

ACT 1

ACT 2/1200XL

ACT 3

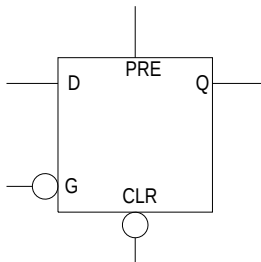
3200DX

40MX

42MX

54SX

DL2C

**Function**

Data Latch with active low Clear, active high Preset, and active low Clock

Truth Table

CLR	PRE	G	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	1	Q
1	0	0	D
0	1	X	*

Inputs

CLR, D, G, PRE

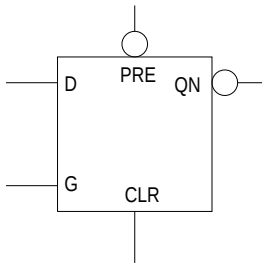
Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DL2D

**Function**

Data Latch with active high Clear, and active low Preset, and Output

Truth Table

CLR	PRE	G	QN _{n+1}
1	1	X	1
0	0	X	0
0	1	0	QN
0	1	1	!D
1	0	X	*

Inputs

CLR, D, G, PRE

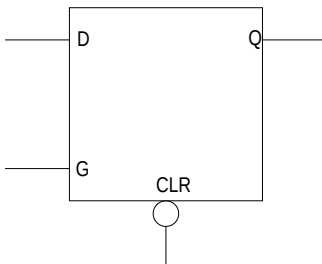
Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DLC

**Function**

Data Latch with active low Clear

Truth Table

CLR	G	Q _{n+1}
0	X	0
1	0	Q
1	1	D

Inputs

CLR, D, G

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

ACT 1

ACT 2/1200XL

ACT 3

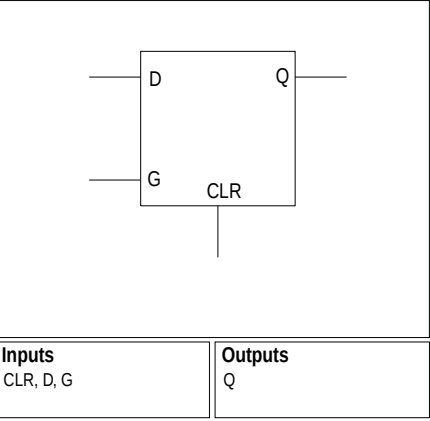
3200DX

40MX

42MX

54SX

DLC1



Function
Data Latch with active high Clear

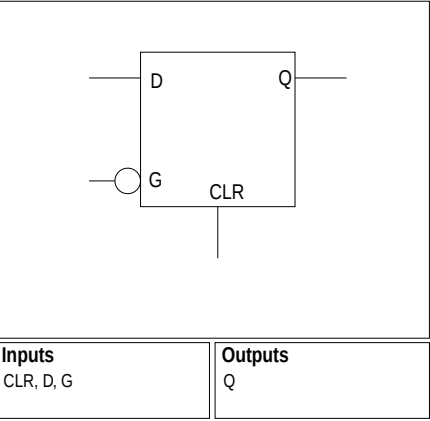
Truth Table

CLR	G	Q_{n+1}
1	X	0
0	0	Q
0	1	D

Inputs CLR, D, G	Outputs Q
----------------------------	---------------------

Family	Modules	
	Seq	Comb
All		1

DLC1A



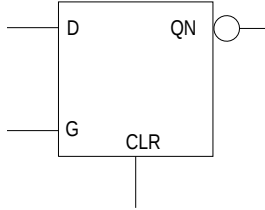
Function
Data Latch with active high Clear, and active low Clock

Truth Table

CLR	G	Q_{n+1}
1	X	0
0	1	Q
0	0	D

Inputs CLR, D, G	Outputs Q
----------------------------	---------------------

Family	Modules	
	Seq	Comb
All		1

DLC1F**Function**

Data Latch with active high Clear, and active low Output

Truth Table

CLR	G	QN_{n+1}
1	X	1
0	0	QN
0	1	!D

Inputs

CLR, D, G

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

ACT 1

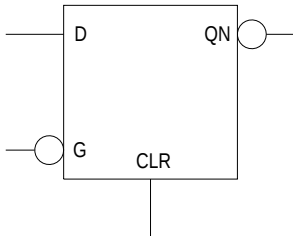
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

DLC1G**Function**

Data Latch with active high Clear, and active low Clock and Output

Truth Table

CLR	G	QN_{n+1}
1	X	1
0	1	QN
0	0	!D

Inputs

CLR, D, G

Outputs

QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

ACT 1

ACT 2/1200XL

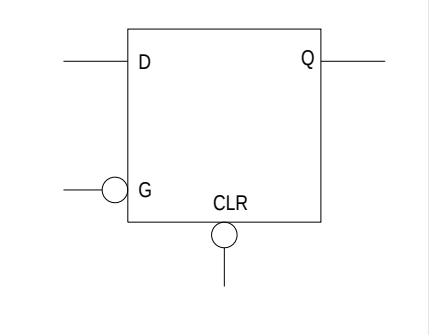
ACT 3

3200DX

40MX

42MX

DLCA



Function
Data Latch with active low Clear and Clock

Truth Table

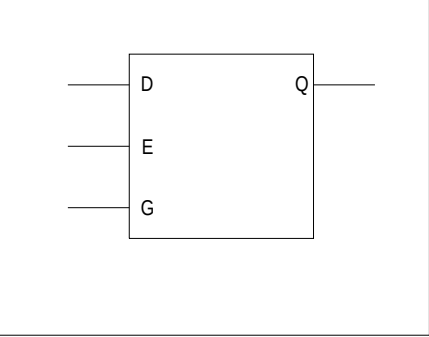
CLR	G	Q_{n+1}
0	X	0
1	1	Q
1	0	D

Inputs
CLR, D, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

DLE



Function
Data Latch with active high Enable

Truth Table

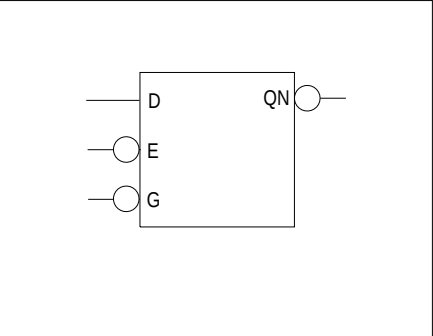
E	G	Q_{n+1}
0	X	Q
X	0	Q
1	1	D

Inputs
D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLE1D



Function
Data Latch with active low Enable and Clock, and active low Output

Truth Table

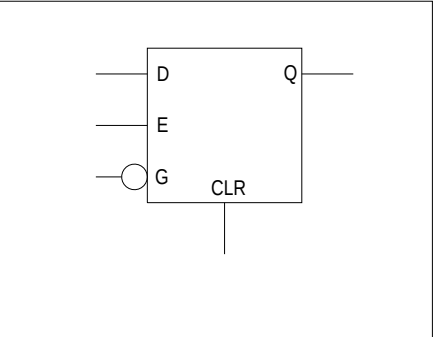
E	G	Q _{n+1}
1	X	QN
X	1	QN
0	0	!D

Inputs D, E, G	Outputs QN
--------------------------	----------------------

Family	Modules	
	Seq	Comb
ACT 1/40fMX		1
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DLE2A



Function
Data Latch with active high Enable and Clear, and active low Clock

Truth Table

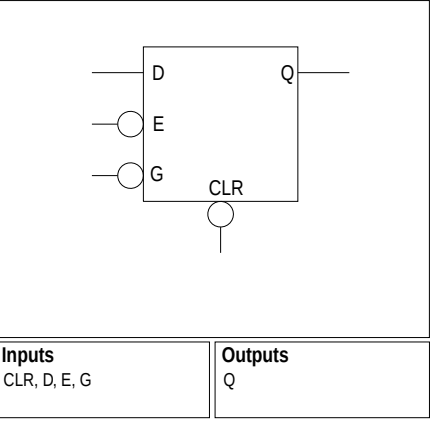
CLR	E	G	Q _{n+1}
1	X	X	0
0	0	X	Q
0	X	1	Q
0	1	0	D

Inputs CLR, D, E, G	Outputs Q
-------------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

- ACT 1
- 40MX

DLE2B



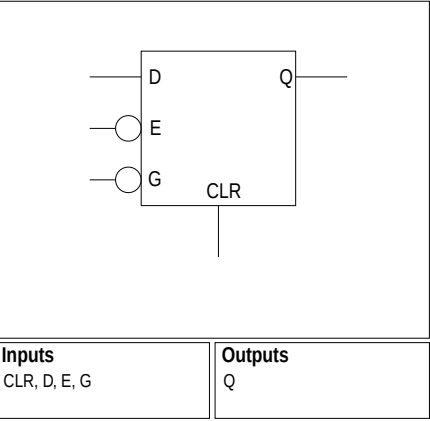
Function
Data Latch with active low Enable, Clear and Clock

Truth Table

CLR	E	G	Q_{n+1}
0	X	X	0
1	1	X	Q
1	X	1	Q
1	0	0	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLE2C



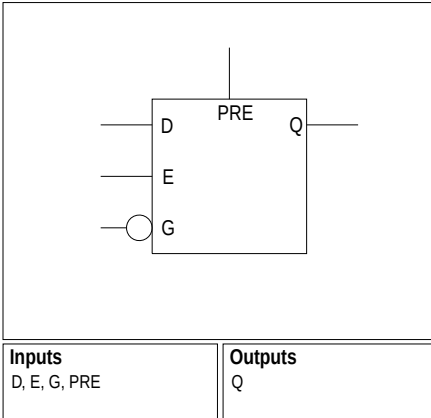
Function
Data Latch with active low Enable and Clock, and active high Clear

Truth Table

CLR	E	G	Q_{n+1}
1	X	X	0
0	1	X	Q
0	X	1	Q
0	0	0	D

Family	Modules	
	Seq	Comb
All		1

DLE3A



Function

Data Latch with active high Enable and Preset, and active low Clock

Truth Table

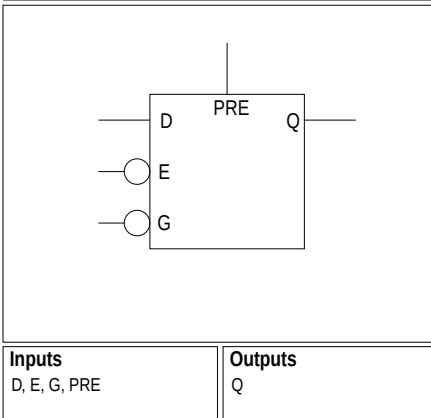
PRE	E	G	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	0	D
0	X	1	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

ACT 1

40MX

DLE3B



Function

Data Latch with active low Enable and Clock, and active low Preset

Truth Table

PRE	E	G	Q_{n+1}
1	X	X	1
0	1	X	Q
0	X	1	Q
0	0	0	D

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

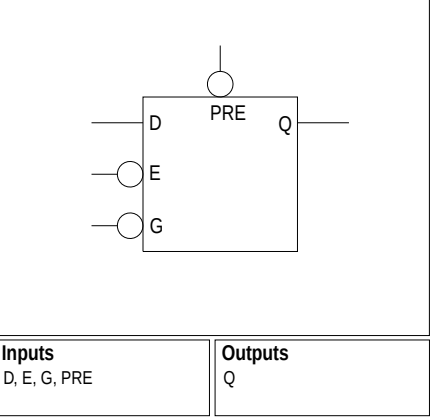
3200DX

40MX

42MX

54SX

DLE3C



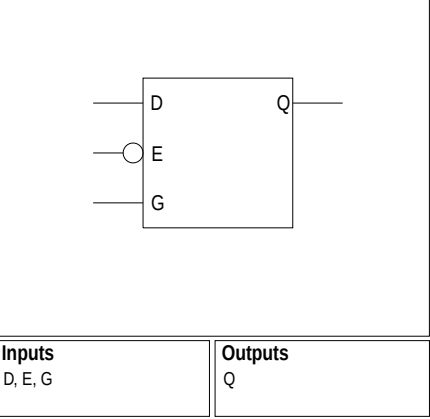
Function
Data Latch with active low Enable, Preset and Clock

Truth Table

PRE	E	G	Q_{n+1}
0	X	X	1
1	1	X	Q
1	X	1	Q
1	0	0	D

Family	Modules	
	Seq	Comb
All		1

DLEA



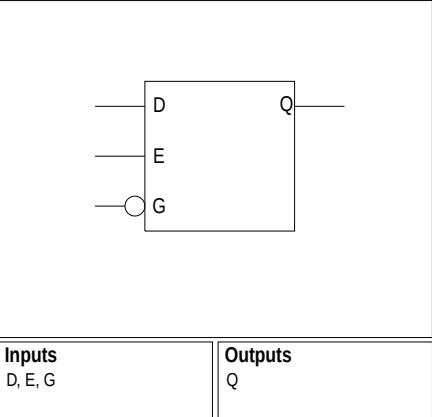
Function
Data Latch with active low Enable, and active high Clock

Truth Table

E	G	Q_{n+1}
1	X	Q
X	0	Q
0	1	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLEB



Function
Data Latch with active high Enable, and active high Clock

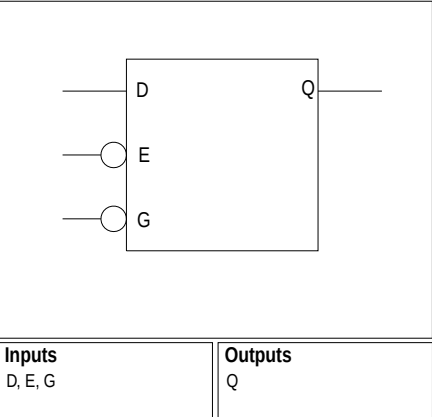
Truth Table

E	G	Q _{n+1}
0	X	Q
X	1	Q
1	0	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

DLEC



Function
Data Latch with active low Enable, and Clock

Truth Table

E	G	Q _{n+1}
1	X	Q
X	1	Q
0	0	D

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX

ACT 1

DLM

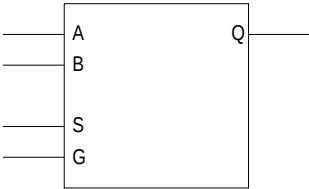
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX



Function
Data Latch with 2-input Multiplexed Data

Truth Table

S	G	Q _{n+1}
X	0	Q
0	1	A
1	1	B

Inputs

A, B, G, S

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

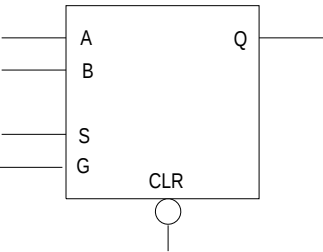
ACT 2/1200XL

DLM2

ACT 3

3200DX

42MX



Function
Data Latch with 2-input Multiplexed Data and Active-Low Clear

Truth Table

CLR	S	G	Q _{n+1}
0	X	X	0
1	X	0	Q
1	0	1	A
1	1	1	B

Inputs

A, B, CLR, G, S

Outputs

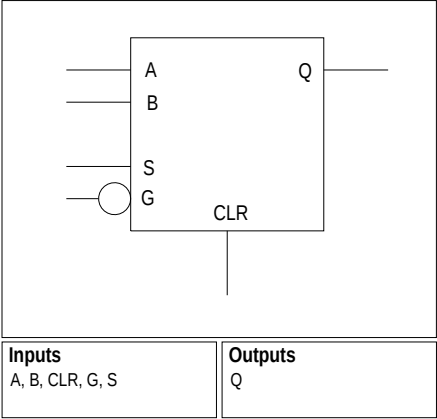
Q

Family	Modules	
	Seq	Comb
All	1	

ACT 1

40MX

DLM2A



Function
Data Latch with 2-input Multiplexed Data and Clear, and Active-Low Clock

Truth Table

CLR	S	G	Q _{n+1}
1	X	X	0
0	X	1	Q
0	0	0	A
0	1	0	B

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

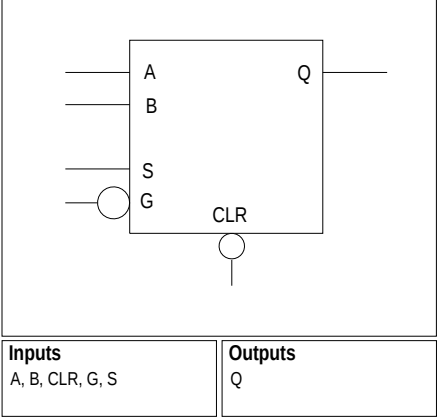
ACT 2/1200XL

ACT 3

3200DX

42MX

DLM2B



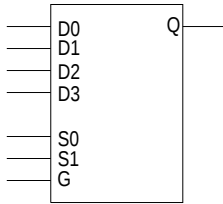
Function
Data Latch with 2-input Multiplexed Data and Active-Low Clock and Clear

Truth Table

CLR	S	G	Q _{n+1}
0	X	X	0
1	X	1	Q
1	0	0	A
1	1	0	B

Family	Modules	
	Seq	Comb
All	1	

DLM3



Function

Data Latch with 4-input Multiplexed Data

Truth Table

S1	S0	G	Q _{n+1}
X	X	0	Q
0	0	1	D0
0	1	1	D1
1	0	1	D2
1	1	1	D3

Inputs

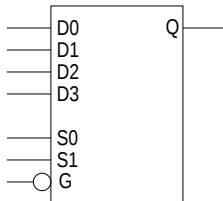
D0, D1, D2, D3, S0, S1, G

Outputs

Q

Family	Modules	
	Seq	Comb
All	1	

DLM3A

**Function**

Data Latch with 4-input Multiplexed Data, and active low Clock

Truth Table

S1	S0	G	Q _{n+1}
X	X	1	Q
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3

Inputs

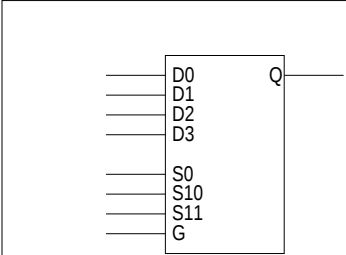
D0, D1, D2, D3, S0, S1, G

Outputs

Q

Family	Modules	
	Seq	Comb
All	1	

DLM4



Function
Data Latch with 4-input Multiplexed Data

Truth Table

S10	S11	S0	G	Q _{n+1}
X	X	X	0	Q
0	0	0	1	D0
0	0	1	1	D1
X	1	0	1	D2
1	X	0	1	D2
X	1	1	1	D3
1	X	1	1	D3

Inputs
D0, D1, D2, D3, D0, S0,
S10, S11, G

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

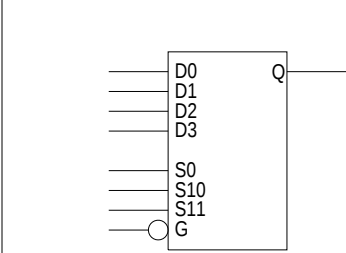
ACT 2/1200XL

ACT 3

3200DX

42MX

DLM4A



Function
Data Latch with 4-input Multiplexed Data

Truth Table

S10	S11	S0	G	Q _{n+1}
X	X	X	1	Q
0	0	0	0	D0
0	0	1	0	D1
X	1	0	0	D2
1	X	0	0	D2
X	1	1	0	D3
1	X	1	0	D3

Inputs
D0, D1, D2, D3, D0, S0,
S10, S11, G

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

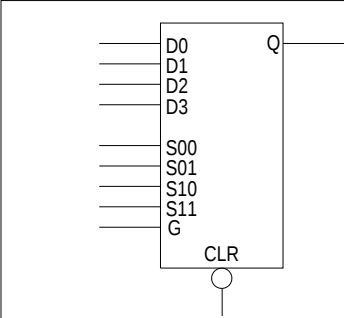
ACT 2/1200XL

ACT 3

3200DX

42MX

DLM8A



Inputs

D0, D1, D2, D3, S00, S01,
S10, S11, CLK, CLR

Outputs

Q

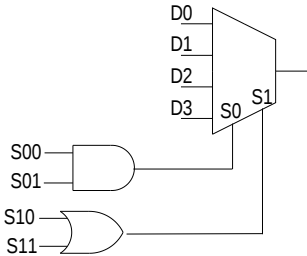
Function

D-Type Latch with 4-input Multiplexed Data and active low Clear

Truth Table

CLR	S11	S10	S01	S00	G	Q _{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	0	Q
1	0	0	0	X	1	D0
1	0	0	X	0	1	D0
1	0	0	1	1	1	D1
1	1	X	0	X	1	D2
1	X	1	0	X	1	D2
1	1	X	X	0	1	D2
1	X	1	X	0	1	D2
1	1	X	1	1	1	D3
1	X	1	1	1	1	D3

Family	Modules	
	Seq	Comb
ACT 3	1	



NOTE 1: The DLM8A macro represents the full ACT 3 S-Module.

NOTE 2: The following schematic describes the interconnections of the select lines.

DLM8B

D0

D1

D2

D3

S00

S01

S10

S11

G

Q

CLR

Inputs

D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

Outputs

Q

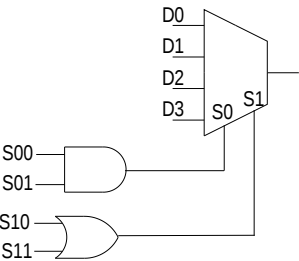
Function

D-Type Latch with 4-input Multiplexed Data and active low Clear

Truth Table

CLR	S11	S10	S01	S00	G	Q _{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	1	Q
1	0	0	0	X	0	D0
1	0	0	X	0	0	D0
1	0	0	1	1	0	D1
1	1	X	0	X	0	D2
1	X	1	0	X	0	D2
1	1	X	X	0	0	D2
1	X	1	X	0	0	D2
1	1	X	1	1	0	D3
1	X	1	1	1	0	D3

Family	Modules	
	Seq	Comb
ACT 3	1	



NOTE 1: The DLM8B macro represents the full ACT 3 S-module.

NOTE 2: The following schematic describes the interconnections of the select lines.

ACT 1

DLMA

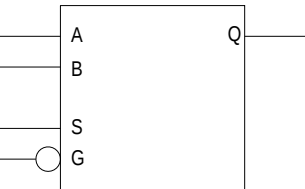
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX



Function
Data Latch with 2-input Multiplexed Data, and active low Clock

Truth Table

S	G	Q _{n+1}
X	1	Q
0	0	A
1	0	B

Inputs

A, B, G, S

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1

DLME1A

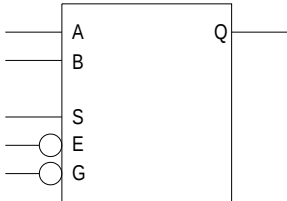
ACT 2/1200XL

ACT 3

3200DX

40MX

42MX



Function
2-bit Data Latch with Multiplexed Data and Enable, and active low Clock

Truth Table

E	S	G	Q _{n+1}
1	X	X	Q
X	X	1	Q
0	0	0	A
0	1	0	B

Inputs

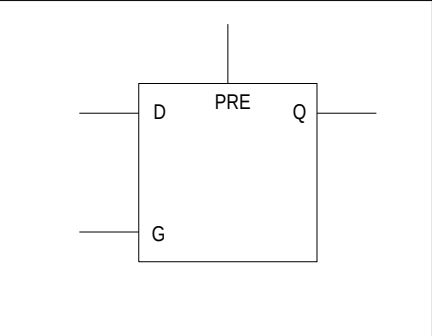
A, B, E, G, S

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLP1



Function
Data Latch with active high Preset, and Clock

Truth Table

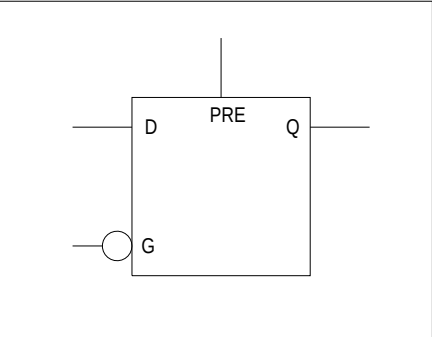
PRE	G	Q _{n+1}
1	X	1
0	0	Q
0	1	D

Inputs	Outputs
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

DLP1A



Function
Data Latch with active high Preset, and active low Clock

Truth Table

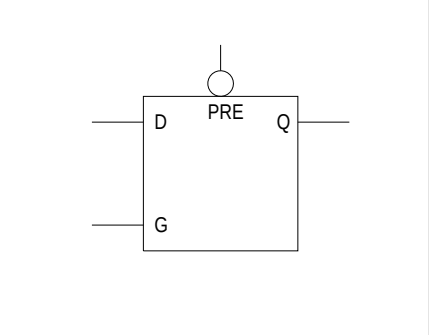
PRE	G	Q _{n+1}
1	X	1
0	1	Q
0	0	D

Inputs	Outputs
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

DLP1B



Function
Data Latch with active low Preset, and active high Clock

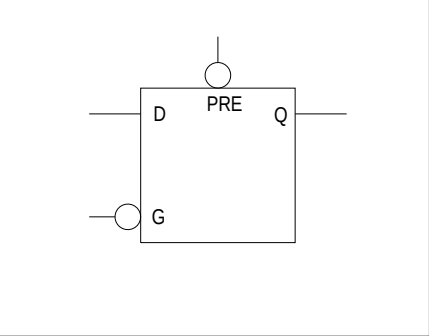
Truth Table

PRE	G	Q_{n+1}
0	X	1
1	0	Q
1	1	D

Inputs	Outputs
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLP1C



Function
Data Latch with active low Preset and Clock

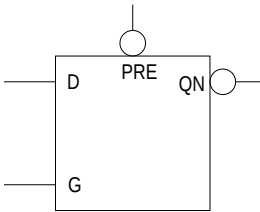
Truth Table

PRE	G	Q_{n+1}
0	X	1
1	1	Q
1	0	D

Inputs	Outputs
D, G, PRE	Q

Family	Modules	
	Seq	Comb
All		1

DLP1D



Function
Data Latch with active low Preset and Output, and active high Clock

Truth Table

PRE	G	Q _{n+1}
0	X	0
1	0	Q _N
1	1	!D

Inputs	Outputs
D, G, PRE	Q _N

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1

ACT 2/1200XL

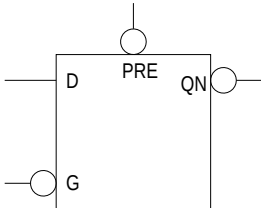
ACT 3

3200DX

40MX

42MX

DLP1E



Function
Data Latch with active low Preset, Clock and Output

Truth Table

PRE	G	Q _{n+1}
0	X	0
1	0	!D
1	1	Q _N

Inputs	Outputs
D, G, PRE	Q _N

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1

ACT 2/1200XL

ACT 3

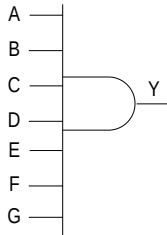
3200DX

40MX

42MX

3200DX

42MX

DXAND7

Function
Seven-input AND Gate

Truth Table

A through G	Y
All inputs = 1	1
Any input = 0	0

Inputs

A, B, C, D, E, F, G

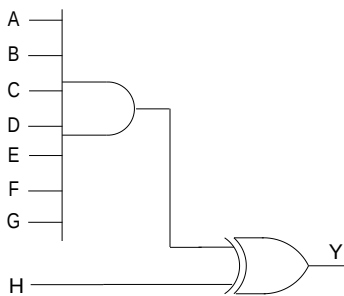
Outputs

Y

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

3200DX

42MX

DXAX7

Function
Eight-input AND/Exclusive-OR Gate

Truth Table

A through G	H	Y
Any input = 0	0	0
Any input = 0	1	1
All inputs = 1	0	1
All inputs = 1	1	0

Inputs

A, B, C, D, E, F, G, H

Outputs

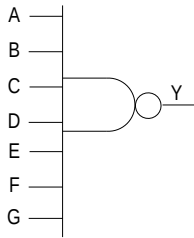
Y

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

DXNAND7

3200DX

42MX



Function
Seven-input NAND Gate

Truth Table

A through G	Y
All inputs = 1	0
Any input = 0	1

Inputs

A, B, C, D, E, F, G

Outputs

Y

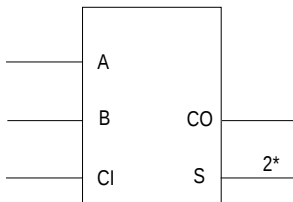
Family	Modules	
	Seq	DX
3200DX/42MX		1

FA1

ACT 1

40MX

54SX



Function
1 bit adder with active high I/Os

Truth Table

A	B	CI	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Inputs

A, B, CI

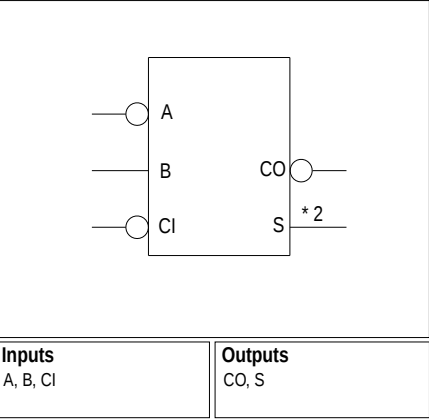
Outputs

CO, S

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		3
54SX		2

* A 2 on the symbol implies 2 logic module delays only in ACT 1 and 40MX.

FA1A



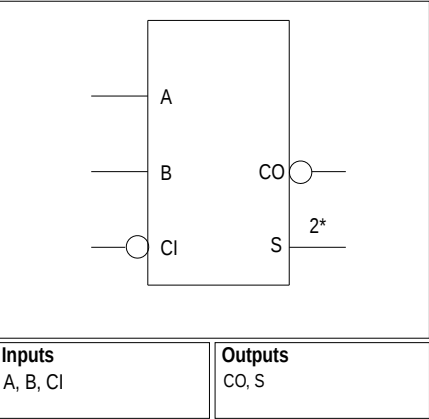
Function
1-bit Adder, with active low Carry In and Carry Out, and active low A-Input

Truth Table				
A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX.

FA1B



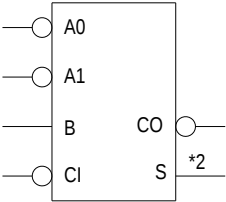
Function
1-bit Adder, with active low Carry In and Carry Out

Truth Table				
A	B	CI	CO	S
0	0	0	1	1
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX.

FA2A



Function
1-bit Adder, with active low Carry In and Carry Out, and active low A0 and A1 Inputs, used in multipliers

Inputs	Outputs
A0, A1, B, CI	CO, S

A0	A1	B	CI	CO	S
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	1	1

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families.

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 1

ACT 2/1200XL

ACT 3

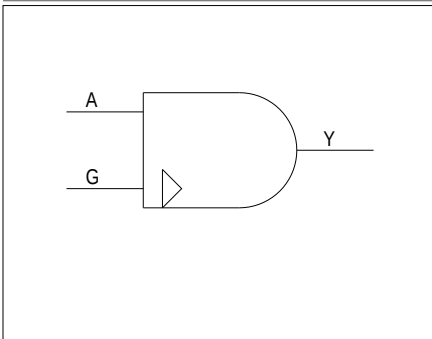
3200DX

40MX

42MX

54SX

GAND2



Function
2-Input AND Clock Net

Truth Table

A	G	Y
X	0	0
0	X	0
1	1	1

Inputs

A, G

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

ACT 1

ACT 2/1200XL

ACT 3

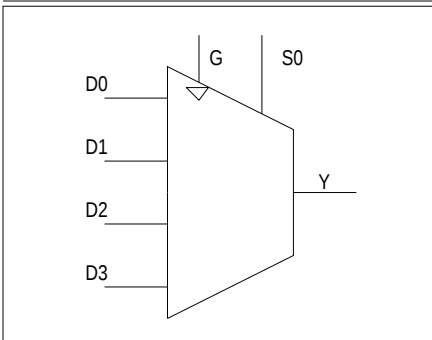
3200DX

40MX

42MX

54SX

GMX4



Function
4-to-1 Mux Clock Net

Truth Table

G	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Inputs

D0, D1, D2, D3, S0, G

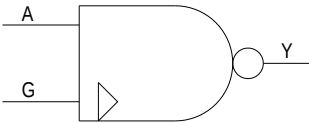
Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GNAND2



Function

2-Input NAND Clock Net

Truth Table

A	G	Y
X	0	1
0	X	1
1	1	0

Inputs

A, G

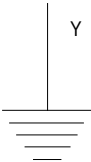
Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GND



Function

Ground

Inputs

Outputs

Y

NOTE: GND does not use any modules.

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

GNOR2

ACT 1

ACT 2/1200XL

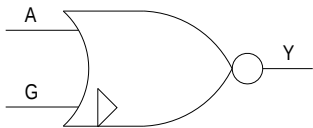
ACT 3

3200DX

40MX

42MX

54SX



Function

2-Input NOR Clock Net

Truth Table

A	G	Y
0	0	1
X	1	0
1	X	0

Inputs

A, G

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GOR2

ACT 1

ACT 2/1200XL

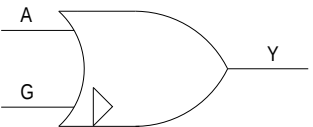
ACT 3

3200DX

40MX

42MX

54SX



Function

2-Input OR Clock Net

Truth Table

A	G	Y
0	0	0
X	1	1
1	X	1

Inputs

A, G

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

HA1

Function
Half-Adder

Truth Table

A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Inputs
A, B

Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

HA1A

Function
Half-Adder with active low A-Input

Truth Table

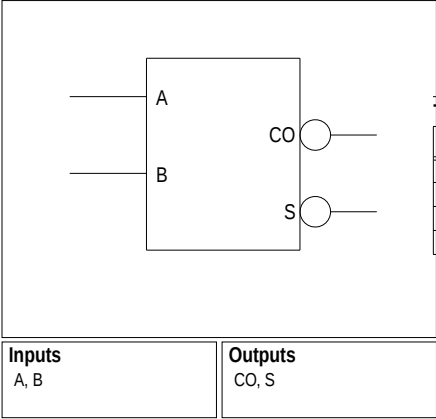
A	B	CO	S
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	1

Inputs
A, B

Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

HA1B



Function
Half-Adder with active low Carry Out and Sum

Truth Table

A	B	CO	S
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

Family	Modules	
	Seq	Comb
All		2

ACT 1

ACT 2/1200XL

ACT 3

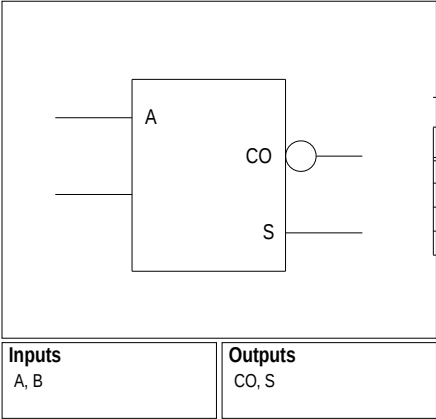
3200DX

40MX

42MX

54SX

HA1C



Function
Half-Adder with active low Carry Out

A	B	CO	S
0	0	1	0
0	1	1	1
1	0	1	1
1	1	0	0

Family	Modules	
	Seq	Comb
All		2

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 1

ACT 2/1200XL

ACT 3

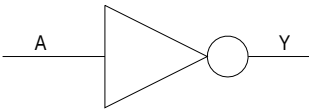
3200DX

40MX

42MX

54SX

INV



Function

Inverter with active low Output

Truth Table

A	Y
0	1
1	0

Inputs

A

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

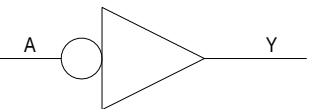
3200DX

40MX

42MX

54SX

INVA



Function

Inverter with active low Input

Truth Table

A	Y
0	1
1	0

Inputs

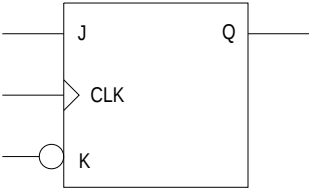
A

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

JKF



Inputs

J, K, CLK

Outputs

Q

Function

JK Flip-Flop with active low K-Input

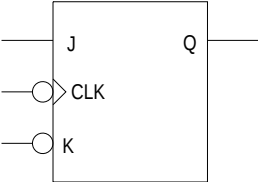
Truth Table

J	K	CLK	Q _{n+1}
0	0	↑	0
0	1	↑	Q
1	0	↑	!Q
1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

JKF1B



Inputs

J, K, CLK

Outputs

Q

Function

JK Flip-Flop with active low Clock and K-Input

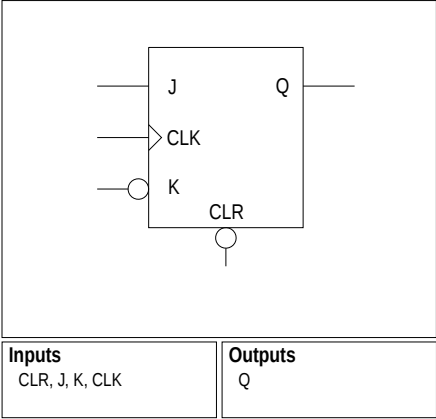
Truth Table

J	K	CLK	Q _{n+1}
0	0	↓	0
0	1	↓	Q
1	0	↓	!Q
1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

JKF2A



Function
JK Flip-Flop with active low Clear and K-Input

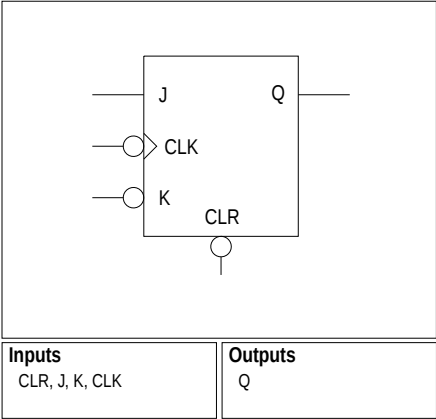
Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	$\uparrow$	0
1	0	1	$\uparrow$	Q
1	1	0	$\uparrow$	$\neg Q$
1	1	1	$\uparrow$	1

Inputs	Outputs
CLR, J, K, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

JKF2B



Function
JK Flip-Flop with active low Clear, Clock and K-Input

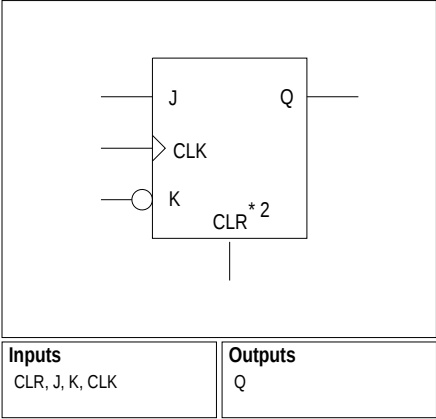
Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	$\downarrow$	0
1	0	1	$\downarrow$	Q
1	1	0	$\downarrow$	$\neg Q$
1	1	1	$\downarrow$	1

Inputs	Outputs
CLR, J, K, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

JKF2C



Function
JK Flip-Flop with active high Clear, and active low K-Input

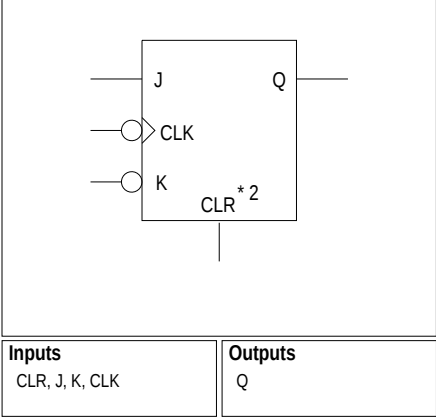
Truth Table

CLR	J	K	CLK	Q _{n+1}
1	X	X	X	0
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

JKF2D



Function
JK Flip-Flop with active high Clear, and active low Clock and K-Input

Truth Table

CLR	J	K	CLK	Q _{n+1}
1	X	X	X	0
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Family	Modules	
	Seq	Comb
ACT 1		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

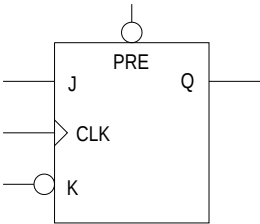
42MX

ACT 1

40MX

54SX

JKF3A



Function

JK Flip-Flop with active low Preset and K-Input

Truth Table

PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	$\uparrow$	0
1	0	1	$\uparrow$	Q
1	1	0	$\uparrow$	$\bar{Q}$
1	1	1	$\uparrow$	1

Inputs

J, K, PRE, CLK

Outputs

Q

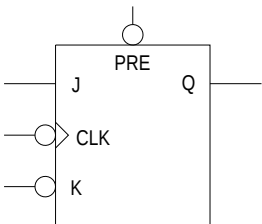
Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1

ACT 1

40MX

54SX

JKF3B



Function

JK Flip-Flop with active low Preset, Clock and K-Input

Truth Table

PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	$\downarrow$	0
1	0	1	$\downarrow$	Q
1	1	0	$\downarrow$	$\bar{Q}$
1	1	1	$\downarrow$	1

Inputs

J, K, PRE, CLK

Outputs

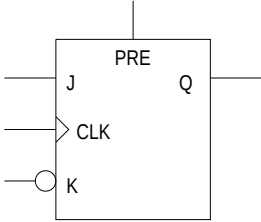
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1

ACT 1

40MX

JKF3C



Inputs

J, K, PRE, CLK

Outputs

Q

Function

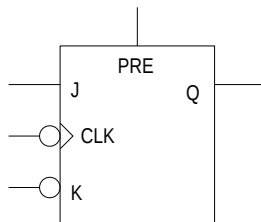
JK Flip-Flop with active high Preset, and active low K-Input

Truth Table

PRE	J	K	CLK	Q _{n+1}
1	X	X	X	1
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

JKF3D



Inputs

J, K, PRE, CLK

Outputs

Q

Function

JK Flip-Flop with active high Preset, and active low Clock and K-Inputs

Truth Table

PRE	J	K	CLK	Q _{n+1}
1	X	X	X	1
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

ACT 1

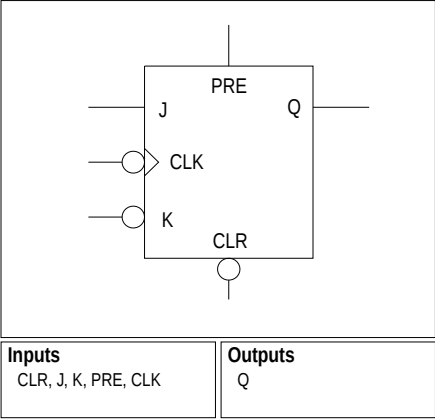
40MX

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

JKF4B



Function
JK Flip-Flop with active high Preset, active low Clear, Clock and K-Input

Truth Table

CLR	PRE	J	K	CLK	Q _{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↓	0
1	0	0	1	↓	Q
1	0	1	0	↓	!Q
1	0	1	1	↓	1
0	1	X	X	X	*

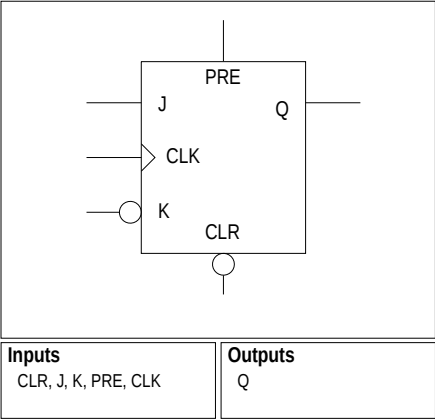
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

ACT 1

40MX

JKFPC



Function
JK Flip-Flop with active high Preset, and active low Clear and K- Input

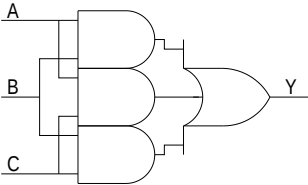
Truth Table

CLR	PRE	J	K	CLK	Q _{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↑	0
1	0	0	1	↑	Q
1	0	1	0	↑	!Q
1	0	1	1	↑	1
0	1	X	X	X	*

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

MAJ3



Inputs
A, B, C

Outputs
Y

Function
3 Input majority function

Truth TableY			
A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

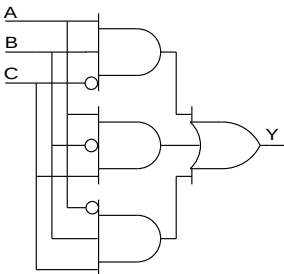
3200DX

40MX

42MX

54SX

MAJ3X



Inputs
A, B, C

Outputs
Y

Function
2 of 3 function

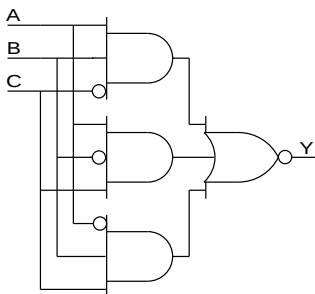
Truth TableY			
A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Family	Modules	
	Seq	Comb
54SX		1

54SX

54SX

MAJ3XI

**Function**

2 of 3 function with active low output

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Inputs

A, B, C

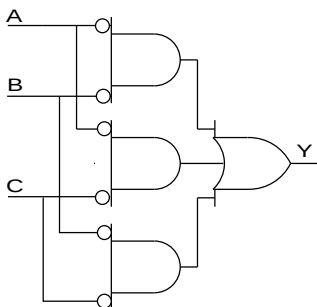
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

MIN3

**Function**

3 input minority function

Truth Table

A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

Inputs

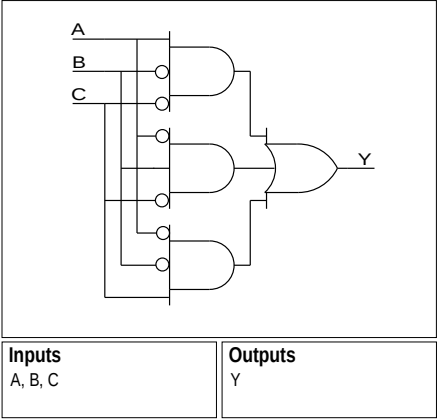
A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

MIN3X



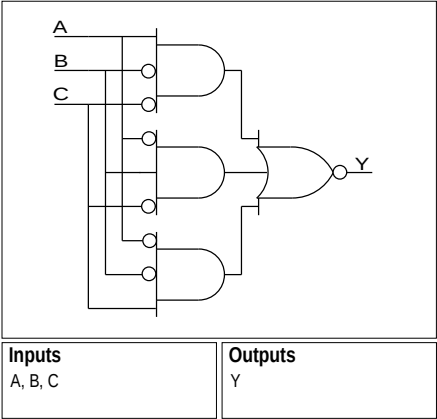
Function
1 of 3 function

Truth TableY

A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

Family	Modules	
	Seq	Comb
54SX		1

MIN3XI



Function
1 of 3 function with active low output

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Family	Modules	
	Seq	Comb
54SX		1

ACT 1

ACT 2/1200XL

ACT 3

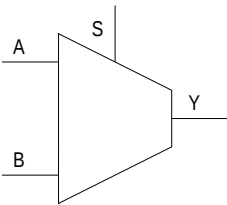
3200DX

40MX

42MX

54SX

MX2



Function
2 to 1 Multiplexer

Truth Table

S	Y
0	A
1	B

Inputs

A, S, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

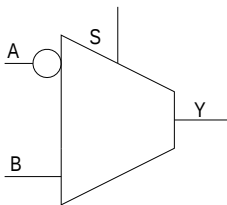
3200DX

40MX

42MX

54SX

MX2A



Function
2 to 1 Multiplexer with active low A-Input

Truth Table

S	Y
0	!A
1	B

Inputs

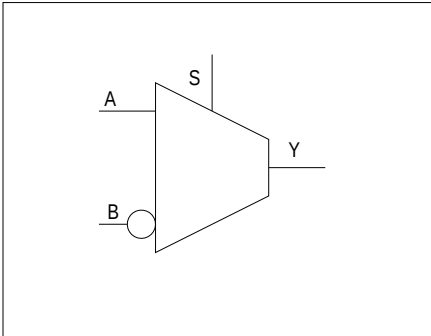
A, S, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

MX2B



Function
2 to 1 Multiplexer with active low B-Input

Truth Table

S	Y
0	A
1	$\text{!}B$

Inputs
A, S, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

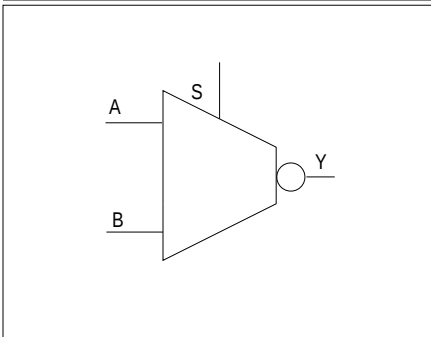
3200DX

40MX

42MX

54SX

MX2C



Function
2 to 1 Multiplexer with active low Output

Truth Table

S	Y
0	$\text{!}A$
1	$\text{!}B$

Inputs
A, S, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 1

ACT 2/1200XL

ACT 3

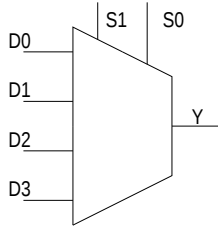
3200DX

40MX

42MX

54SX

MX4



Function
4 to 1 Multiplexer

Truth Table

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Inputs

D0, S0, S1, D1, D2, D3

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

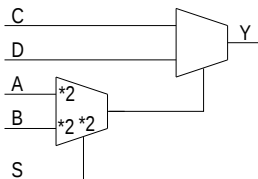
ACT 3

3200DX

40MX

42MX

MXC1



Function
Carry select multiplexer, used in adders

Truth Table

A	B	S	Y
0	X	0	C
1	X	0	D
X	0	1	C
X	1	1	D

Inputs

S, A, B, C, D

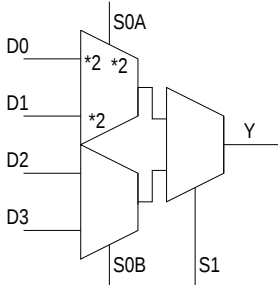
Outputs

Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

MXT



Function

Multiplexer with separate select lines

Truth Table

SOB	SOA	S1	Y
X	0	0	D0
X	1	0	D1
0	X	1	D2
1	X	1	D3

Inputs

D0 , D1, D2, D3, S0A, S0B, S1

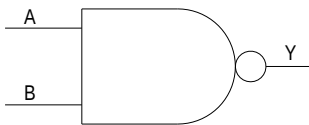
Outputs

Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* A 2 on the symbol implies a 2 logic module delay on all families except ACT 1 and 40MX.

NAND2



Function

2-Input NAND

Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

Inputs

A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

ACT 1

ACT 2/1200XL

ACT 3

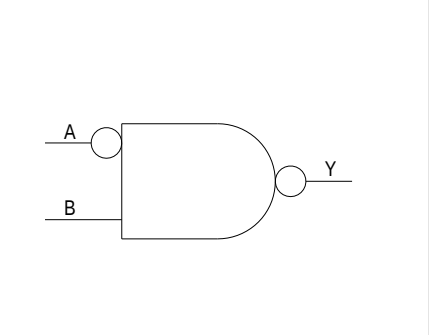
3200DX

40MX

42MX

54SX

NAND2A



Function
2-Input NAND with active low A-Input

Truth Table

A	B	Y
X	0	1
0	1	0
1	X	1

Inputs

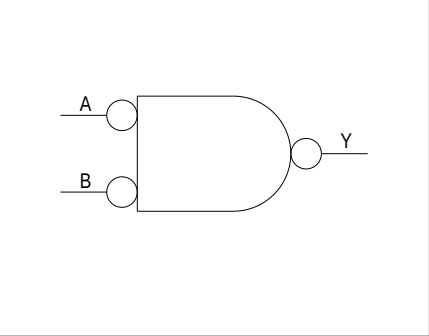
A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NAND2B



Function
2-Input NAND with active low Inputs

Truth Table

A	B	Y
0	0	0
X	1	1
1	X	1

Inputs

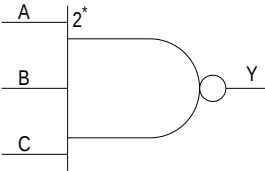
A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NAND3



Inputs
A, B, C

Outputs
Y

Function
3-Input NAND

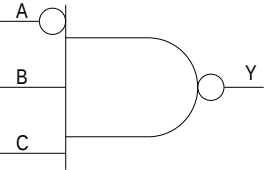
Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

NAND3A



Inputs
A, B, C

Outputs
Y

Function
3-Input NAND with active low A-input

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

ACT 1

NAND3B

ACT 2/1200XL

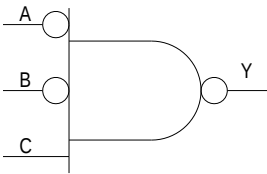
ACT 3

3200DX

40MX

42MX

54SX



Function
3-Input NAND with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

NAND3C

ACT 2/1200XL

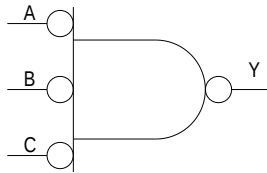
ACT 3

3200DX

40MX

42MX

54SX



Function
3-Input NAND with active low Inputs

Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Inputs

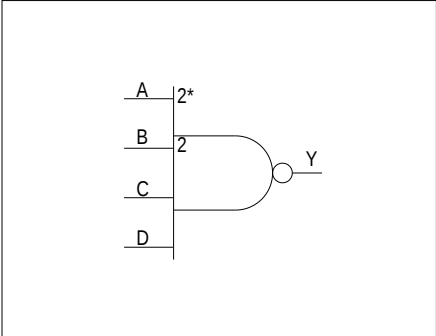
A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NAND4



Function
4-Input NAND

Truth Table

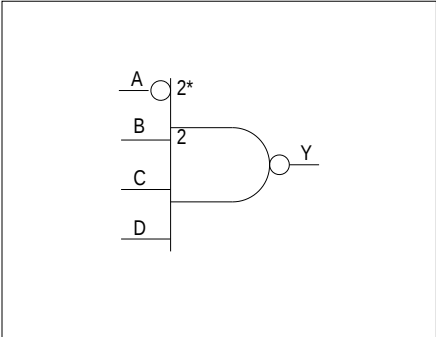
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

Inputs	Outputs
A, B, C, D	Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except in 54SX.

NAND4A



Function
4-Input NAND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	1	1	1	0
1	X	X	X	1

Inputs	Outputs
A, B, C, D	Y

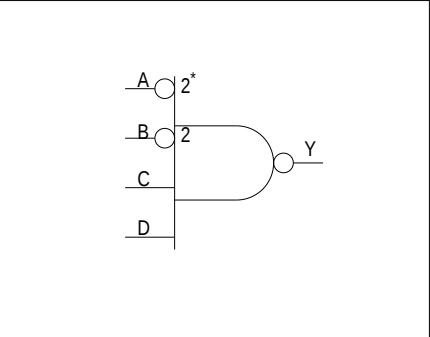
Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

NAND4B



Function
4-Input NAND with active low A- and B-Inputs

Truth Table

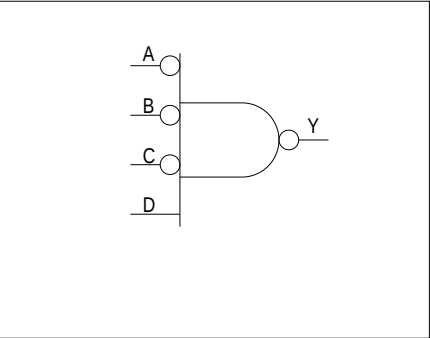
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	1	1	0
X	1	X	X	1
1	X	X	X	1

Inputs A, B, C, D	Outputs Y
-----------------------------	---------------------

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

NAND4C



Function
4-Input NAND with active low A-, B- and C-Inputs

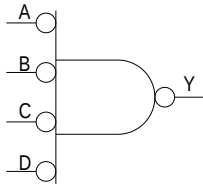
Truth Table

A	B	C	D	Y
X	X	X	0	1
0	0	0	1	0
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Inputs A, B, C, D	Outputs Y
-----------------------------	---------------------

Family	Modules	
	Seq	Comb
All		1

NAND4D

**Function**

4-Input NAND with active low Inputs

Truth Table

A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Inputs

A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

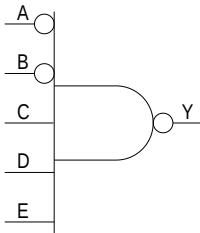
3200DX

40MX

42MX

54SX

NAND5B

**Function**

5-input NAND with active low A- and B-inputs

Truth Table

A	B	C	D	E	Y
1	X	X	X	X	1
X	1	X	X	X	1
X	X	0	X	X	1
X	X	X	0	X	1
X	X	X	X	0	1
0	0	1	1	1	0

Inputs

A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

ACT 2/1200XL

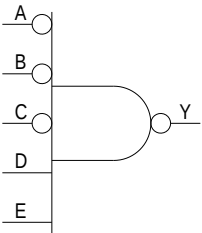
ACT 3

3200DX

42MX

54SX

NAND5C



Inputs
A, B, C, D, E

Outputs
Y

Function
5-Input NAND with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	0	X	1
0	0	0	1	1	0
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

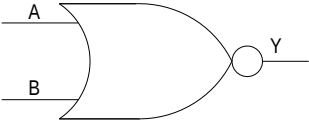
3200DX

40MX

42MX

54SX

NOR2



Inputs
A, B

Outputs
Y

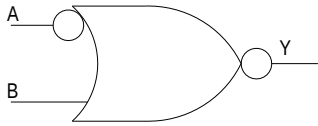
Function
2-Input NOR

Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

Family	Modules	
	Seq	Comb
All		1

NOR2A



Inputs
A, B

Outputs
Y

Function
2-Input NOR with active low A-Input

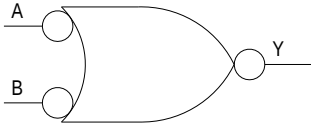
Truth Table

A	B	Y
0	X	0
1	0	1
X	1	0

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

NOR2B



Inputs
A, B

Outputs
Y

Function
2-Input NOR with active low Inputs

Truth Table

A	B	Y
X	0	0
0	X	0
1	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

NOR3

ACT 1

ACT 2/1200XL

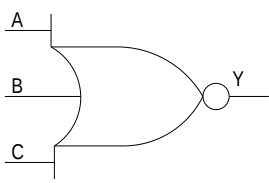
ACT 3

3200DX

40MX

42MX

54SX



Inputs

A, B, C

Outputs

Y

Function
3-Input NOR

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Family	Modules	
	Seq	Comb
All		1

NOR3A

ACT 1

ACT 2/1200XL

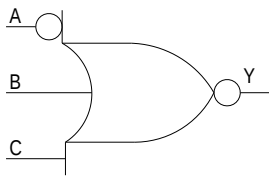
ACT 3

3200DX

40MX

42MX

54SX



Inputs

A, B, C

Outputs

Y

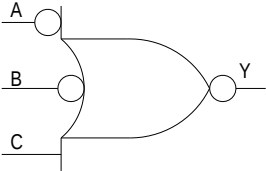
Function
3-Input NOR with active low A-Input

Truth Table

A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

Family	Modules	
	Seq	Comb
All		1

NOR3B



Inputs
A, B, C

Outputs
Y

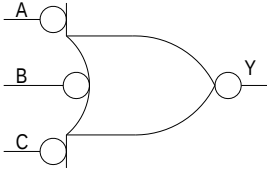
Function
3-Input NOR with active low A- and B-Inputs

Truth Table			
A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

NOR3C



Inputs
A, B, C

Outputs
Y

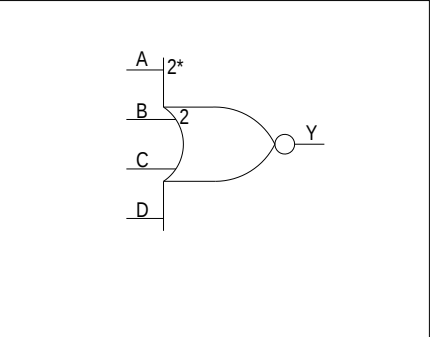
Function
3-Input NOR with active low Inputs

Truth Table			
A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

NOR4



Function
4-Input NOR

Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Inputs

A, B, C, D

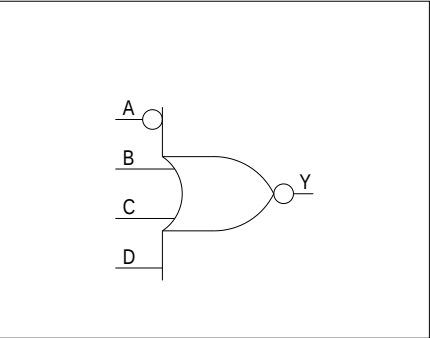
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except 54SX.

NOR4A



Function
4-Input NOR with active low A-Input

Truth Table

A	B	C	D	Y
0	X	X	X	0
1	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0

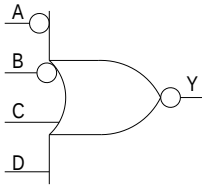
Inputs

A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NOR4B**Function**

4-Input NOR with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	0	X	X	0
0	X	X	X	0
1	1	0	0	1
X	X	X	1	0
X	X	1	X	0

Inputs

A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

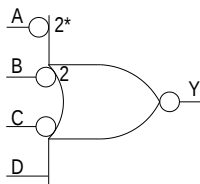
ACT 3

3200DX

40MX

42MX

54SX

NOR4C**Function**

4-Input NOR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	0	1
X	X	X	1	0

Inputs

A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

ACT 1

ACT 2/1200XL

ACT 3

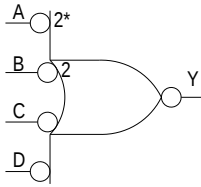
3200DX

40MX

42MX

54SX

NOR4D

**Function**

4-Input NOR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Inputs

A, B, C, D

Outputs

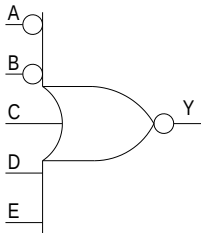
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

54SX

NOR5B

**Function**

5-Input NOR with active low A- and B-Inputs

Truth Table

A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	1	0
1	1	0	0	0	1

Inputs

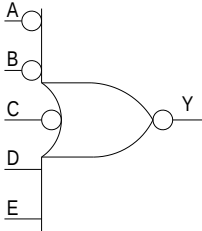
A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

NOR5C



Inputs
A, B, C, D, E

Outputs
Y

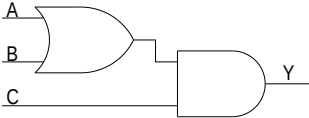
Function
5-Input NOR with active low A-, B- and C-Inputs

Truth Table					
A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	1	0	0	1

Family	Modules	
	Seq	Comb
All		1

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX
- 54SX

OA1



Inputs
A, B, C

Outputs
Y

Function
3 Input OR-AND

Truth Table			
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

OA1A

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

Inputs
A, B, C

Outputs
Y

Function
3 Input OR-AND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

Family	Modules	
	Seq	Comb
All		1

OA1B

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

Inputs
A, B, C

Outputs
Y

Function
3 Input OR-AND with active low C-Input

Truth Table

A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Family	Modules	
	Seq	Comb
All		1

OA1C

Inputs
A, B, C

Outputs
Y

Function
3 Input OR-AND with active low A- and C-Inputs

Truth Table

A	B	C	Y
0	X	0	1
X	X	1	0
1	0	X	0
X	1	0	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

OA2

Inputs
A, B, C, D

Outputs
Y

Function
2-wide 4-Input OR-AND

Truth Table

A	B	C	D	Y
X	X	0	0	0
0	0	X	X	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

OA2A

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

Inputs
A, B, C, D

Outputs
Y

Function 2 wide 4-Input OR-AND with active low A-Input				
Truth Table				
A	B	C	D	Y
X	X	0	0	0
0	X	X	1	1
0	X	1	X	1
1	0	X	X	0
X	1	X	1	1
X	1	1	X	1

Family	Modules	
	Seq	Comb
All		1

OA3

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

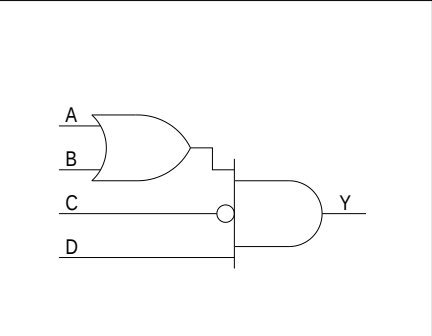
Inputs
A, B, C, D

Outputs
Y

Function 4 Input OR-AND				
Truth Table				
A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	X	X	0
X	1	1	1	1
1	X	1	1	1

Family	Modules	
	Seq	Comb
All		1

OA3A



Inputs	Outputs
A, B, C, D	Y

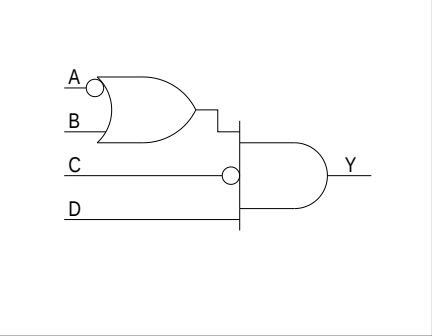
Function
4 Input OR-AND with active low C-Input

Truth Table				
A	B	C	D	Y
X	X	X	0	0
0	0	X	X	0
X	1	0	1	1
X	X	1	X	0
1	X	0	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

OA3B



Inputs	Outputs
A, B, C, D	Y

Function
4 Input OR-AND with active low A- and C-Inputs

Truth Table				
A	B	C	D	Y
X	X	X	0	0
0	X	0	1	1
X	X	1	X	0
1	0	X	X	0
X	1	0	1	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 2/1200XL

ACT 3

3200DX

42MX

54SX

OA4

```
graph LR; A --- OR1(( )); B --- OR1; C --- OR1; D --- OR1; OR1 --- AND1(( )); D --- AND1; AND1 --- Y
```

Inputs
A, B, C, D

Outputs
Y

Function
4 Input OR-AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	1	1

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

OA4A

```
graph LR; A --- OR1(( )); B --- OR1; C --- NOT1(( )) --- OR1; D --- OR1; OR1 --- AND1(( )); D --- AND1; AND1 --- Y
```

Inputs
A, B, C, D

Outputs
Y

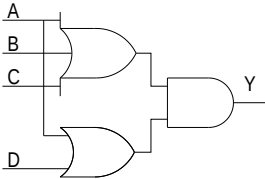
Function
4 Input OR-AND with active low C-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	1	1
0	0	1	X	0
X	1	X	1	1
1	X	X	1	1

Family	Modules	
	Seq	Comb
All		1

OA5



Inputs
A, B, C, D

Outputs
Y

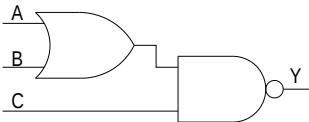
Function
4 Input complex OR-AND

Truth Table				
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

OAI1



Inputs
A, B, C

Outputs
Y

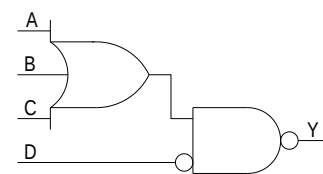
Function
3 Input OR-AND-INVERT

Truth Table			
A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

OAI2A



Inputs
A, B, C, D

Outputs
Y

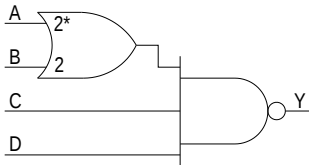
Function
4 Input OR-AND-INVERT with active low D-Input

Truth Table

A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Family	Modules	
	Seq	Comb
All		1

OAI3



Inputs
A, B, C, D

Outputs
Y

Function
4 Input OR-AND-INVERT

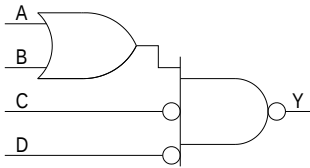
Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OAI3A

**Function**

4 Input OR-AND-INVERT with active low C- and D-Inputs

Truth Table

A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Inputs

A, B, C, D

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

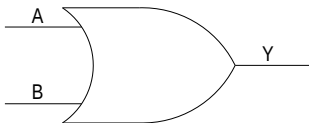
3200DX

40MX

42MX

54SX

OR2

**Function**

2-Input OR

Truth Table

A	B	Y
0	0	0
X	1	1
1	X	1

Inputs

A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

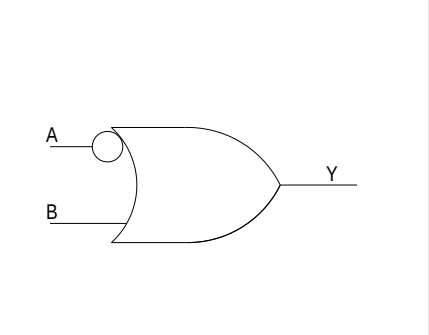
3200DX

40MX

42MX

54SX

OR2A



Function
2-Input OR with active low A-Input

Truth Table

A	B	Y
0	X	1
1	0	0
X	1	1

Inputs

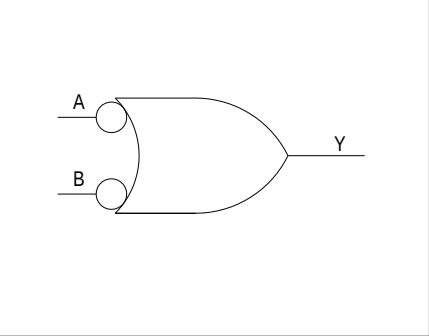
A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

OR2B



Function
2-Input OR with active low Inputs

Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

Inputs

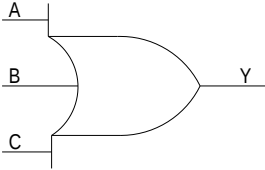
A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

OR3



Inputs
A, B, C

Outputs
Y

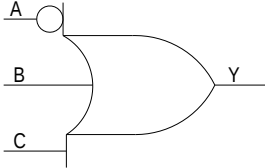
Function
3-Input OR

Truth Table

A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Family	Modules	
	Seq	Comb
All		1

OR3A



Inputs
A, B, C

Outputs
Y

Function
3-Input OR with active low A-Input

Truth Table

A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 1

ACT 2/1200XL

ACT 3

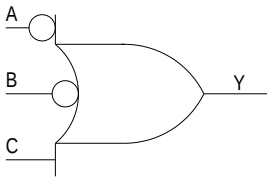
3200DX

40MX

42MX

54SX

OR3B

**Function**

3-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

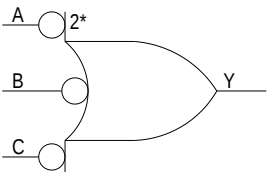
3200DX

40MX

42MX

54SX

OR3C

**Function**

3-Input OR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Inputs

A, B, C

Outputs

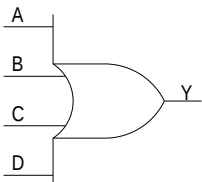
Y

Combinational, OR

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4

		Function 4-Input OR																												
		Truth Table <table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>X</td><td>X</td><td>X</td><td>1</td><td>1</td></tr><tr><td>X</td><td>X</td><td>1</td><td>X</td><td>1</td></tr><tr><td>X</td><td>1</td><td>X</td><td>X</td><td>1</td></tr><tr><td>1</td><td>X</td><td>X</td><td>X</td><td>1</td></tr></table>	A	B	C	D	Y	0	0	0	0	0	X	X	X	1	1	X	X	1	X	1	X	1	X	X	1	1	X	X
A	B	C	D	Y																										
0	0	0	0	0																										
X	X	X	1	1																										
X	X	1	X	1																										
X	1	X	X	1																										
1	X	X	X	1																										
Inputs A, B, C, D	Outputs Y																													

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

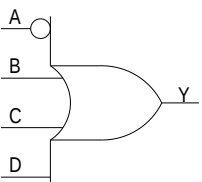
3200DX

40MX

42MX

54SX

OR4A

		Function 4-Input OR with active low A-Input																												
		Truth Table <table><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>X</td><td>X</td><td>X</td><td>1</td><td>1</td></tr><tr><td>X</td><td>X</td><td>1</td><td>X</td><td>1</td></tr><tr><td>X</td><td>1</td><td>X</td><td>X</td><td>1</td></tr></table>	A	B	C	D	Y	0	X	X	X	1	1	0	0	0	0	X	X	X	1	1	X	X	1	X	1	X	1	X
A	B	C	D	Y																										
0	X	X	X	1																										
1	0	0	0	0																										
X	X	X	1	1																										
X	X	1	X	1																										
X	1	X	X	1																										
Inputs A, B, C, D	Outputs Y																													

Family	Modules	
	Seq	Comb
All		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

OR4B

ACT 1

ACT 2/1200XL

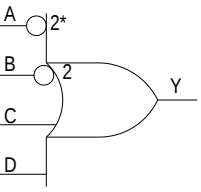
ACT 3

3200DX

40MX

42MX

54SX



Inputs

A, B, C, D

Outputs

Y

Function				
4-Input OR with active low A- and B-Inputs				
Truth Table				
A	B	C	D	Y
X	0	X	X	1
0	X	X	X	1
1	1	0	0	0
X	X	X	1	1
X	X	1	X	1

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4C

ACT 1

ACT 2/1200XL

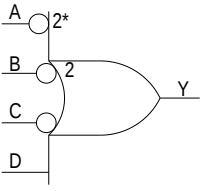
ACT 3

3200DX

40MX

42MX

54SX



Inputs

A, B, C, D

Outputs

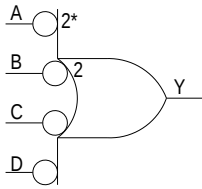
Y

Function				
4-Input OR with active low A-, B- and C-Inputs				
Truth Table				
A	B	C	D	Y
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	0	0
X	X	X	1	1

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4D



Function
4-Input OR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

Inputs

A, B, C, D

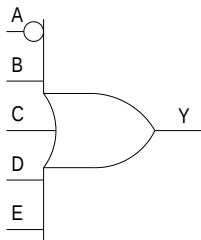
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except for 54SX.

OR5A



Function
5-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	D	E	Y
0	X	X	X	1	1
X	1	X	X	X	1
X	X	1	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	0	0	0	0	0

Inputs

A, B, C, D, E

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

54SX

ACT 2/1200XL

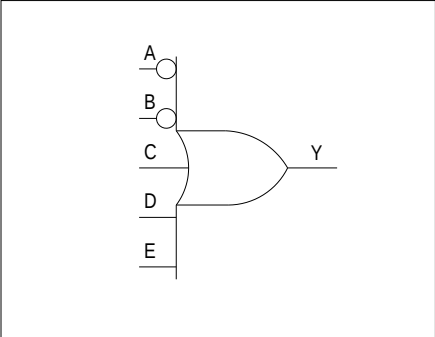
ACT 3

3200DX

42MX

54SX

OR5B



Inputs	Outputs
A, B, C, D, E	Y

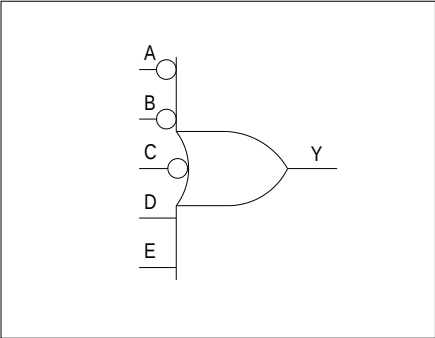
Function
5-Input OR with active low A-Input

Truth Table					
A	B	C	D	E	Y
X	0	X	X	X	1
0	X	X	X	X	1
1	1	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1

Family	Modules	
	Seq	Comb
All		1

54SX

OR5C



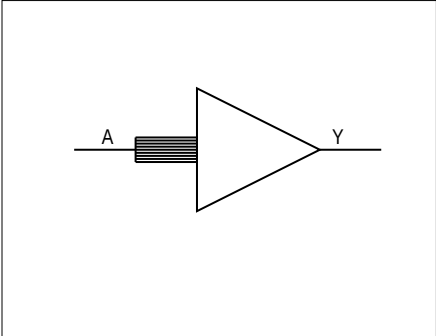
Inputs	Outputs
A, B, C, D, E	Y

Function
5-Input OR with active low A-, B- and C-Inputs

Truth Table					
A	B	C	D	E	Y
0	X	X	X	X	1
X	0	X	X	X	1
X	X	0	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	1	1	0	0	0

Family	Modules	
	Seq	Comb
54SX		1

QCLKINT



Function
Internal Clock Interface

Truth Table

A	Y
0	0
1	1

Inputs

A

Outputs

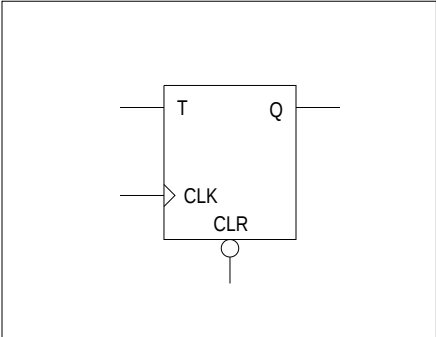
Y

NOTE: QCLKINT does not use any modules.
For more information on the Global Clock Network, refer to Actel's Databook.

3200DX

42MX

TF1A



Function
T-Type Flip-Flop with active low Clear

Truth Table

CLR	T	CLK	Q_{n+1}
0	X	X	0
1	1	$\uparrow$	!Q
1	0	$\uparrow$	Q

Inputs

CLR, T, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
All	1	

ACT 2/1200XL

ACT 3

3200DX

42MX

54SX

ACT 2/1200XL

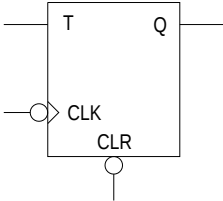
ACT 3

3200DX

42MX

54SX

TF1B



Function

T-Type Flip-Flop with active low Clear and Clock

Truth Table

CLR	T	CLK	Q _{n+1}
0	X	X	0
1	1	↓	!Q
1	0	↓	Q

Inputs

CLR, T, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
All	1	

ACT 1

ACT 2/1200XL

ACT 3

3200DX

40MX

42MX

54SX

VCC



Function

Power

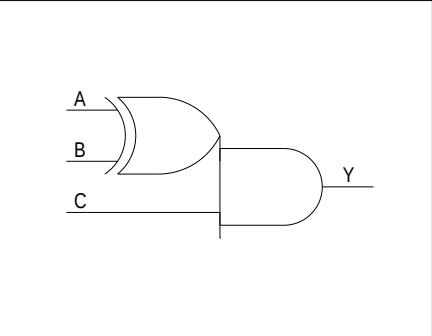
Inputs

Outputs

Y

NOTE: VCC does not use any module.

XA1



Function
3 Input XOR-AND

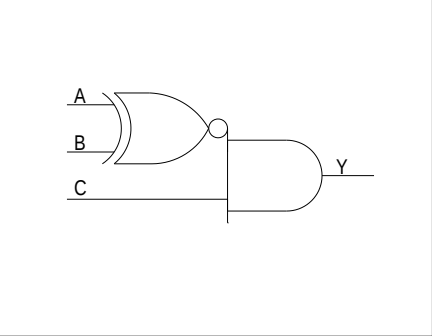
Truth Table			
A	B	C	Y
X	X	0	0
0	0	X	0
0	1	1	1
1	0	1	1
1	1	X	0

Inputs	Outputs
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

XA1A



Function
3 Input XNOR-AND

Truth Table			
A	B	C	Y
X	X	0	0
0	0	1	1
0	1	X	0
1	0	X	0
1	1	1	1

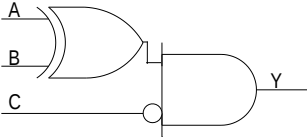
Inputs	Outputs
A, B, C	Y

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

54SX

XA1B



Inputs
A, B, C

Outputs
Y

Function
3 Input XNOR-AND with active low C-input

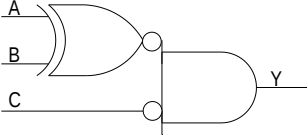
Truth Table

A	B	C	Y
X	X	1	0
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0

Family	Modules	
	Seq	Comb
54SX		1

54SX

XA1C



Inputs
A, B, C

Outputs
Y

Function
3 Input XNOR-AND with active low C-input

Truth Table

A	B	C	Y
X	X	1	0
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1

Family	Modules	
	Seq	Comb
54SX		1

54SX

XAI1

A

B

C

Y

Function

3 Input XNOR-NAND

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Inputs

A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

XAI1A

A

B

C

Y

Function

3 Input XNOR-NAND

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Inputs

A, B, C

Outputs

Y

54SX

Family	Modules	
	Seq	Comb
54SX		1

ACT 1

ACT 2/1200XL

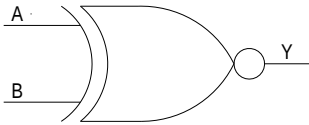
ACT 3

3200DX

40MX

42MX

54SX

XNOR2
Function
 2 Input XNOR
Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Inputs

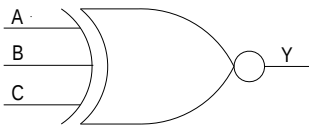
A, B, Y

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

54SX

XNOR3
Function
 3 Input XNOR
Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Inputs

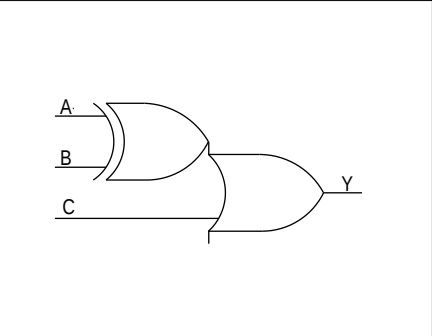
A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

XO1



Inputs	Outputs
A, B, C	Y

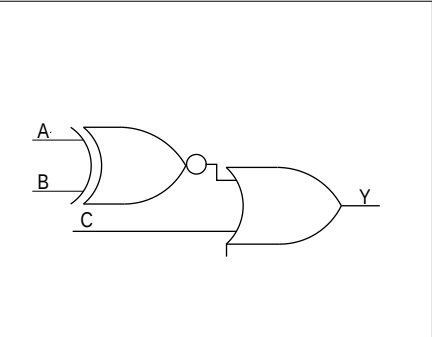
Function
3 Input XOR-OR

Truth Table			
A	B	C	Y
0	0	0	0
X	X	1	1
0	1	X	1
1	0	X	1
1	1	0	0

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

XO1A



Inputs	Outputs
A, B, C	Y

Function
3 Input XOR-OR

Truth Table			
A	B	C	Y
0	0	0	1
X	X	1	1
0	1	0	0
1	0	0	0
1	1	0	1

Family	Modules	
	Seq	Comb
All		1

- ACT 1
- ACT 2/1200XL
- ACT 3
- 3200DX
- 40MX
- 42MX
- 54SX

ACT 1

ACT 2/1200XL

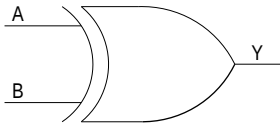
ACT 3

3200DX

40MX

42MX

54SX

XOR2
Function
 2 Input XOR
Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Inputs

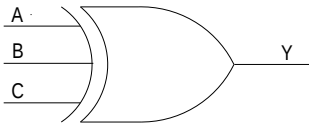
A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

54SX

XOR3
Function
 3 Input XOR
Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

Inputs

A, B, C

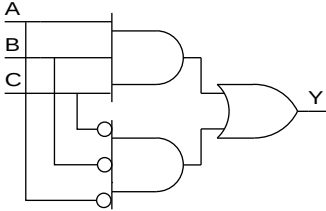
Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

ZOR3



Function

3 Input function

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

Inputs

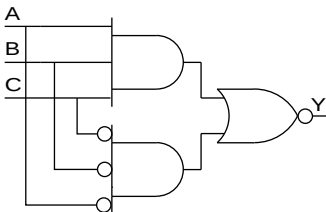
A, B, C

Outputs

Y

Family	Modules	
	Seq	Comb
54SX		1

ZOR3



Function

3 Input function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Inputs

A, B, C

Outputs

Y

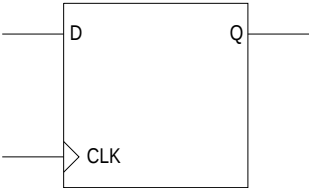
54SX

Family	Modules	
	Seq	Comb
54SX		1

CC-Module Flip Flops

These macros are useful in some radiation hostile applications. They sacrifice area in exchange for a lower single-event upset (SEU) rate caused by ion particle collisions. These special cells use two combinational modules to implement a register instead of using the dedicated registers in the array. (See the application note titled, *Design Techniques for RadHard Field Programmable Gate Arrays*.)

DF1_CC



Inputs

D, CLK

Outputs

Q

Function

D-Type Flip-Flop

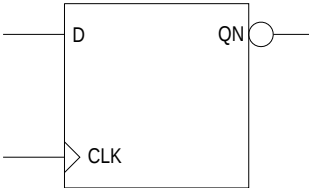
Truth Table

CLK	Q _{n+1}
↑	D

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

DF1A_CC



Inputs

D, CLK

Outputs

QN

Function

D-Type Flip-Flop with active low Output

Truth Table

CLK	QN _{n+1}
↑	!D

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

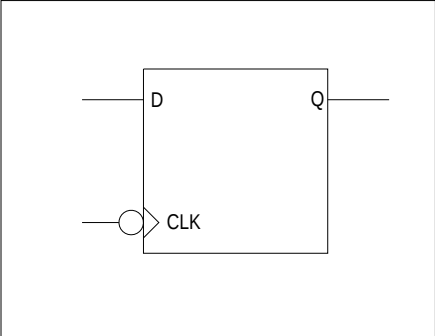
ACT 2/1200XL

ACT 3

3200DX

42MX

DF1B_CC



Function
D-Type Flip-Flop with active low Clock

Truth Table

CLK	Q_{n+1}
↓	D

Inputs	Outputs
D, CLK	Q

Family	Modules	
	Seq	Comb
All		2

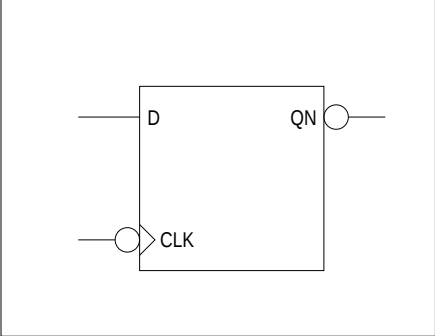
ACT 2/1200XL

ACT 3

3200DX

42MX

DF1C_CC



Function
D-Type Flip-Flop with active low Clock and Output

Truth Table

CLK	QN_{n+1}
↓	!D

Inputs	Outputs
D, CLK	QN

Family	Modules	
	Seq	Comb
All		2

DFC1_CC

Logic diagram of DFC1_CC: A D-type flip-flop with inputs D, CLK, and CLR. The output is Q. The CLR input is active high.

Function
D-Type Flip-Flop, with active high Clear

Truth Table

CLR	CLK	Q _{n+1}
1	X	0
0	↑	D

Inputs CLR, D, CLK	Outputs Q	

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

DFC1A_CC

Logic diagram of DFC1A_CC: A D-type flip-flop with inputs D, CLK, and CLR. The output is Q. The CLR input is active high, and the CLK input is active low.

Function
D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

CLR	CLK	Q _{n+1}
1	X	0
0	↓	D

Inputs CLR, D, CLK	Outputs Q	

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

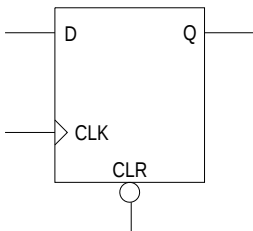
ACT 2/1200XL

DFC1B_CC

ACT 3

3200DX

42MX



Function

D-Type Flip-Flop, with active low Clear

Truth Table

CLR	CLK	Q_{n+1}
0	X	0
1	↑	D

Inputs

CLR, D, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
All		2

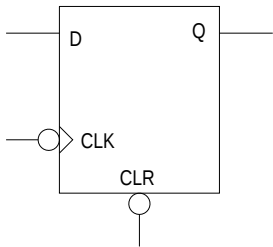
ACT 2/1200XL

DFC1D_CC

ACT 3

3200DX

42MX



Function

D-Type Flip-Flop, with active low Clear and Clock

Truth Table

CLR	CLK	Q_{n+1}
0	X	0
1	↓	D

Inputs

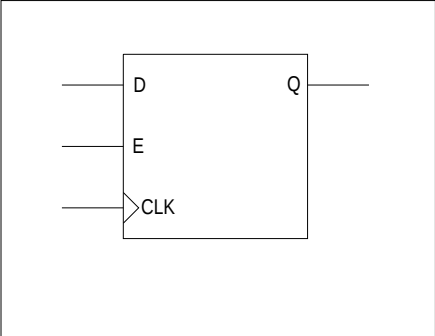
CLR, D, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
All		2

DFE_CC



Function
D-Type Flip-Flop, with active high Enable

Truth Table

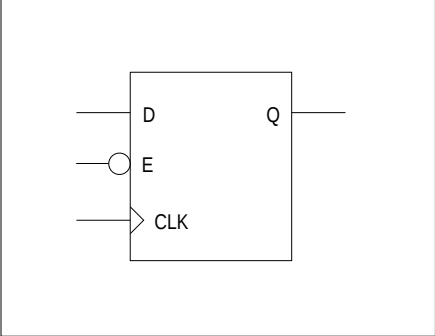
E	CLK	Q _{n+1}
0	X	Q
1	↑	D

Inputs	Outputs
D, E, CLK	Q

Family	Modules	
	Seq	Comb
All		2

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

DFE1B_CC



Function
D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q _{n+1}
1	X	Q
0	↑	D

Inputs	Outputs
D, E, CLK	Q

Family	Modules	
	Seq	Comb
All		2

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

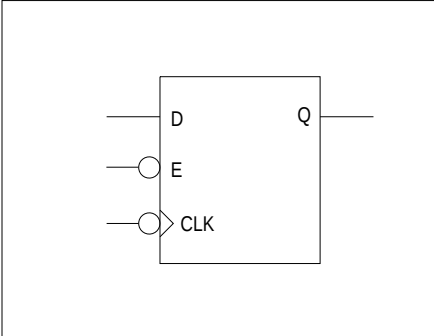
ACT 2/1200XL

DFE1C_CC

ACT 3

3200DX

42MX



Function
D-Type Flip-Flop, with active low Enable and Clock

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↓	D

Inputs	Outputs
D, E, CLK	Q

Family	Modules	
	Seq	Comb
All		2

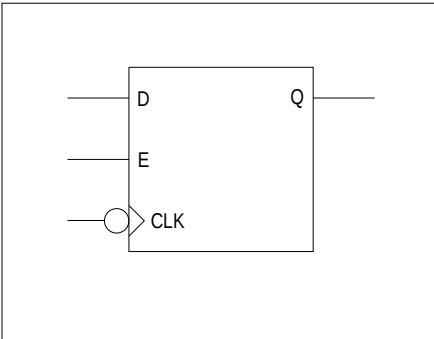
ACT 2/1200XL

DFEA_CC

ACT 3

3200DX

42MX



Function
D-Type Flip-Flop, with Enable, and active low Clock

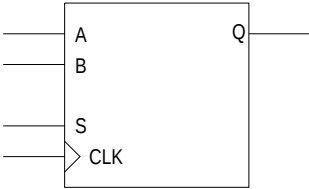
Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↓	D

Inputs	Outputs
D, E, CLK	Q

Family	Modules	
	Seq	Comb
All		2

DFM_CC



Inputs

A, B, S, CLK

Outputs

Q

Function

D-Type Flip-Flop with 2-input Multiplexed Data

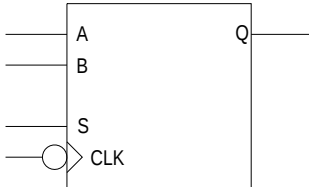
Truth Table

S	CLK	Q _{n+1}
0	↑	A
1	↑	B

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

DFMA_CC



Inputs

A, B, S, CLK

Outputs

Q

Function

D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

S	CLK	Q _{n+1}
0	↓	A
1	↓	B

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

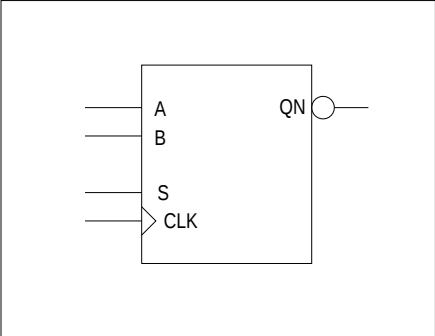
ACT 2/1200XL

ACT 3

3200DX

42MX

DFM1B_CC



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

S	CLK	QN _{n+1}
0	↑	!A
1	↑	!B

Inputs	Outputs
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All		2

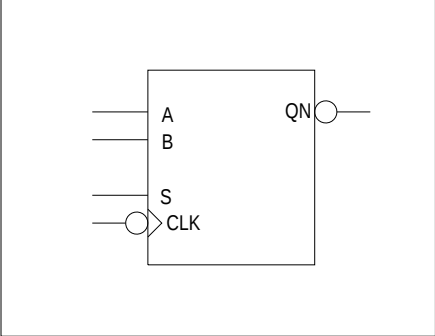
ACT 2/1200XL

ACT 3

3200DX

42MX

DFM1C_CC



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

S	CLK	QN _{n+1}
0	↓	!A
1	↓	!B

Inputs	Outputs
A, B, S, CLK	QN

Family	Modules	
	Seq	Comb
All		2

DFP1_CC*

Logic diagram of DFP1_CC: A D-type flip-flop with inputs D, PRE (active high), and CLK (active high). The output is Q.

Function

D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↑	D

Inputs

D, PRE, CLK

Outputs

Q

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1.

DFP1A_CC*

Logic diagram of DFP1A_CC: A D-type flip-flop with inputs D, PRE (active high), and CLK (active low). The output is Q.

Function

D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q _{n+1}
1	X	1
0	↓	D

Inputs

D, PRE, CLK

Outputs

Q

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1A.

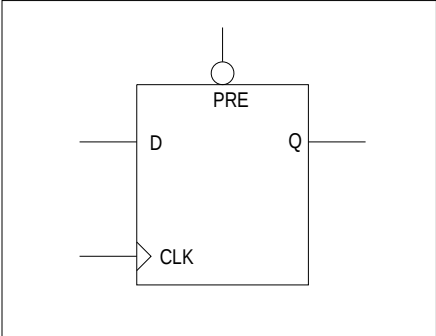
ACT 2/1200XL

DFP1B_CC*

ACT 3

3200DX

42MX



Function
D-Type Flip-Flop with active low Preset

Truth Table

PRE	CLK	Q _{n+1}
0	X	1
1	↑	D

Inputs D, PRE, CLK	Outputs Q
------------------------------	---------------------

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1B.

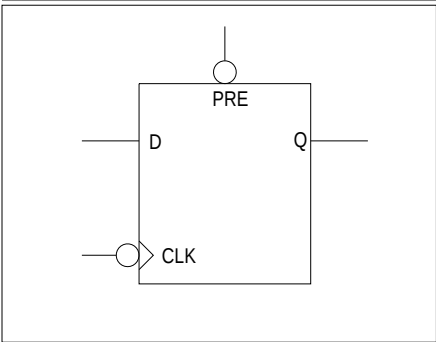
ACT 2/1200XL

DFP1D_CC*

ACT 3

3200DX

42MX



Function
D-Type Flip-Flop with active low Preset and Clock

Truth Table

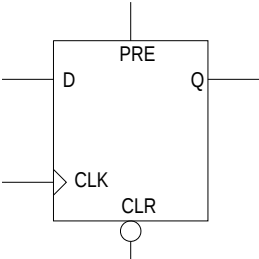
PRE	CLK	Q _{n+1}
0	X	1
1	↓	D

Inputs D, PRE, CLK	Outputs Q
------------------------------	---------------------

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1D.

DFPC_CC*



Function
D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	X	X	0
1	1	X	1
1	0	↓	D

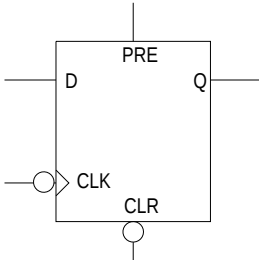
Inputs	Outputs
CLR, D, PRE, CLK	Q

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

* Identical to DFPC

DFPCA_CC*



Function
D-Type Flip-Flop with active high Preset, active low Clear, and active low Clock

Truth Table

CLR	PRE	CLK	Q _{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	**

Inputs	Outputs
CLR, D, PRE, CLK	Q

- ACT 2/1200XL
- ACT 3
- 3200DX
- 42MX

Family	Modules	
	Seq	Comb
All		2

* Identical to Macro DFPCA

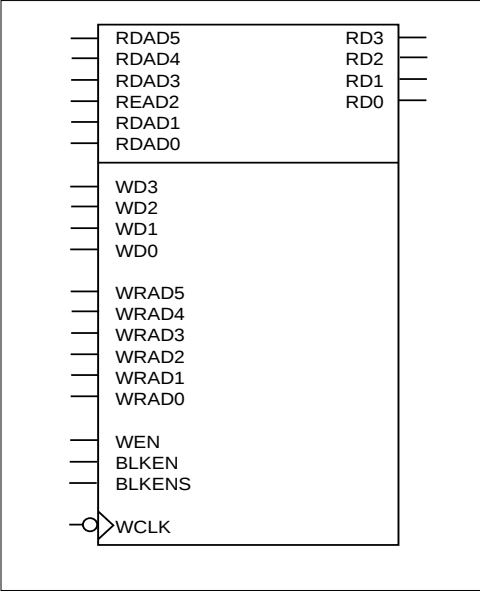
** Your design should not allow both PRE and CLR to be asserted at the same time.

RAM Macros

3200DX

42MX

RAM4FA



Function

64X4 dual-port RAM with falling Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

- NOTE 1: RDAD contents always appear at RD.
- NOTE 2: BLKENS must be driven by a GND or VCC macro.
- NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

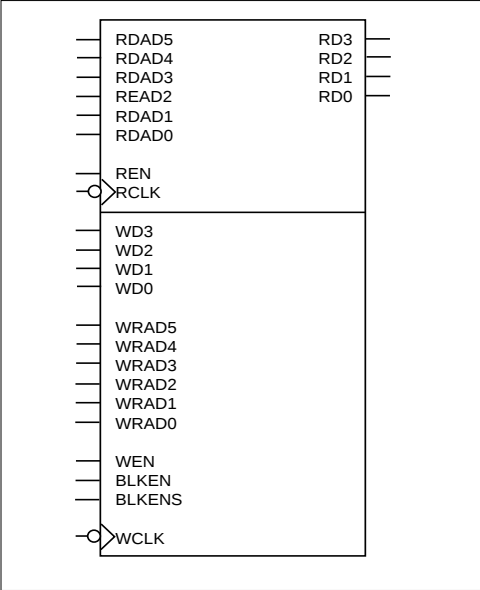
Inputs	Outputs
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK	RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM4FF



Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD3, RD2, RD1, RD0

Function

64X4 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

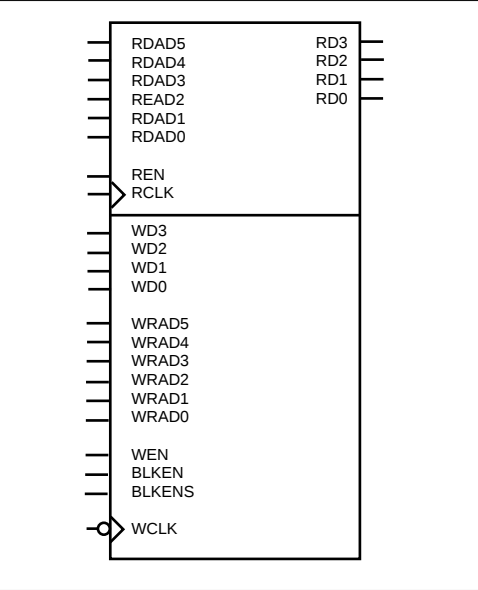
NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

3200DX

42MX

RAM4FR



Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD3, RD2, RD1, RD0

Function

64X4 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

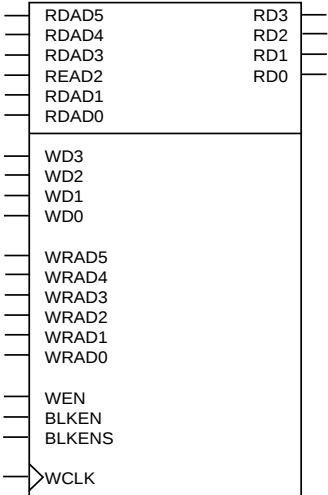
NOTE 1: BLKENS must be driven by a GND or VCC macro.
NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

3200DX

42MX

RAM4RA



Function

64X4 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

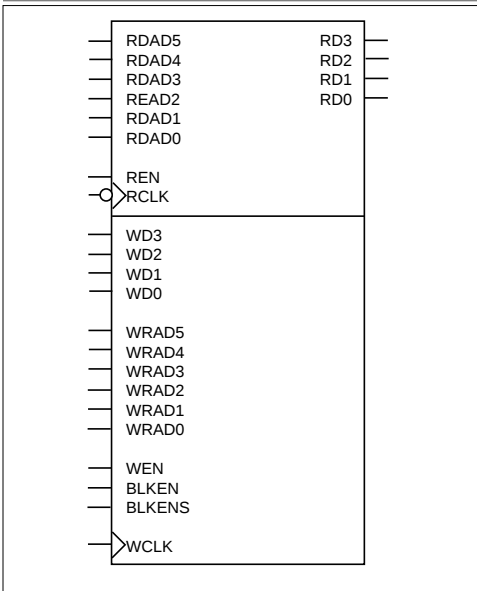
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM4RF



Function

64X4 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

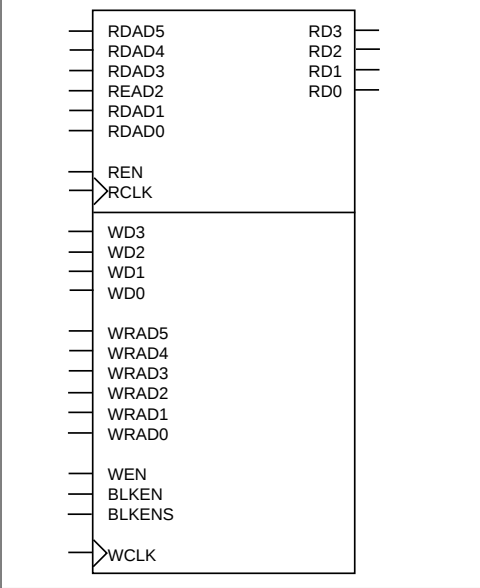
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM4RR



Function

64X4 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

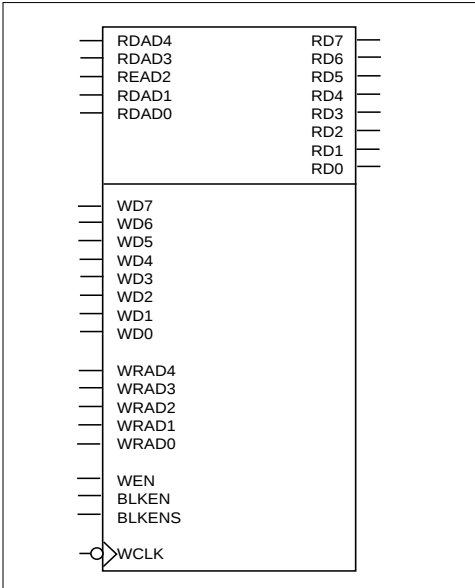
RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM8FA



Function

32X8 dual-port RAM with falling Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

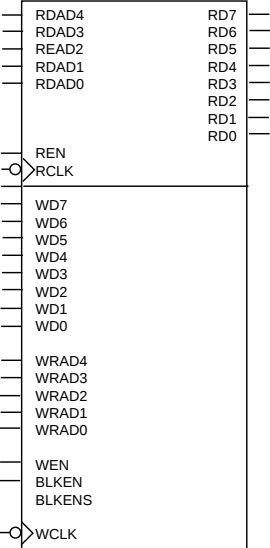
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM8FF



Function

32X8 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

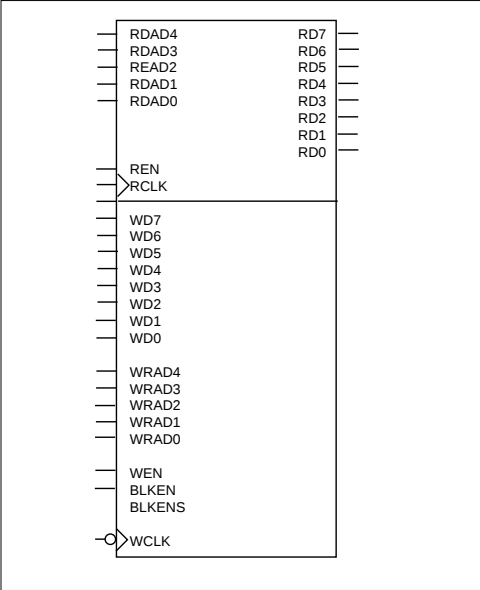
NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

3200DX

42MX

RAM8FR



Function

32X8 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

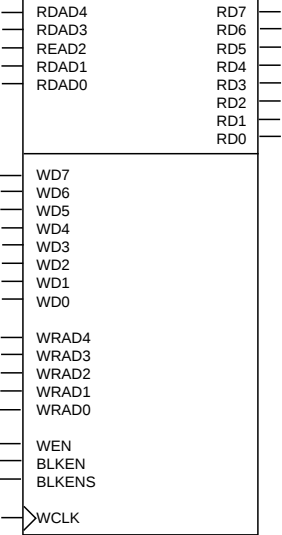
NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

3200DX

42MX

RAM8RA



Function

32X8 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

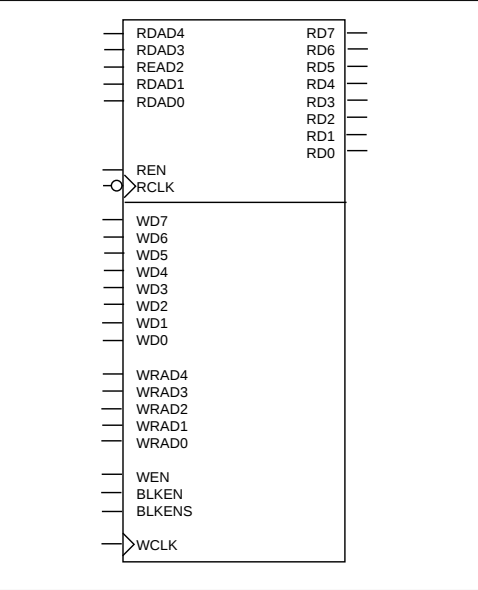
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM8RF



Function

32X8 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

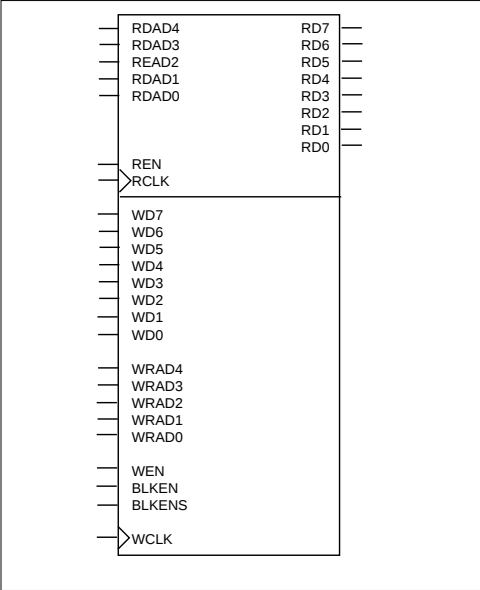
NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

3200DX

42MX

RAM8RR



Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Function

32X8 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

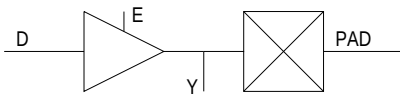
RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Family	Modules
	RAM
All	1

I/O Macros

General Use I/O Macros

BIBUF



Function

Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

Truth Table

MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

Inputs
D, E, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
All		1

ACT 1

ACT 2/1200XL

ACT 3

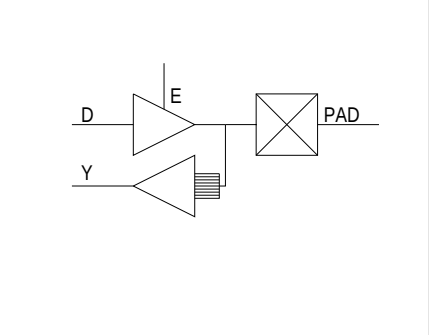
3200DX

40MX

42MX

54SX

CLKBIBUF



Function
Biderctional with Input Dedicated to routed Clock Network

Truth Table			
D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

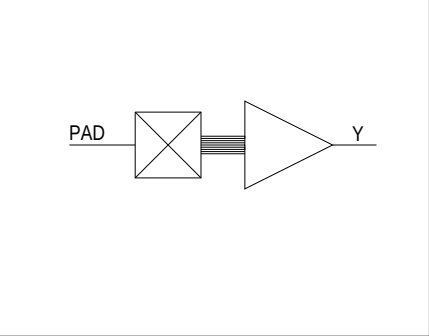
Inputs
D, E, PAD

Outputs
PAD, Y

NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

CLKBUF



Function
Input for Dedicated Routed Clock Network

Truth Table	
PAD	Y
0	0
1	1

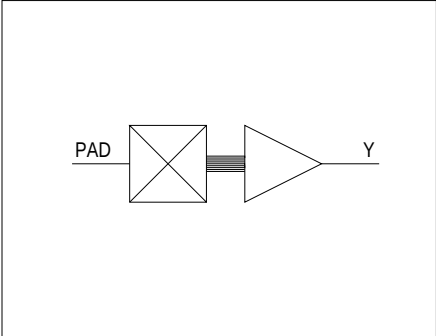
Inputs
PAD

Outputs
Y

NOTE 1: For an internal Clock net, refer to the CLKINT macro.
NOTE 2: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

HCLKBUF



Function
Dedicated high-speed S-Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

Inputs
PAD

Outputs
Y

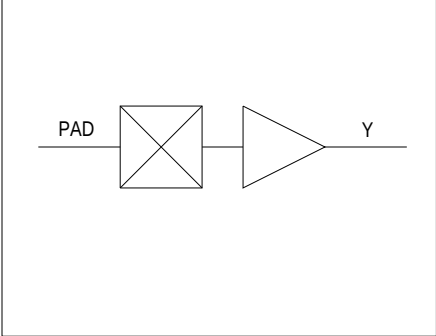
NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

ACT 3

54SX

INBUF



Function
Input Buffer

Truth Table

PAD	Y
0	0
1	1

Inputs
PAD

Outputs
Y

Family	Modules	
	Seq	I/O
All		1

ACT 1

ACT 2/1200XL

ACT 3

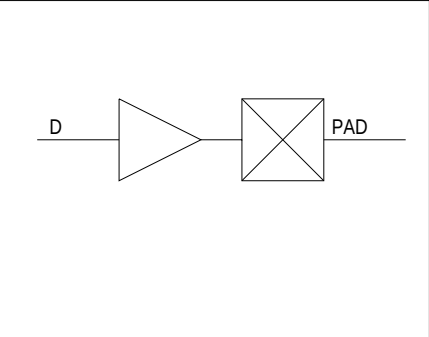
3200DX

40MX

42MX

54SX

OUTBUF



Function
Output Buffer, High Slew

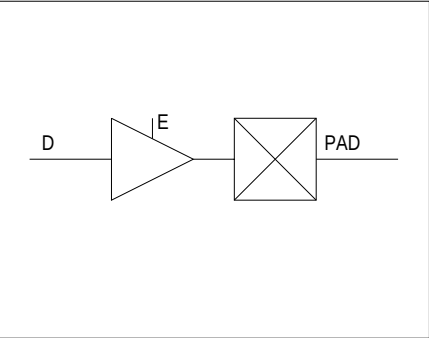
Truth Table

D	PAD
0	0
1	1

Inputs	Outputs
D	PAD

Family	Modules	
	Seq	I/O
All		1

TRIBUFF



Function
Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

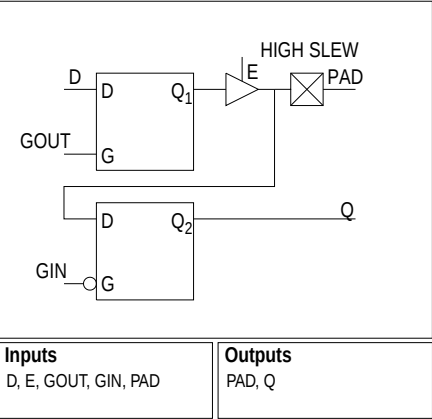
Inputs	Outputs
D, E	PAD

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

Family	Modules	
	Seq	I/O
All		1

ACT 2/XL/DX/42MX I/O Macros

BBDLHS



Function
Bidirectional with Input Latch and Output Latch

Truth Table

MODE	E	GOUT	GIN	PAD	Q
OUTPUT	1	0	1	PAD _{n-1}	Q _{n-1}
	1	1	0	D	D
INPUT	0	X	1	X	Q _{n-1}
	0	X	0	X	PAD

Family	Modules	
	Seq	I/O
All		1

- ACT 2/1200XL
- 3200DX
- 42MX

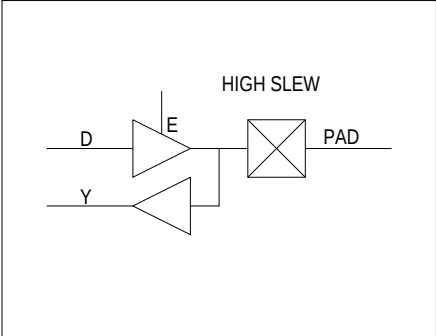
ACT 2/1200XL

ACT 3

3200DX

42MX

BBHS



Function
Bidirectional Buffer, High Slew

Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Inputs

D, E, PAD

Outputs

PAD, Y

Family	Modules	
	Seq	I/O
All		1

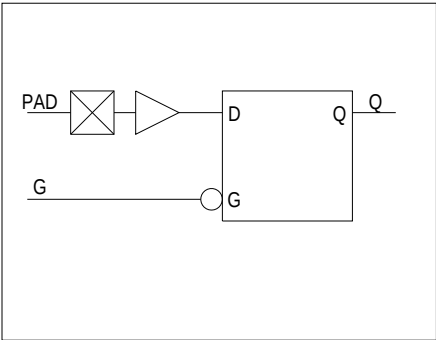
NOTE: For new designs, instead of BBHS we recommend that you use BIBUF on page 221.

ACT 2/1200XL

3200DX

42MX

IBDL



Function
Input Buffer with Input Latch, with active low Clock

Truth Table

G	Q
1	Q_{n-1}
0	PAD

Inputs

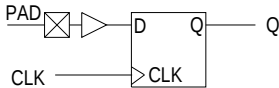
G, PAD

Outputs

Q

Family	Modules	
	Seq	I/O
All		1

IR



Inputs
PAD, CLK

Outputs
Q

Function
Input Register

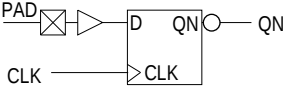
Truth Table

CLK	Q
↑	PAD

Family	Modules	
	Seq	I/O
All	1	1

- ACT 2/1200XL
- 3200DX
- 42MX

IRI



Inputs
PAD, CLK

Outputs
QN

Function
Input register with active Low output

Truth Table

CLK	QN
↑	!PAD

Family	Modules	
	Seq	I/O
All	1	1

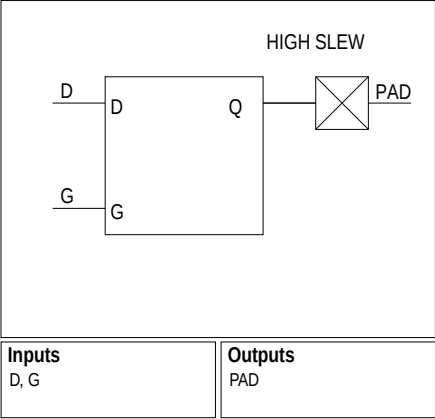
- ACT 2/1200XL
- 3200DX
- 42MX

ACT 2/1200XL

3200DX

42MX

OBDLHS



Function
Output Buffer with Output Latch, High Slew

Truth Table

G	PAD
0	PAD _{n-1}
1	D

Family	Modules	
	Seq	I/O
All		1

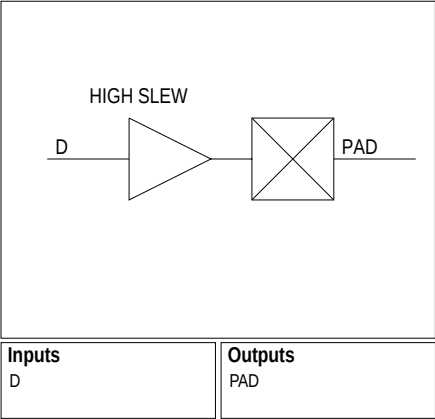
ACT 2/1200XL

ACT 3

3200DX

42MX

OBHS



Function
Output Buffer, High Slew

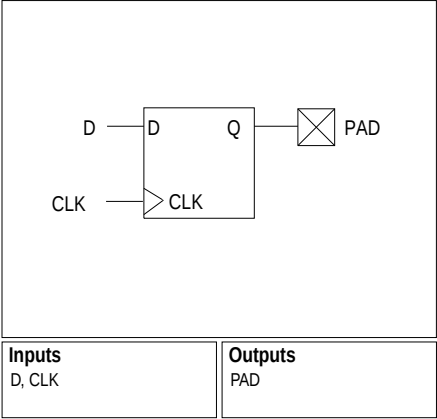
Truth Table

D	PAD
0	0
1	1

Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of OBHS we recommend that you use OUTBUF on page 224.

ORH



Function
Output Register, High Slew

Truth Table

CLK	PAD _{n+1}
↑	D

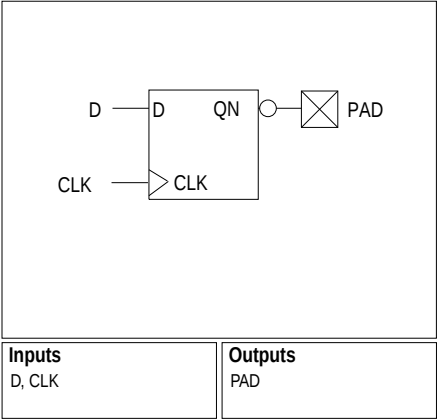
Family	Modules	
	Seq	I/O
All	1	1

ACT 2/1200XL

3200DX

42MX

ORIH



Function
Inverted Output Register, High Slew

Truth Table

CLK	PAD _{n+1}
↑	!D

Family	Modules	
	Seq	I/O
All	1	1

ACT 2/1200XL

3200DX

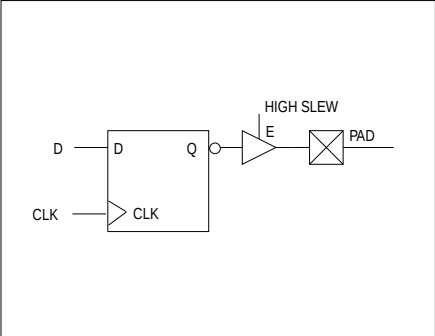
42MX

ACT 2/1200XL

ORITH

3200DX

42MX



Function
Inverted Output Register, Tristate Enable, High Slew

Truth Table

E	CLK	PAD _{n+1}
0	X	Z
1	↑	!D

Inputs
D, E, CLK

Outputs
PAD

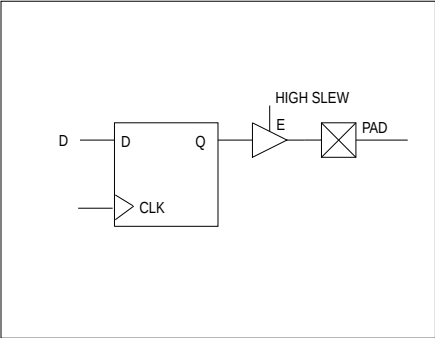
Family	Modules	
	Seq	I/O
All	1	1

ACT 2/1200XL

ORTH

3200DX

42MX



Function
Output Register, Tristate Enable, High Slew

Truth Table

E	CLK	PAD _{n+1}
0	X	Z
1	↑	D

Inputs
D, E, CLK

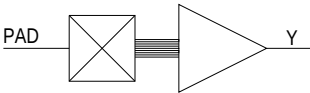
Outputs
PAD

Family	Modules	
	Seq	I/O
All	1	1

3200DX

42MX

QCLKBUF



Function
Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

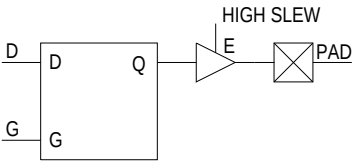
Inputs
PAD

Outputs
Y

NOTE 1: For an internal Clock net, refer to the CLKINT macro.
NOTE 2: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

TBDLHS



Function
Tristate Output with Latch, High Slew

Truth Table

E	G	PAD
0	X	Z
1	1	D
1	0	PAD _{n-1}

Inputs
D, E, G

Outputs
PAD

Family	Modules	
	Seq	I/O
All		1

ACT 2/1200XL

3200DX

42MX

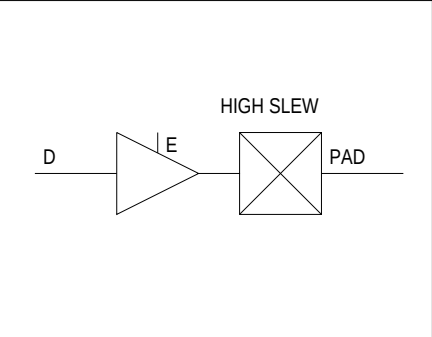
ACT 2/1200XL

ACT 3

3200DX

42MX

TBHS



Function
Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

Inputs
D, E

Outputs
PAD

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

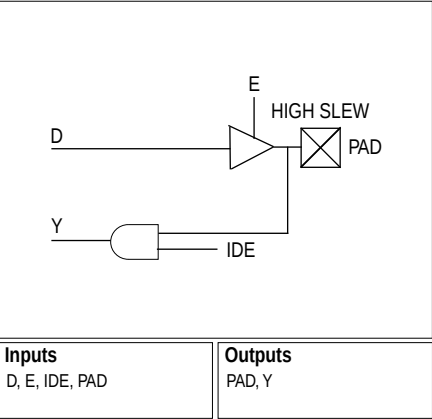
Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of TBHS we recommend that you use TRIBUFF on page 224.

ACT 3 I/O Macros

BBHSA

ACT 3



Function
Bidirectional buffer with AND gate, High Slew

Truth Table				
MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

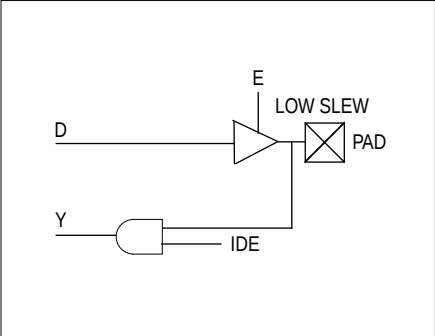
Inputs
D, E, IDE, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BBLSA



Function
Bidirectional buffer with AND gate, Low Slew

Truth Table

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

Inputs

D, E, IDE, PAD

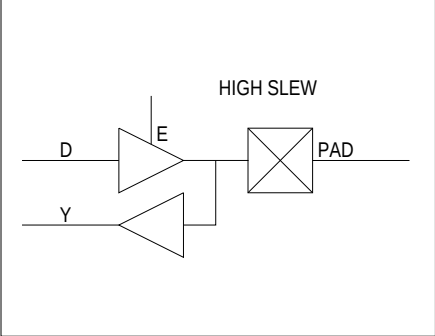
Outputs

PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BBUFTH



Function
Bidirectional Buffer, Tristate Enable, High Slew

Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

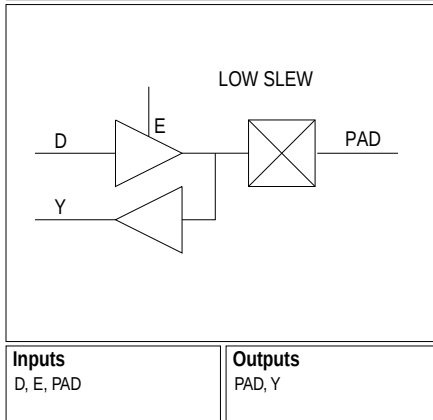
Inputs

D, E, PAD

Outputs

PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

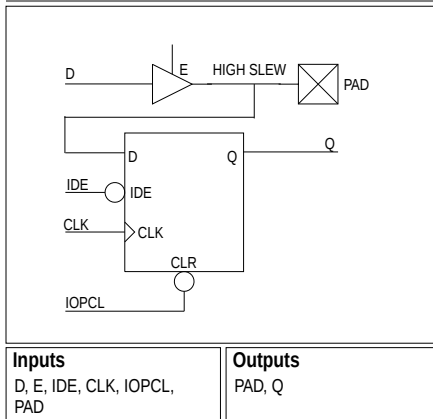
BBUFTL**Function**

Bidirectional Buffer, Tristate Enable, Low Slew

Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTH**Function**

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

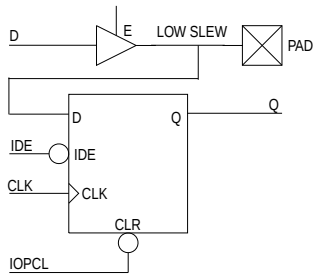
Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BIECTL

**Function**

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Inputs

D, E, IDE, CLK, IOPCL,
PAD

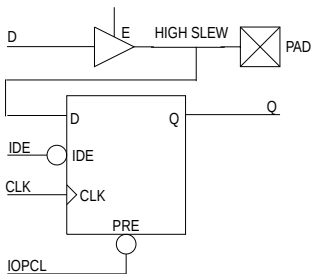
Outputs

PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BIEPTH

**Function**

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Inputs

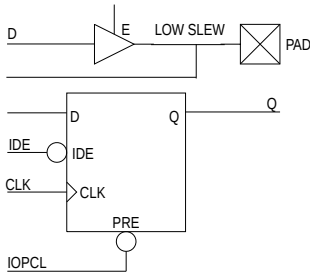
D, E, IDE, CLK, IOPCL,
PAD

Outputs

PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPTL

**Function**

Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q _{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q _{n-1}

Inputs

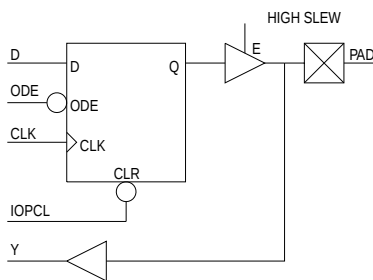
D, E, IDE, CLK, IOPCL,
PAD

Outputs

PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BRECHT

**Function**

Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Inputs

CLK, D, ODE, IOPCL, E,
PAD

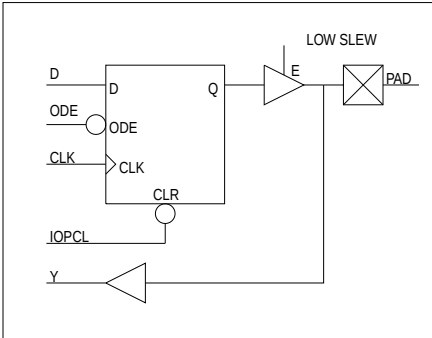
Outputs

PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BRECTL

**Inputs**CLK, D, ODE, IOPCL, E,
PAD**Outputs**

PAD, Y

Function

Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

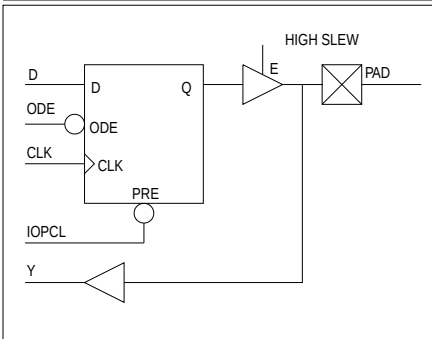
Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BREPTH

**Inputs**CLK, D, ODE, IOPCL, E,
PAD**Outputs**

PAD, Y

Function

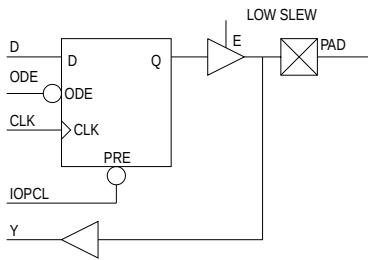
Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTL

**Function**

Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD _{n-1}	Y _{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Inputs

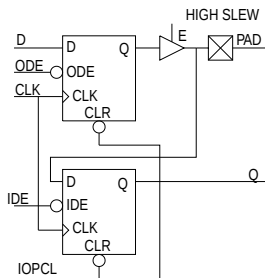
CLK, D, ODE, IOPCL, E, PAD

Outputs

PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

DECETH

**Function**

Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q _{n-1}

Inputs

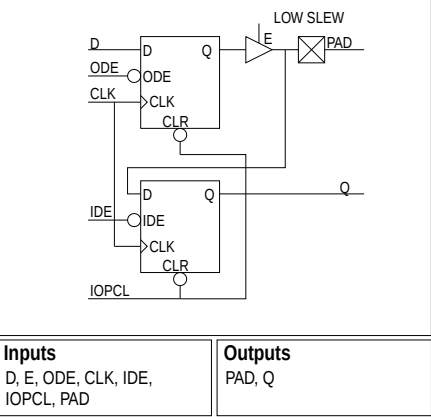
D, E, ODE, CLK, IDE, IOPCL, PAD

Outputs

PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

DECETL

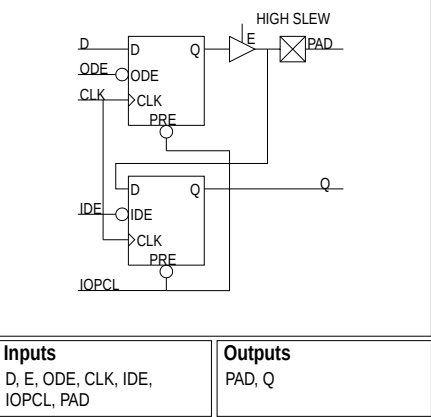


Function
Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Truth Table							
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETH

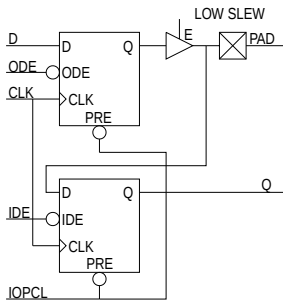


Function
Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Truth Table							
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETL



Inputs
D, E, ODE, CLK, IDE,
IOPLC, PAD

Outputs
PAD, Q

Function

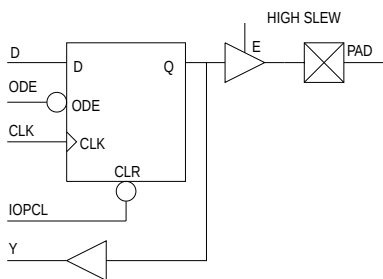
Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Truth Table

MODE	E	IOPLC	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD _{n-1}	Q _{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q _{n-1}

Family	Modules	
	Seq	I/O
ACT 3		1

FECTH



Inputs
D, E, ODE, CLK, IOPLC,
PAD

Outputs
PAD, Y

Function

Output Register with feedback, Clear, Output Data Enable, Tristate Enable, High Slew

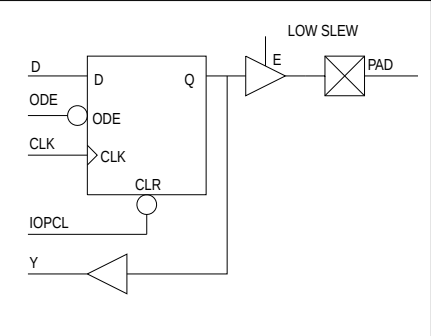
Truth Table

E	IOPLC	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y _{n-1}	Y _{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y _{n-1}	Z

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FECTL



Function
Output Register with feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

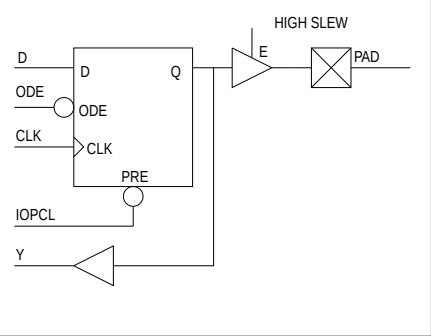
Truth Table					
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Inputs	Outputs
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FEPTH



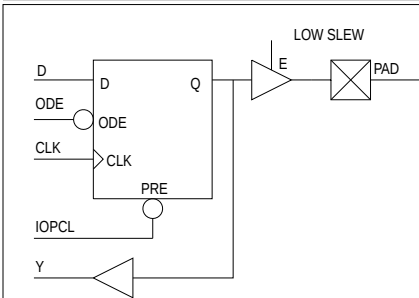
Function
Output Register with feedback, Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table					
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Inputs	Outputs
D, E, ODE, CLK, IOPCL, PAD	PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTL

**Function**

Output Register with feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Inputs

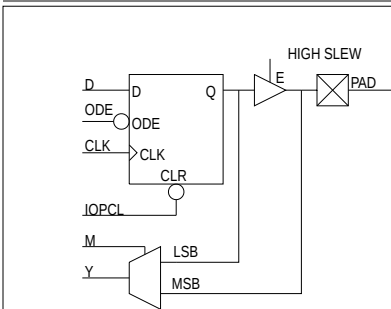
D, E, ODE, CLK, IOPCL, PAD

Outputs

PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

FECTMH

**Function**

Output Register with Muxed Feedback, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

Inputs

D, E, ODE, CLK, IOPCL, PAD, M

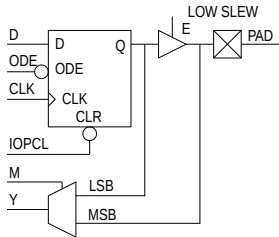
Outputs

PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FECTML

**Inputs**D, E, ODE, CLK, IOPCL,
PAD, M**Outputs**

PAD, Y

FunctionOutput Register with Muxed Feedback, with Clear, Output Data Enable,
Tristate Enable, Low Slew**Truth Table**

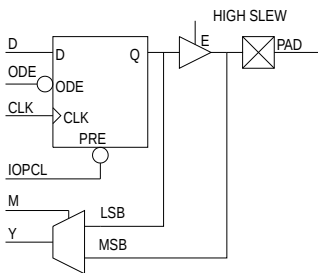
MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FEPTMH

**Inputs**D, E, ODE, CLK, IOPCL,
PAD, M**Outputs**

PAD, Y

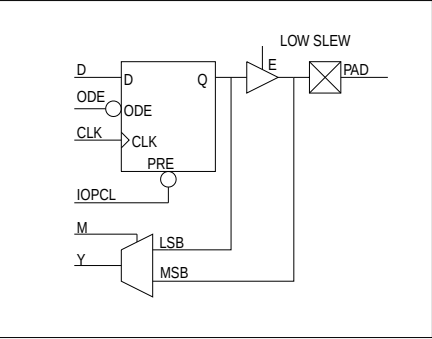
FunctionOutput Register with Muxed Feedback, with Preset, Output Data Enable,
Tristate Enable, High Slew**Truth Table**

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTML



Function
Output Register with Muxed Feedback, with Preset, Output Data Enable, Tristate Enable, Low Slew

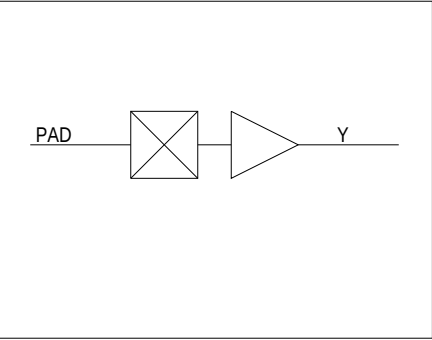
Truth Table							
MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD _{n-1}	X	Y _{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

Inputs	Outputs
D, E, ODE, CLK, IOPCL, PAD, M	PAD, Y

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

Family	Modules	
	Seq	I/O
ACT 3		1

IBUF



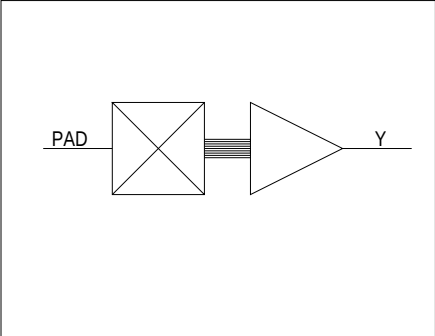
Function
Input Buffer

Truth Table	
PAD	Y
0	0
1	1

Inputs	Outputs
PAD	Y

Family	Modules	
	Seq	I/O
ACT 3		1

IOCLKBUF



Function
Dedicated I/O Module Clock Buffer

Truth Table

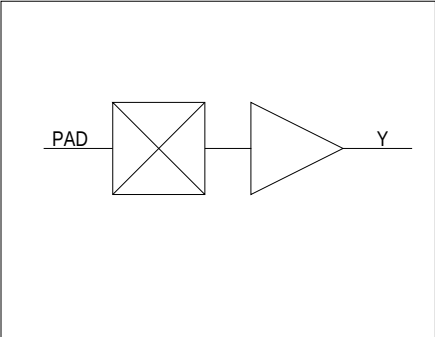
PAD	Y
0	0
1	1

Inputs	Outputs
PAD	Y

NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
ACT 3		1

IOPCLBUF



Function
Dedicated I/O Preset Clear Buffer

Truth Table

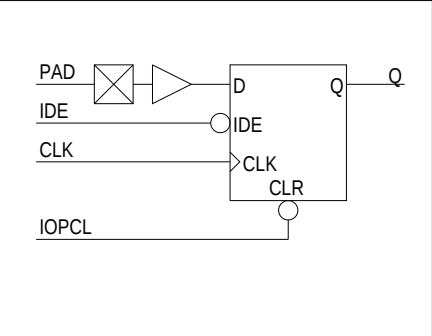
PAD	Y
0	0
1	1

Inputs	Outputs
PAD	Y

NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
ACT 3		1

IREC



Function
Input Register, with Clear, Input Data Enable

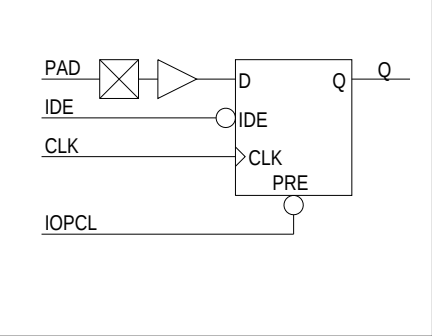
Truth Table

IOPCL	IDE	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	$\uparrow$	PAD

Inputs	Outputs
PAD, IDE, CLK, IOPCL	Q

Family	Modules	
	Seq	I/O
ACT 3		1

IREP



Function
Input Register, with Preset, Input Data Enable

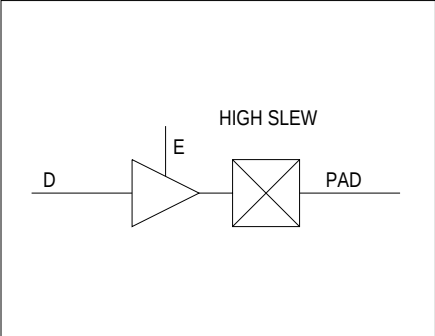
Truth Table

IOPCL	IDE	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	$\uparrow$	PAD

Inputs	Outputs
PAD, IDE, CLK, IOPCL	Q

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTH



Function
Output Buffer, Tristate Enable, High Slew

Truth Table

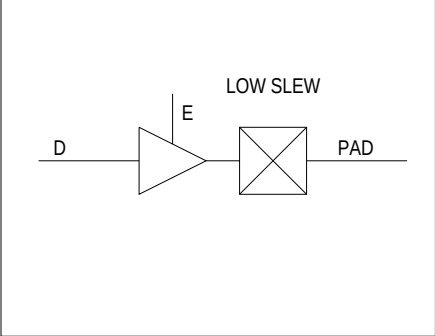
D	E	PAD
X	0	Z
0	1	0
1	1	1

Inputs
D, E

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OBUFTL



Function
Output Buffer, Tristate Enable, Low Slew

Truth Table

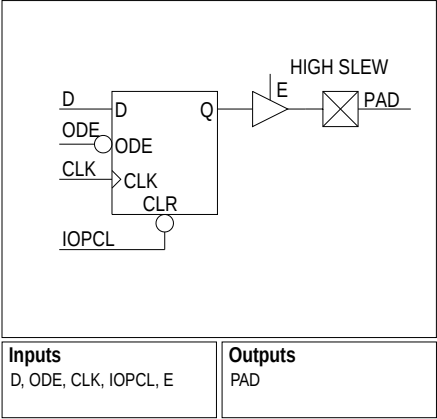
D	E	PAD
X	0	Z
0	1	0
1	1	1

Inputs
D, E

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTH



Function
Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

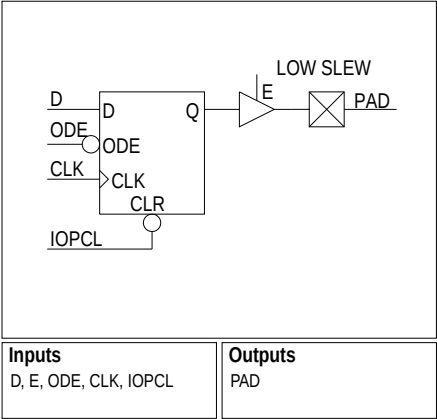
Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Inputs	Outputs
D, ODE, CLK, IOPCL, E	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTL



Function
Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

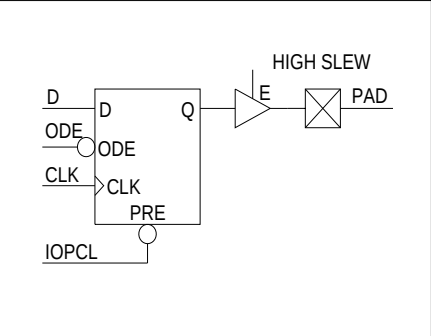
Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Inputs	Outputs
D, E, ODE, CLK, IOPCL	PAD

Family	Modules	
	Seq	I/O
ACT 3		1

OREPTH



Function
Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

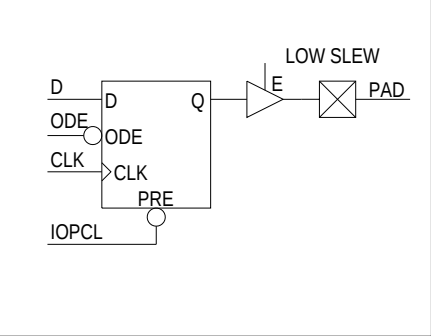
Truth Table

IOPL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Inputs D, E, ODE, CLK, IOPL	Outputs PAD
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	Modules	
Family	Seq	I/O
ACT 3		1

OREPTL



Function
Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

IOPL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Inputs D, E, ODE, CLK, IOPL	Outputs PAD
---------------------------------------	-----------------------

	Modules	
Family	Seq	I/O
ACT 3		1