Macro Library Guide

June 1998

Actel

Actel Corporation, Sunnyvale, CA 94086

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Introduction

Definitions

Hard Macros

The Hard Macro library consists of logic elements constructed of one or more ACT family modules. Modules may be of type sequential or combinatorial. Please refer to the ACT Family Field Programmable Gate Array Databook for definitions of ACT family modules. The relative placement of two module-macros is predefined. The timing characteristics are a function of the fanout on the output of the macro.

ACTgen Macro

ACTgen macros are described in Actel's publication, "A Guide to ACTgen Macros."

Combinability

For information on combinability, refer to the *Designer Series Development Tool User's Guide.*

How to Use this Guide

Family Inclusion Indicator

On the side of each data page are tabs indicating whether the cell is a member of the ACT 1, ACT 2/1200XL, 3200DX, ACT 3, 40MX, 42MX, or 54SX library.

Guidelines

These Guidelines are applicable to Hard macros only.

1. All input pin loading is assumed to be a single load except macros that are built using two combinational modules or one sequential and one combinatorial module. These macros are assumed to have a load of two on some of their input pins.

2. All macros have output pin loading of zero except for the sequential macros that are built using two combinational modules only. These macros have an output pin loading of one.

3. All hard macros have logic levels equal to one except cells with pin delays of two. A "2" is added to the corresponding symbol in the Hard Macro section of this manual.

Truth Table Nomenclature

Truth tables are arranged with *Inputs* before *Outputs*. The following symbol definitions apply.

↑	denotes rising edge clock
↓	denotes falling edge clock
X	in an input column denotes a 'don't care' or logic simulation state 'unknown'
!Q	denotes Q not

Pin Delay Annotation

Two-module combinatorial macros contain extra delay on some or all of the pins. If a macro symbol in this guide displays a "2" on a pin, then two levels of logic delay exist on the input to output path.

Note: Many two-level logic functions in one family are implemented in a single module in another family, hence the "2" may apply to specific families only.

Restrictions

Special I/Os

Some I/O pins are able to connect to global control signals such as clock or clear. These I/O pins may be used as "normal" data input/output buffers or they may be used as "special" pins. The following constraints apply to I/O pins used as "special" pins.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX register cells may be clocked by either of the two global clock networks by connecting their CLK input to the output of a CLKBUF, CLKBIBUF, or CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX register cells may be globally preset, reset or enabled by connecting the PRE, CLR, or E input to the output of a CLKBUF, CLKBIBUF, CLKINT macro.

All ACT 2/1200XL, 3200DX, ACT 3, 42MX, and 54SX I/O three-state buffers may be globally enabled by connecting their E input to the output of a CLKBUF, CLKBIBUF, OR CLKINT macro.

All ACT 3 and 54SX register cells composed of sequential modules may be clocked by high speed clock buffer network by connecting their CLK input to the output of a HCLKBUF macro.

ACT 3 registered I/O macros may *only* be clocked by the IOCLKBUF macro.

ACT 3 registered I/O macros may *only* be asynchronously set or preset by the IOPCL macro.

Advanced Application Notes

For Advanced Application notes, please refer to Actel's *Databook.*

HDL Instantiation of Macros

Individual macros can be instantiated in your Verilog or VHDL Code.

In Verilog, an instantiation is performed within a module with the following syntax:

```
macro_name instance_name
(.macro_pin_name(net_name), ...);
```

For example, an instantiation of an AND3 macro could be entered as:

```
AND3 U12 (.A(SIG1), .B(SIG2), .C(SIG3),
.Y(SIG4));
```

In VHDL, an instantiation is performed within an architecture with the following syntax:

```
instance_name: macro_name PORT MAP
(macro_pin_name=>signal_name, ...);
```

For example, an instantiation of an AND3 macro could be entered as:

```
U12: AND3 PORT MAP (A=>SIG1, B=>SIG2,
C=>SIG3, Y=>SIG4);
```

In either language, connection by name rather than by position is shown and is the recommended practice.

Migration Between Families

Actel provides the capability of migrating a netlist created for one family to another family in some cases. Macros listed in this manual as being available in the old family will not be shown as available in the new family when the new macro is inefficient or when the function can be better implemented with different macros, however, the macro may be available in the new family. Such macros are not recommended for new designs.

In all cases, if an HDL description is available, it is best to resynthesize, targeting the new family.

If an HDL description is not available, it is still generally best to do gate level retargeting to the new family.

If neither of the above is done, a netlist created for one family may be used in another family as follows: No special procedures are needed to use the netlist in Designer, but a migration library must be enabled in CAE environments as explained in individual CAE interface guides.

	Target Family			
Original Family	**ACT 1/40MX**	**ACT 2/1200XL/ 3200DX/42MX**	**ACT 3**	**54SX**
ACT 1 or 40MX	X	YES	YES	NO
ACT 2, 1200XL, 3200DX, 42MX	NO	X	YES**	YES**
ACT 3	NO	NO	X	YES*
54SX	NO	NO	NO	X

* Except registered I/O, IOCLK, and IOPCL

** Except QCLK and RAM

Hard Combinational Macros

Hard Sequential Macros

CC-Module Flip Flops

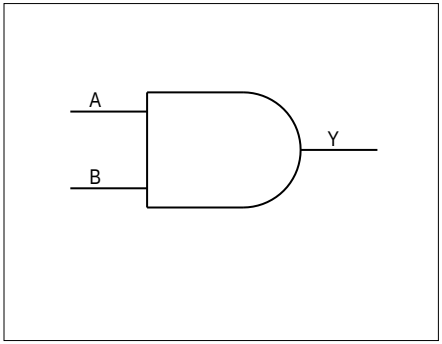
RAM Macros

I/O Macros

Alphabetical List of Macros

Hard Macros

AND2



Function
2 Input AND

Truth Table

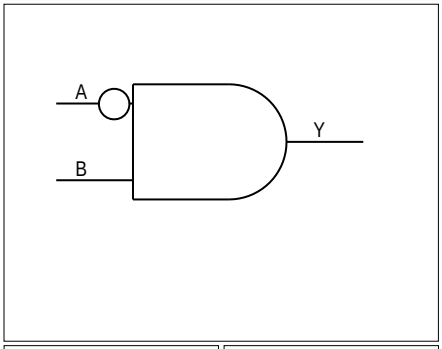
A	B	Y
X	0	0
0	X	0
1	1	1

Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AND2A



Function
2 Input AND with active low A-Input

Truth Table

A	B	Y
X	0	0
0	1	1
1	X	0

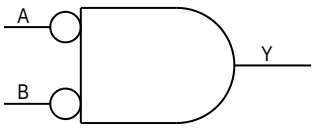
Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AND2B



Function
2 Input AND with active low Inputs

Truth Table

A	B	Y
0	0	1
X	1	0
1	X	0

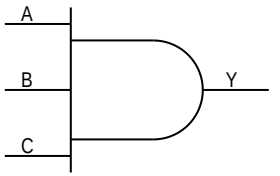
Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AND3



Function
3 Input AND

Truth Table

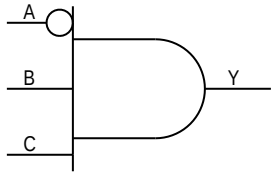
A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AND3A



Function
3 Input AND with active low A-Input

Truth Table

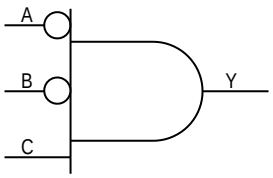
A	B	C	Y
X	X	0	0
X	0	X	0
0	1	1	1
1	X	X	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AND3B



Function
3 Input AND with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
X	1	X	0
1	X	X	0

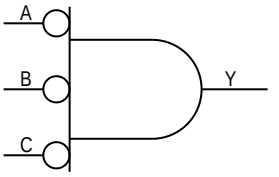
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AND3C



Function
3 Input AND with active low Inputs

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

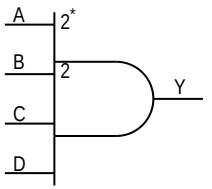
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AND4



Function
4 Input AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

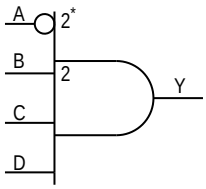
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1/40MX.

AND4A



Function
4 Input AND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	1	1	1	1
1	X	X	X	0

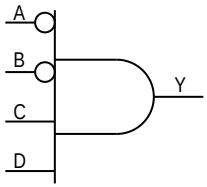
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

AND4B



Function
4 Input AND with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	1	1	1
X	1	X	X	0
1	X	X	X	0

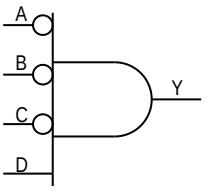
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AND4C



Function
4 Input AND with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	1	1
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

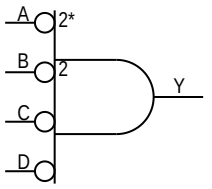
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AND4D



Function
4 Input AND with active low Inputs

Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

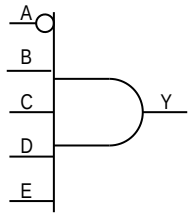
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except 54SX.

AND5A



Function

5 Input AND with active low A input

Truth Table

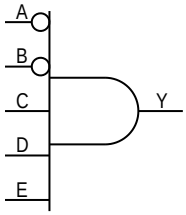
A	B	C	D	E	Y
0	1	1	1	1	1
1	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AND5B



Function

5 Input AND with active low A- and B-Inputs

Truth Table

A	B	C	D	E	Y
X	X	X	X	0	0
X	X	X	0	X	0
X	X	0	X	X	0
0	0	1	1	1	1
X	1	X	X	X	0
1	X	X	X	X	0

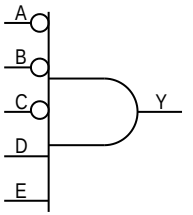
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

54SX

AND5C



Function
5 Input AND with active low A-, B-, and C-inputs

Truth Table

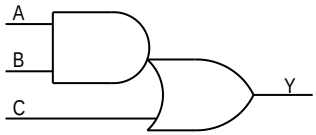
A	B	C	D	E	Y
0	0	0	1	1	1
1	X	X	X	X	0
X	1	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AO1



Function
3 Input AND-OR

Truth Table

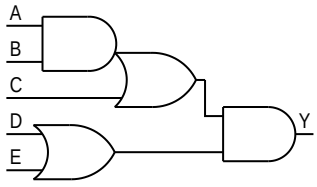
A	B	C	Y
X	0	0	0
X	X	1	1
0	X	0	0
1	1	X	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO10



Function
5 Input AND-OR-AND

Truth Table

A	B	C	D	E	Y
X	X	X	0	0	0
X	0	0	X	X	0
X	X	1	X	1	1
X	X	1	1	X	1
0	X	0	X	X	0
1	1	X	X	1	1
1	1	X	1	X	1

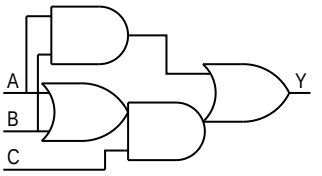
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO11



Function
3 Input AND-OR

Truth Table

A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

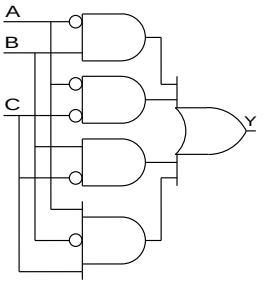
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

54SX

AO12



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

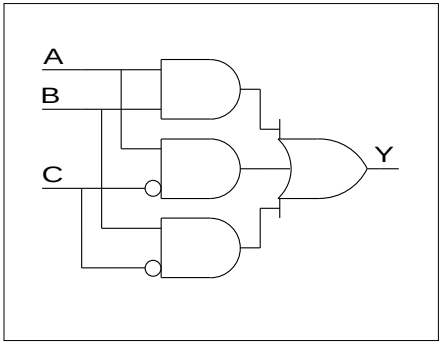
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AO13

54SX



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

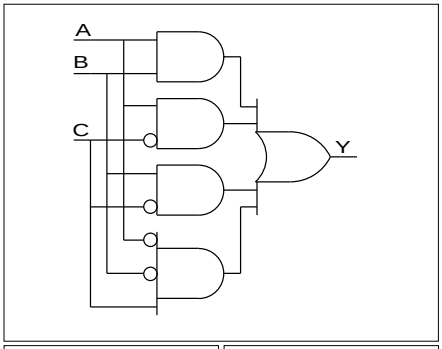
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AO14

54SX



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

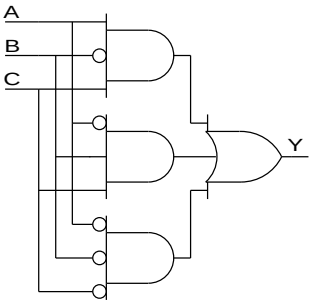
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AO15



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

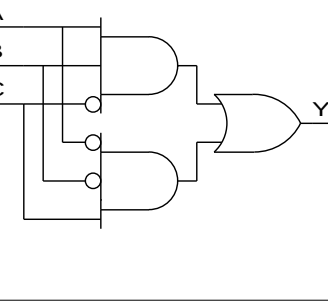
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AO16



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

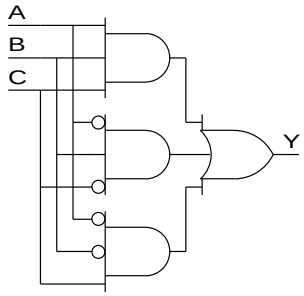
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AO17

54SX



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

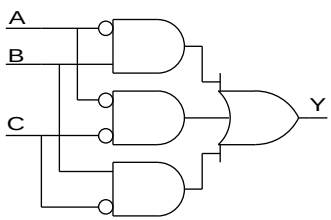
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AO18

54SX



Function
3 Input AND-OR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

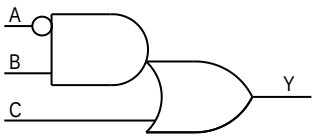
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AO1A



Function
3 Input AND-OR with active low A-Input

A	B	C	Y
X	0	0	0
X	X	1	1
0	1	X	1
1	X	0	0

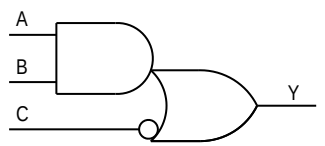
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AO1B



Function
3 Input AND-OR with active low C-Input

Truth Table

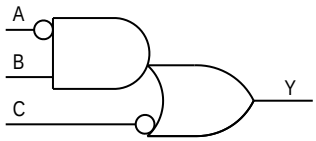
A	B	C	Y
X	X	0	1
X	0	1	0
0	X	1	0
1	1	X	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO1C



Function
3 Input AND-OR with active low A- and C-Inputs

Truth Table

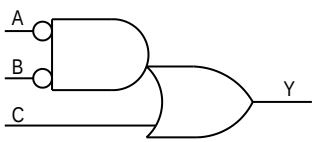
A	B	C	Y
X	X	0	1
X	0	1	0
0	1	X	1
1	X	1	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO1D



Function
3 Input AND-OR with active low A- and B-Inputs

Truth Table

A	B	C	Y
0	0	X	1
X	1	0	0
X	X	1	1
1	X	0	0

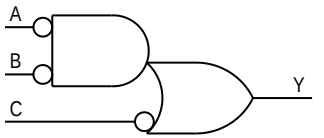
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO1E



Function
3 Input AND-OR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

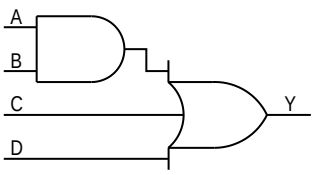
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AO2



Function
4 Input AND-OR

Truth Table

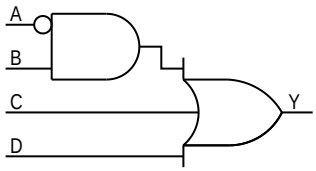
A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	X	0	0	0
1	1	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO2A



Function
4 Input AND-OR with active low A-Input

Truth Table

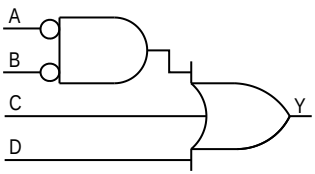
A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
X	X	1	X	1
0	1	X	X	1
1	X	0	0	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO2B



Function
4 Input AND-OR with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

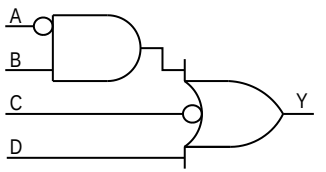
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO2C



Function
4 Input AND-OR with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
1	X	1	0	0
X	0	1	0	0
0	1	X	X	1
X	X	0	X	1
X	X	X	1	1

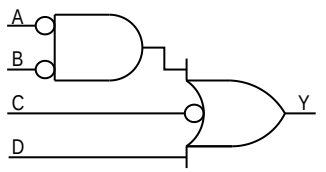
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO2D



Function
4 Input AND-OR with active low A-, B- and C-Inputs

Truth Table

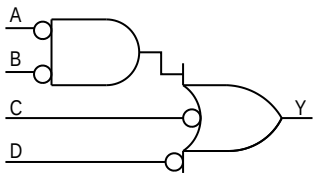
A	B	C	D	Y
X	X	0	X	1
0	0	X	X	1
X	1	1	0	0
X	X	X	1	1
1	X	1	0	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO2E



Function
4 Input AND-OR with active low Inputs

Truth Table

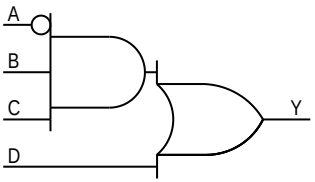
A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO3



Function
4 Input AND-OR with active low A Input

Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	1	1	X	1
1	X	X	0	0

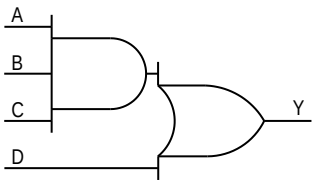
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO3A



Function
4 Input AND-OR

Truth Table

A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
X	0	X	0	0
0	X	X	0	0
1	1	1	X	1

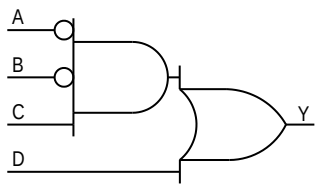
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO3B



Function
4 Input AND-OR with active low A-, B- Inputs

Truth Table

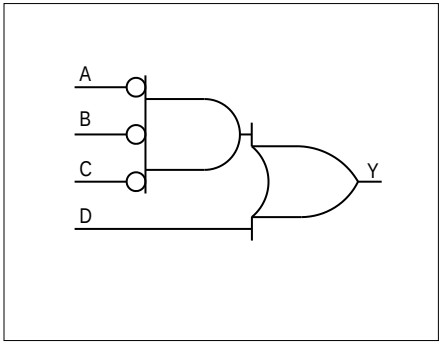
A	B	C	D	Y
X	X	0	0	0
X	X	X	1	1
0	0	1	X	1
X	1	X	0	0
1	X	X	0	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO3C



Function
4 Input AND-OR with active low A-, B-, C- Inputs

Truth Table

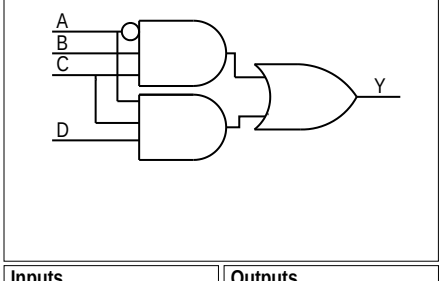
A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO4A



Function
4 Input AND-OR

Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	X	0	0
0	0	X	X	0
0	1	1	X	1
1	X	1	1	1
1	X	X	0	0
X	1	1	1	1

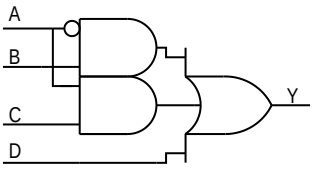
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AO5A



Function
4 Input AND-OR

Truth Table

A	B	C	D	Y
X	0	0	0	0
X	X	X	1	1
0	0	X	0	0
0	1	X	X	1
1	X	1	X	1
1	X	0	0	0
X	1	1	X	1

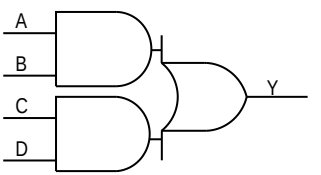
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO6



Function
2-wide 4-Inputs AND-OR

Truth Table

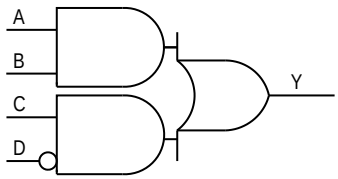
A	B	C	D	Y
X	0	X	0	0
X	0	0	X	0
X	X	1	1	1
0	X	X	0	0
0	X	0	X	0
1	1	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO6A



Function
2-wide 4-Inputs AND-OR with active low D-Input

Truth Table

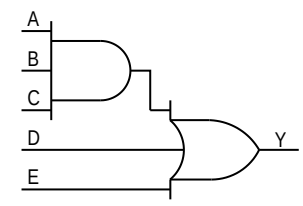
A	B	C	D	Y
X	0	0	X	0
X	X	1	0	1
X	0	X	1	0
0	X	0	X	0
0	X	X	1	0
1	1	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AO7



Function
5 Input AND-OR

A	B	C	D	E	Y
X	X	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	0	X	0	0	0
0	X	X	0	0	0
1	1	1	X	X	1

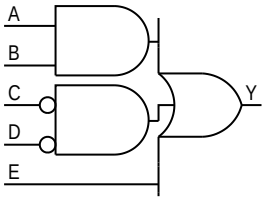
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO8



Function
5 Input AND-OR with active low C- and D-Inputs

Truth Table

A	B	C	D	E	Y
X	X	0	0	X	1
X	0	X	1	0	0
X	X	X	X	1	1
X	0	1	X	0	0
0	X	X	1	0	0
0	X	1	X	0	0
1	1	X	X	X	1

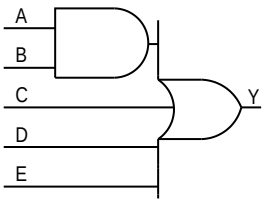
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AO9



Function
5 Input AND-OR

Truth Table

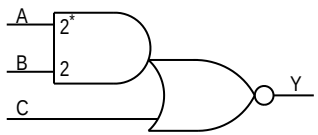
A	B	C	D	E	Y
X	0	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
0	X	0	0	0	0
1	1	X	X	X	1

Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AOI1



Function
3 Input AND-OR-INVERT

Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	X	0	1
1	1	X	0

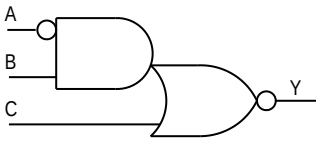
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

AOI1A



Function
3 Input AND-OR-INVERT with active low A-Input

Truth Table

A	B	C	Y
X	0	0	1
X	X	1	0
0	1	X	0
1	X	0	1

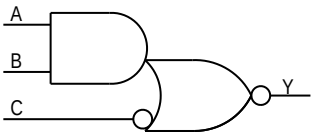
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AOI1B



Function
3 Input AND-OR-INVERT with active low C-Input

Truth Table

A	B	C	Y
X	X	0	0
X	0	1	1
0	X	1	1
1	1	X	0

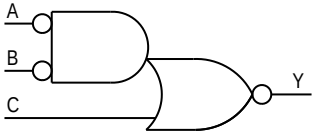
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AOI1C



Function
3 Input AND-OR-INVERT with active low A- and B-Inputs

Truth Table

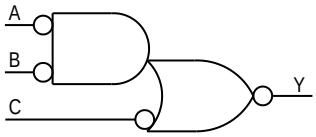
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AOI1D



Function
3 Input AND-OR-INVERT with active low Inputs

Truth Table

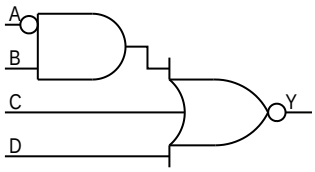
A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AOI2A



Function
4 Input AND-OR-INVERT with active low A-Input

Truth Table

A	B	C	D	Y
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
0	1	X	X	0
1	X	0	0	1

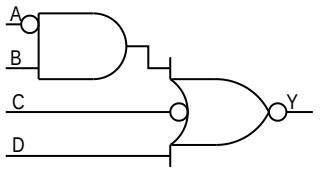
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AOI2B



Function
4 Input AND-OR-INVERT with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	1	0	1
X	X	X	1	0
0	1	X	X	0
1	X	1	0	1

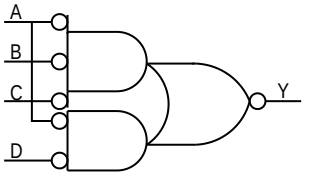
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AOI3A



Function
4 Input AND-OR-INVERT with active low Inputs

Truth Table

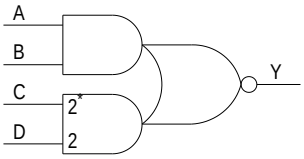
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AOI4



Function
2-wide 4-Inputs AND-OR-INVERT

Truth Table

A	B	C	D	Y
X	0	X	0	1
X	0	0	X	1
X	X	1	1	0
0	X	X	0	1
0	X	0	X	1
1	1	X	X	0

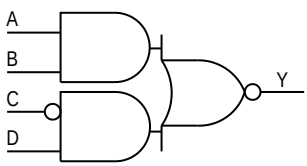
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except 54SX.

AOI4A



Function
2-wide 4-Inputs AND-OR-INVERT with active low C-Input

Truth Table

A	B	C	D	Y
X	0	X	0	1
X	X	0	1	0
X	0	1	X	1
0	X	X	0	1
0	X	1	X	1
1	1	X	X	0

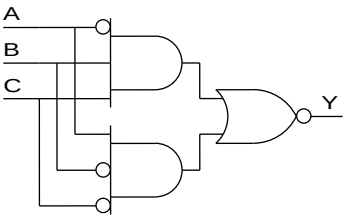
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

54SX

AOI5



Function
3-Input AND-OR-INVERT

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0

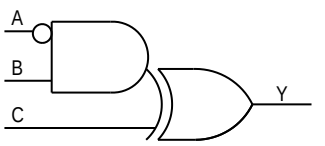
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

AX1



Function
3 Input AND-XOR with active low A-Input

Truth Table

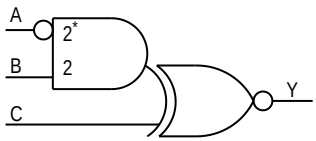
A	B	C	Y
X	0	0	0
X	0	1	1
0	1	0	1
0	1	1	0
1	X	0	0
1	X	1	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

AX1A



Function
3 Input AND-XOR-INVERT with active low A-Input

Truth Table

A	B	C	Y
X	0	0	1
X	0	1	0
0	1	0	0
0	1	1	1
1	X	0	1
1	X	1	0

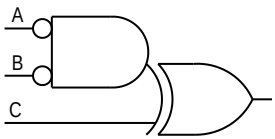
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX/54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays for all families except ACT 1, 40MX, and 54SX.

AX1B



Function
3 Input AND-XOR with active low A- and B-Inputs

Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
X	1	0	0
X	1	1	1
1	X	0	0
1	X	1	1

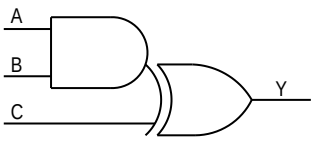
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

AX1C



Function
3 Input AND-XOR

Truth Table

A	B	C	Y
X	0	0	0
X	0	1	1
0	X	0	0
0	X	1	1
1	1	0	1
1	1	1	0

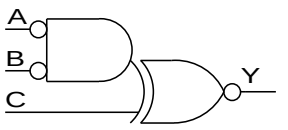
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

54SX

AX1D



Function
3 Input AND-XOR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	0

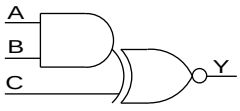
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AX1E

54SX



Function
3 Input AND-XNOR

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

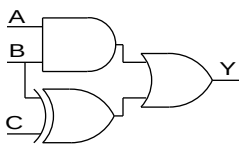
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXO1

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

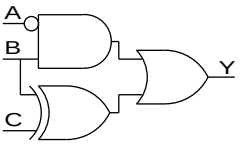
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXO2



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

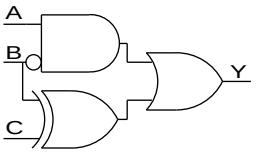
Inputs
A,. B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXO3



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

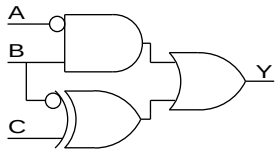
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXO5

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

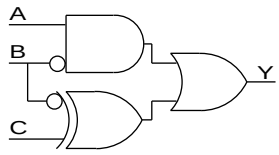
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXO6

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

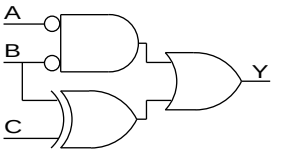
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXO7



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

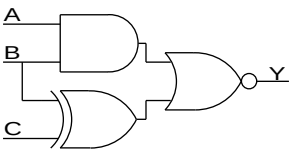
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXOI1



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	0

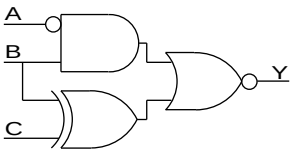
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI2

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

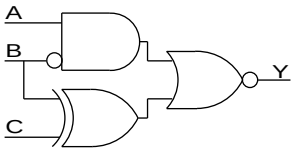
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI3

54SX



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

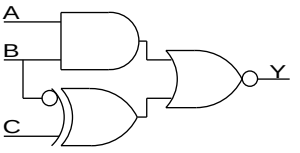
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXOI4



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

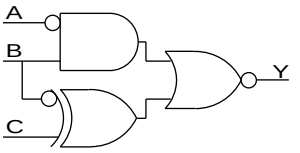
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

AXOI5



Function
3-Input Gate

Truth Table

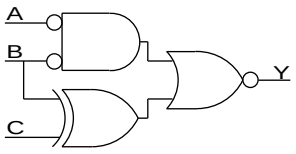
A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

AXOI7



Function
3-Input Gate

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	1
1	1	1	1

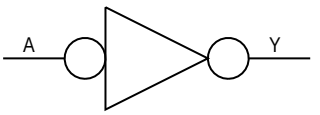
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

BUFA



Function
Buffer, with active low Input and Output

Truth Table

A	Y
0	0
1	1

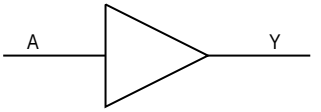
Inputs
A

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

BUFF



Function
Buffer

Truth Table

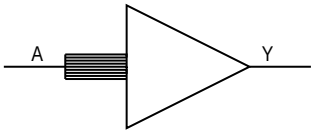
A	Y
0	0
1	1

Inputs
A

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

CLKINT



Function
Internal Clock Interface

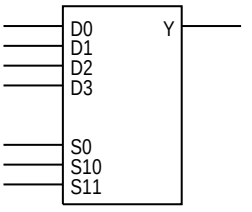
A	Y
0	0
1	1

Inputs
A

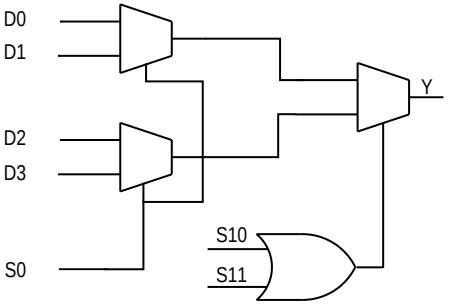
Outputs
Y

NOTE: CLKINT does not use any modules.
For more information on the Global Clock Network, refer to Actel's Databook.

CM7



Function
Full Combinational Module



Inputs
D0, D1, D2, D3, S0, S10, S11

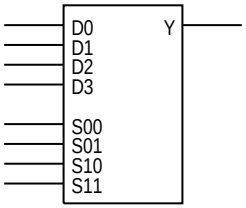
Outputs
Y

Truth Table

S11	S10	S0	Y
0	0	0	D0
0	0	1	D1
X	1	0	D2
1	X	0	D2
X	1	1	D3
1	X	1	D3

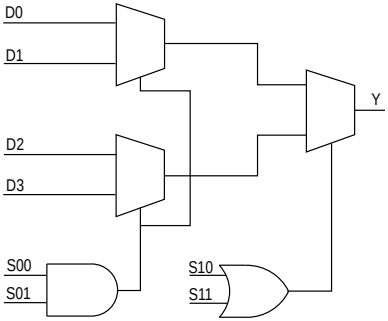
Family	Modules	
	Seq	Comb
All		1

CM8



Function

Full Combinational Module



Inputs

D0, D1, D2, D3, S00, S01, S10, S11

Outputs

Y

Truth Table

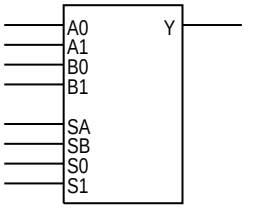
S11	S10	S01	S00	Y
0	0	X	0	D0
0	0	0	X	D0
0	0	1	1	D1
X	1	X	0	D2
X	1	0	X	D2
1	X	X	0	D2
1	X	0	X	D2
X	1	1	1	D3
1	X	1	1	D3

Family	Modules	
	Seq	Comb
All		1

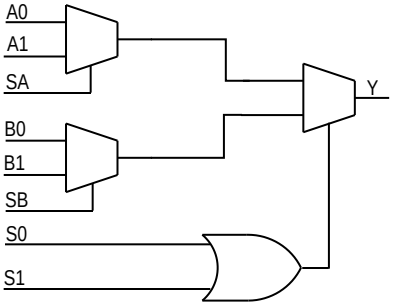
ACT 1

40MX

CM8A



Function
Full Combinational Module



Inputs
A0, A1, B0, B1, SA, SB, S0, S1

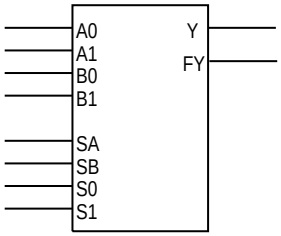
Outputs
Y

Truth Table

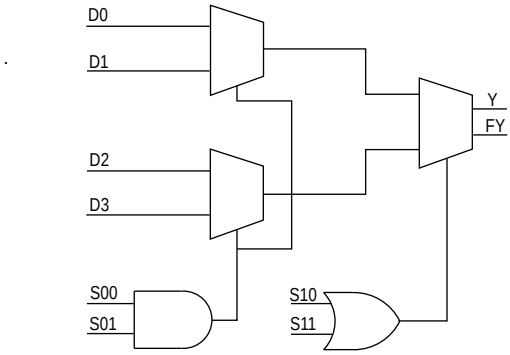
S0	S1	SA	SB	Y
0	0	0	X	A0
0	0	1	X	A1
1	X	X	0	B0
X	1	X	0	B0
1	X	X	1	B1
X	1	X	1	B1

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

CM8F



Function
Full Combinational Module with fast output



Inputs
D0, D1, D2, D3, S00, S01, S10, S11

Outputs
Y, FY

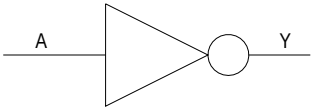
Truth Table

S11	S10	S01	S00	Y	FY
0	0	X	0	D0	D0
0	0	0	X	D0	D0
0	0	1	1	D1	D1
X	1	X	0	D2	D2
X	1	0	X	D2	D2
1	X	X	0	D2	D2
1	X	0	X	D2	D2
X	1	1	1	D3	D3
1	X	1	1	D3	D3

Family	Modules	
	Seq	Comb
54SX		1

NOTE: FY is a fast output that has a maximum fanout of 1.

CM8INV



Function
Inverter with active low output

Truth Table

A	Y
0	1
1	0

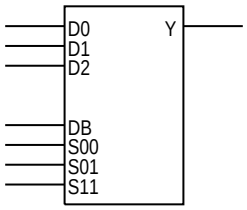
Inputs
A

Outputs
Y

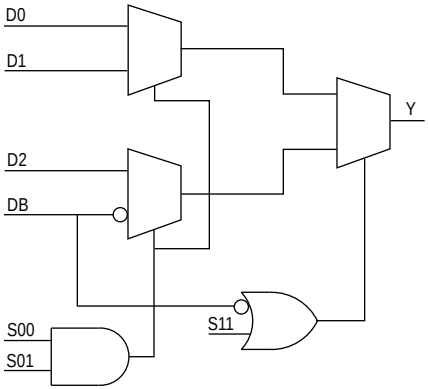
Family	Modules	
	Seq	Comb
54SX		0

NOTE: This macro can drive any number of CM8 pins and will be absorbed into that module

CMB7



Function
Full Combinational Module



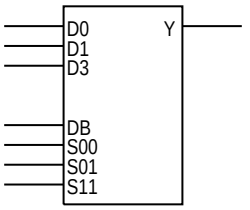
Inputs
D0, D1, D2, DB, S00, S01, S11

Outputs
Y

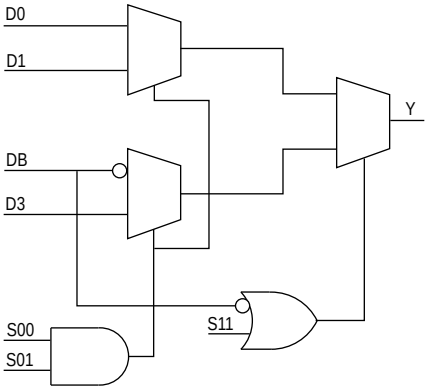
Family	Modules	
	Seq	Comb
54SX		1

54SX

CMBB



Function
Full Combinational Module

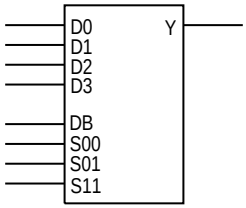


Inputs
D0, D1, D3, DB, S00, S01, S11

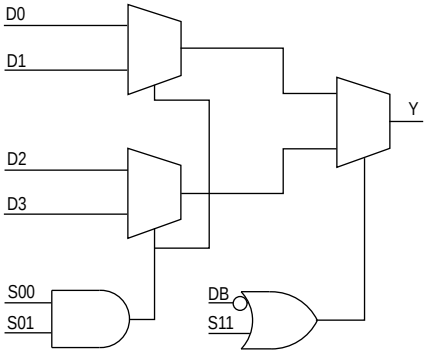
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMBF



Function
Full Combinational Module



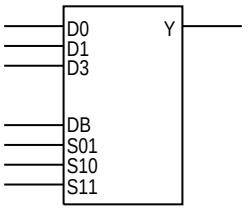
Inputs
D0, D1, D2, D3, DB, S00, S01, S11

Outputs
Y

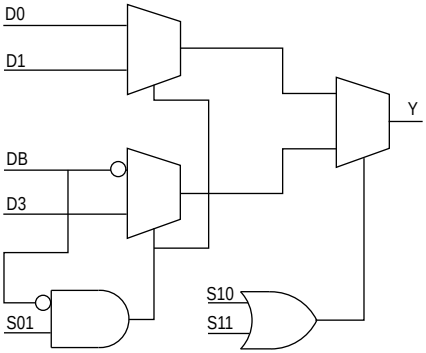
Family	Modules	
	Seq	Comb
54SX		1

54SX

CMEB



Function
Full Combinational Module

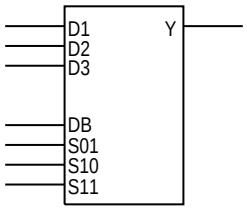


Inputs
D0, D1, D3, DB, S01, S10, S11

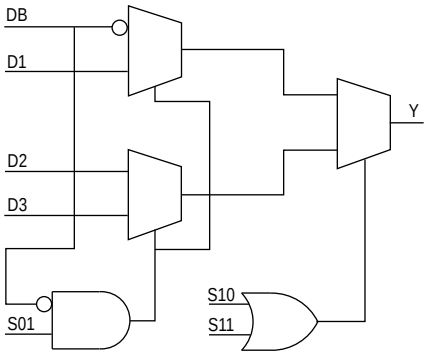
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMEE



Function
Full Combinational Module

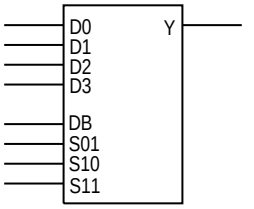


Inputs
D1, D2, D3, DB, S01, S10, S11

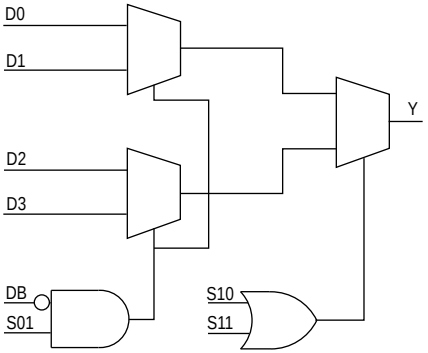
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMEF



Function
Full Combinational Module

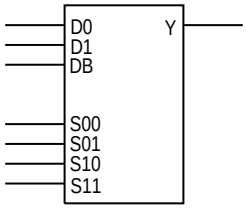


Inputs
D0, D1, D2, D3, DB, S01, S10, S11

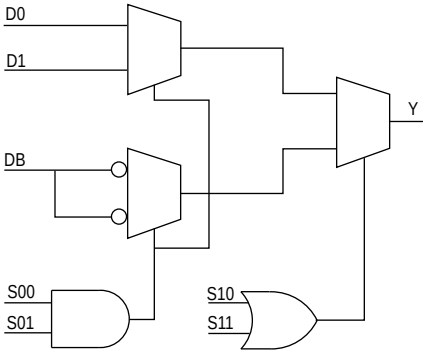
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMF3



Function
Full Combinational Module



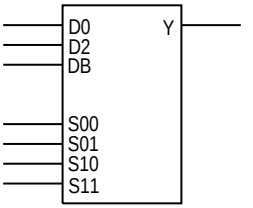
Inputs
D0, D1, DB, S00, S01, S10, S11

Outputs
Y

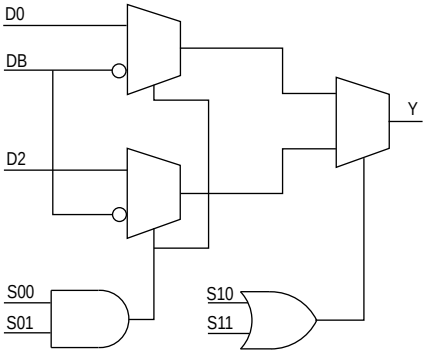
Family	Modules	
	Seq	Comb
54SX		1

54SX

CMF5



Function
Full Combinational Module

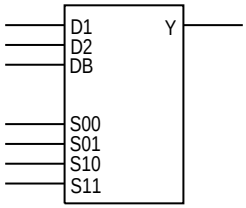


Inputs
D0, D2, DB, S00, S01, S10, S11

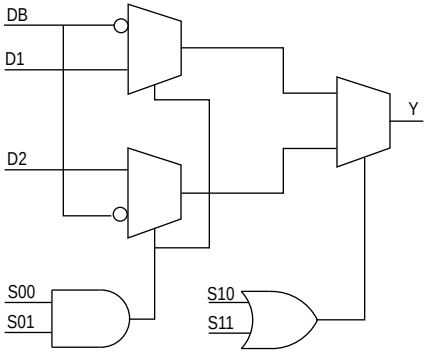
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMF6



Function
Full Combinational Module

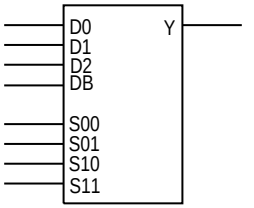


Inputs
D1, D2, DB, S00, S01, S10, S11

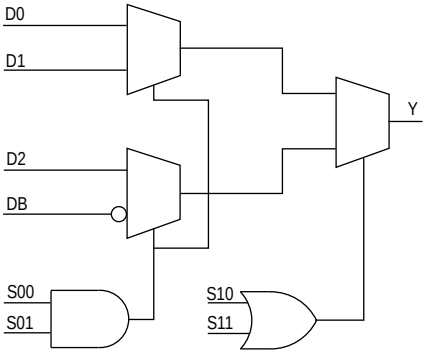
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMF7



Function
Full Combinational Module

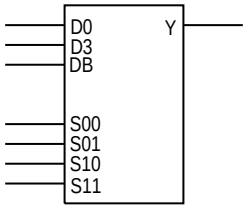


Inputs
D0, D1, D2, DB, S00, S01, S10, S11

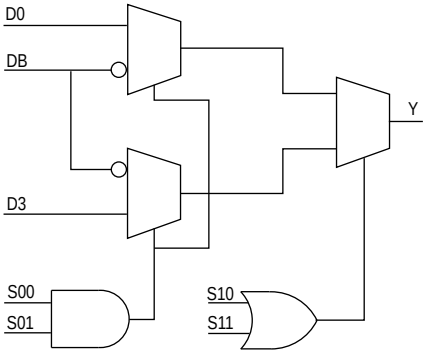
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMF9



Function
Full Combinational Module



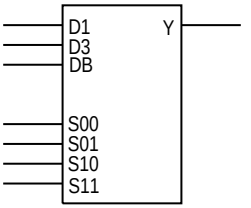
Inputs
D0, D3, DB, S00, S01, S10, S11

Outputs
Y

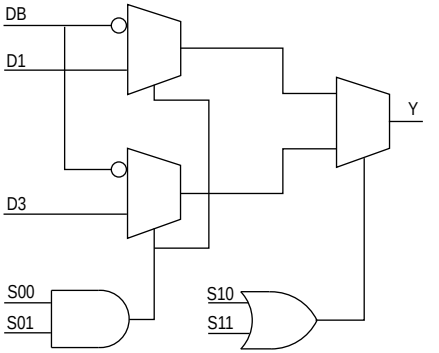
Family	Modules	
	Seq	Comb
54SX		1

54SX

CMFA



Function
Full Combinational Module

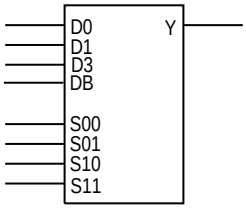


Inputs
D1, D3, DB, S00, S01, S10, S11

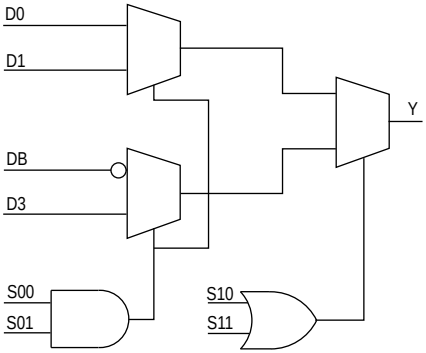
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMFB



Function
Full Combinational Module



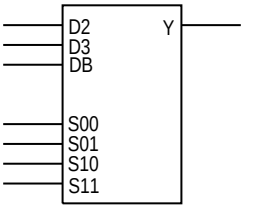
Inputs
D0, D1, D3, DB, S00, S01, S10, S11

Outputs
Y

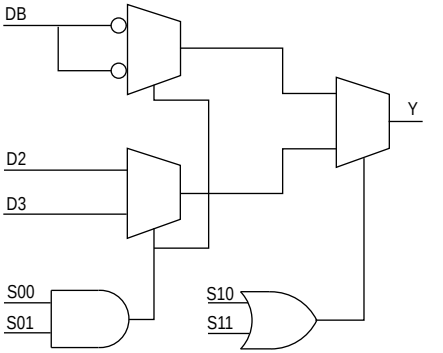
Family	Modules	
	Seq	Comb
54SX		1

54SX

CMFC



Function
Full Combinational Module

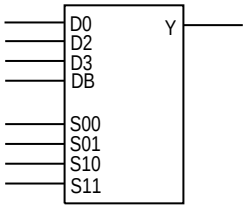


Inputs
D2, D3, DB, S00, S01, S10, S11

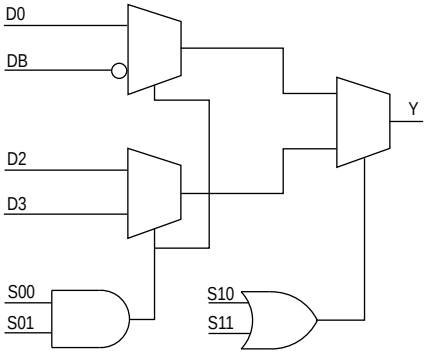
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMFD



Function
Full Combinational Module

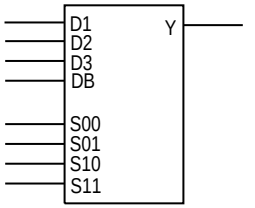


Inputs
D0, DB, D2, D3, S00, S01, S10, S11

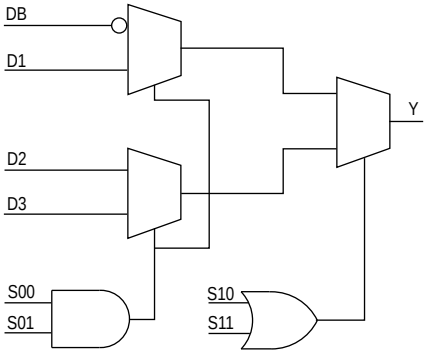
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CMFE



Function
Full Combinational Module

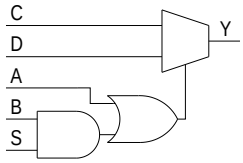


Inputs
D1, D2, D3, DB, S00, S01, S10, S11

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CS1



Function
Carry Select for Implementing High Speed Adders

Truth Table

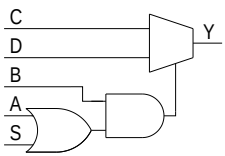
A	S	B	C	D	Y
X	X	X	0	0	0
0	X	0	0	X	0
0	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	X	X	1	1
1	X	X	X	0	0
X	X	X	1	1	1

Inputs
A, S, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

CS2



Function
Carry Select for Implementing High Speed Adders

Truth Table

A	S	B	C	D	Y
X	X	X	0	0	0
X	X	0	0	X	0
X	X	0	1	X	1
0	0	X	0	X	0
0	0	X	1	X	1
X	1	1	X	1	1
X	1	1	X	0	0
1	X	1	X	1	1
1	X	1	X	0	0
X	X	X	1	1	1

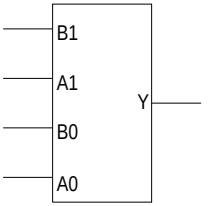
Inputs
A, S, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

CY2A



Function
Carry Generator

Truth Table

A1	B1	A0	B0	Y
X	0	X	0	0
X	0	0	X	0
0	0	X	X	0
0	X	X	0	0
0	X	0	X	0
X	1	1	1	1
1	X	1	1	1
1	1	X	X	1

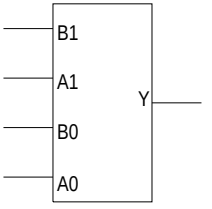
Inputs
A1, B1, A0, B0

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

CY2B



Function
Carry Generator

Truth Table

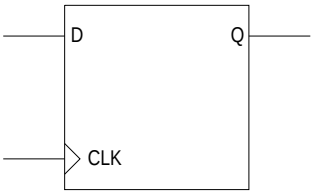
A1	B1	A0	B0	Y
X	0	0	0	0
0	0	X	X	0
0	X	0	0	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1
1	1	X	X	1

Inputs
A1, B1, A0, B0

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

DF1



Function
D-Type Flip-Flop

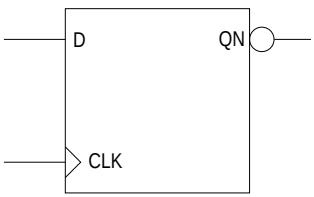
Truth Table

CLK	Q_{n+1}
↑	D

Inputs	Outputs
D, CLK	Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DF1A



Function
D-Type Flip-Flop with active low Output

Truth Table

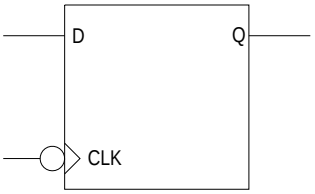
CLK	QN_{n+1}
↑	!D

Inputs	Outputs
D, CLK	QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DF1B



Function
D-Type Flip-Flop with active low Clock

Truth Table

CLK	Q_{n+1}
↓	D

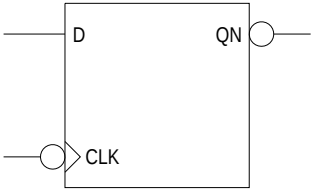
Inputs
D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DF1C



Function
D-Type Flip-Flop with active low Clock and Output

Truth Table

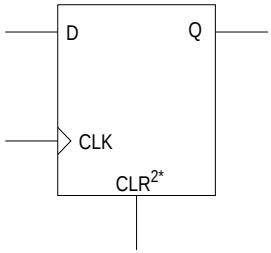
CLK	QN_{n+1}
↓	!D

Inputs
D, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFC1



Function
D-Type Flip-Flop, with active high Clear

Truth Table

CLR	CLK	Q_{n+1}
1	X	0
0	↑	D

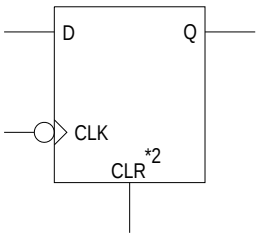
Inputs
CLR, D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

DFC1A



Function
D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

CLR	CLK	Q_{n+1}
1	X	0
0	↓	D

Inputs
CLR, D, CLK

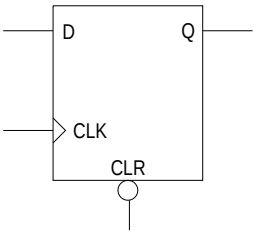
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT1 and 40MX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DFC1B



Function
D-Type Flip-Flop, with active low Clear

Truth Table

CLR	CLK	Q_{n+1}
0	X	0
1	↑	D

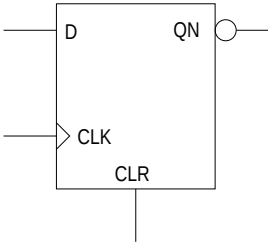
Inputs
CLR, D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
40MX

DFC1C



Function
D-Type Flip-Flop, with active high Clear and Clock

Truth Table

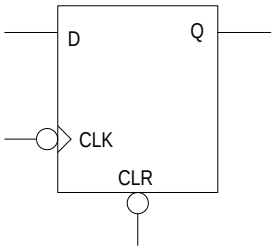
CLR	CLK	QN_{n+1}
1	X	1
0	↑	!D

Inputs
CLR, D, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFC1D



Function
D-Type Flip-Flop, with active low Clear and Clock

Truth Table

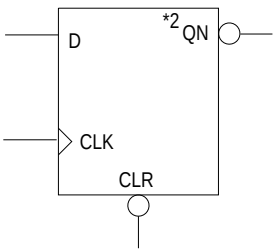
CLR	CLK	Q_{n+1}
0	X	0
1	↓	D

Inputs
CLR, D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFC1E



Function
D-Type Flip-Flop, with active low Clear and Output

Truth Table

CLR	CLK	QN_{n+1}
0	X	1
1	↑	!D

Inputs
CLR, D, CLK

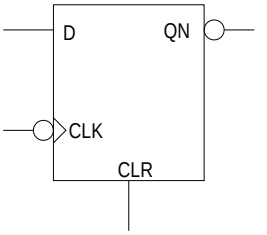
Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

ACT 1
40MX

DFC1F



Function
D-Type Flip-Flop, with active high Clear, active low Clock and Output

Truth Table

CLR	CLK	QN_{n+1}
1	X	1
0	↓	!D

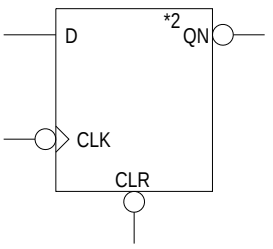
Inputs
CLR, D, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFC1G



Function
D-Type Flip-Flop, with active low Clear, Clock and Output

Truth Table

CLR	CLK	Q_{n+1}
0	X	1
1	↓	!D

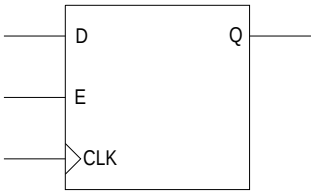
Inputs
CLR, D, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

A 2 on the symbol implies 2 logic module delays except for ACT1 and 40MX.

DFE



Function
D-Type Flip-Flop, with active high Enable

Truth Table

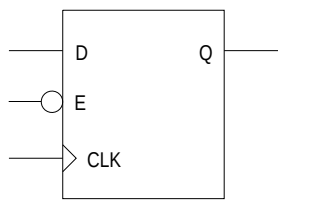
E	CLK	Q_{n+1}
0	X	Q
1	↑	D

Inputs
D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE1B



Function
D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↑	D

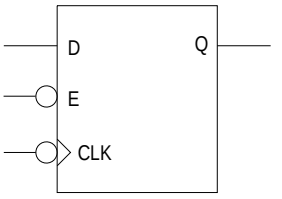
Inputs
D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DFE1C



Function
D-Type Flip-Flop, with active low Enable and Clock

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↓	D

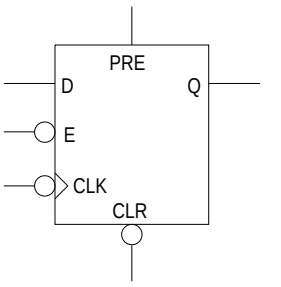
Inputs
D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
40MX

DFE2D



Function
D-Type Flip-Flop, with active high Preset, active low Enable, Clear, and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↓	D
0	1	X	X	*

Inputs
CLR, D, E, PRE, CLK

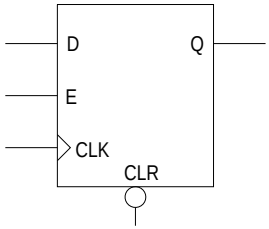
Outputs
Q

.

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFE3A



Function
D-Type Flip-Flop, with Enable and active low Clear

Truth Table

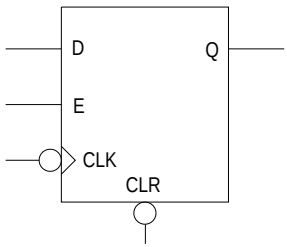
CLR	E	CLK	Q_{n+1}
0	X	X	0
1	0	X	Q
1	1	↑	D

Inputs
CLR, D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE3B



Function
D-Type Flip-Flop, with Enable and active low Clear and Clock

Truth Table

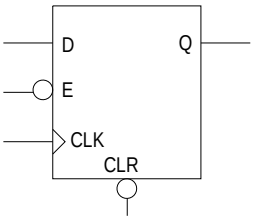
CLR	E	CLK	Q_{n+1}
0	X	X	0
1	0	X	Q
1	1	↓	D

Inputs
CLR, D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE3C



Function
D-Type Flip-Flop, with active low Enable, and Clear

Truth Table

CLR	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

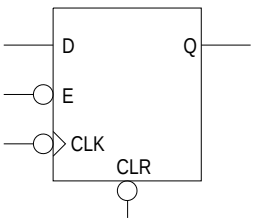
Inputs
CLR, D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DFE3D



Function
D-Type Flip-Flop, with active low Enable, Clear and Clock

Truth Table

CLR	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↓	D

Inputs
CLR, D, E, CLK

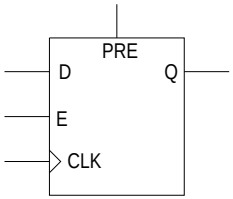
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFE4

ACT 1

40MX



Function
D-Type Flip-Flop, with active high Enable and Preset

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	↑	D

Inputs
D, E, PRE, CLK

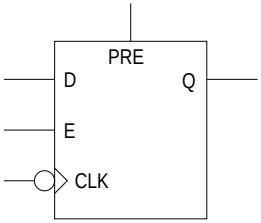
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4A

ACT 1

40MX



Function
D-Type Flip-Flop, with active high Enable and Preset, and active low Clock

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	↓	D

Inputs
D, E, PRE, CLK

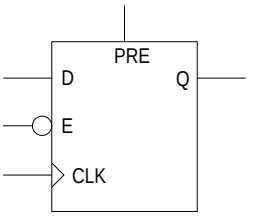
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

DFE4B



Function
D-Type Flip-Flop, with active low Enable, and active high Preset

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	1	X	Q
0	0	↑	D

Inputs
D, E, PRE, CLK

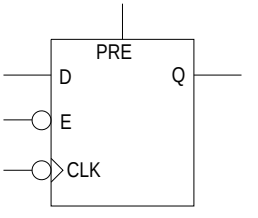
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

DFE4C



Function
D-Type Flip-Flop, with active low Enable and Clock, and active high Preset

Truth Table

PRE	E	CLK	Q_{n+1}
1	X	X	1
0	1	X	Q
0	0	↓	D

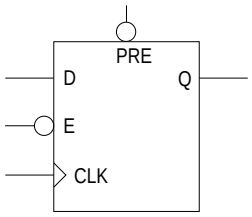
Inputs
D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFE4F

54SX



Function
D-Type Flip-Flop, with active low Enable, and active low Preset

PRE	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

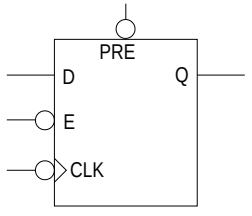
Inputs
D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	

DFE4G

54SX



Function
D-Type Flip-Flop, with active low Enable and Clock, and active low Preset

Truth Table

PRE	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↓	D

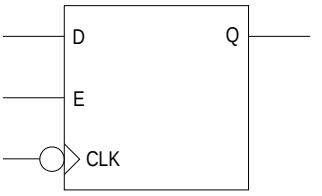
Inputs
D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFEA



Function
D-Type Flip-Flop, with Enable, and active low Clock

Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↓	D

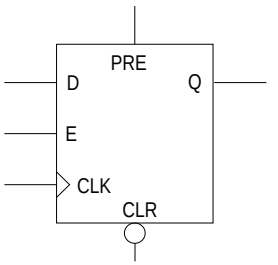
Inputs
D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
40MX

DFEB



Function
D-Type Flip-Flop, with Enable, Preset, and active low Clear

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↑	D
0	1	X	X	*

Inputs
CLR, D, E, PRE, CLK

Outputs
Q

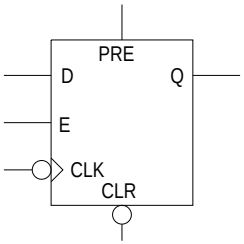
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFEC

ACT 1

40MX



Function
D-Type Flip-Flop, with Enable, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	X	Q
1	0	1	↓	D
0	1	X	X	*

Inputs
CLR, D, E, PRE, CLK

Outputs
Q

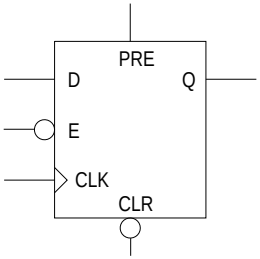
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFED

ACT 1

40MX



Function
D-Type Flip-Flop, with active low Enable and Clear, and active high Preset

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	1	X	Q
1	0	0	↑	D
0	1	X	X	*

Inputs
CLR, D, E, PRE, CLK

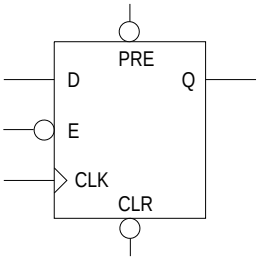
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* You design should not allow both PRE and CLR to be asserted at the same time.

54SX

DFEG



Function
D-Type Flip-Flop with Enable and active low Preset Clear and Clock

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	1	Q
1	1	0	↑	D

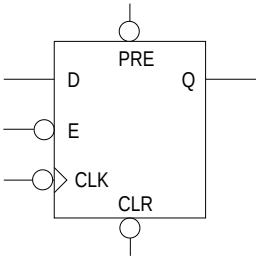
Inputs
CLK, CLR, D, E, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	

54SX

DFEH



Function
D-Type Flip-Flop with active low Enable and Clear and Preset

Truth Table

CLR	PRE	E	CLK	Q_{n+1}
0	X	X	X	0
1	0	X	X	1
1	1	1	X	Q
1	1	0	↓	D

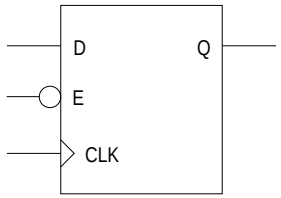
Inputs
CLK, CLR, D, E, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	

IODFE

ACT 3



Function
D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↑	D

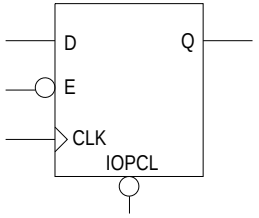
Inputs
D, E, CLK

Outputs
Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
WARNING: Using the IODFE macro will disable the IOPCLBUF clock network.
NOTE 2: Uses an I/O module.

IODFEC

ACT 3



Function
D-Type Flip-Flop, with active low Enable and Clear

Truth Table

IOPCL	E	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	D

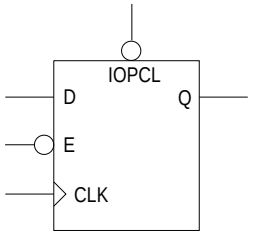
Inputs
IOPCL, D, E, CLK

Outputs
Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.
NOTE 3: Uses an I/O module.

ACT 3

IODFEP



Function
D-Type Flip-Flop, with active low Enable and Preset

Truth Table

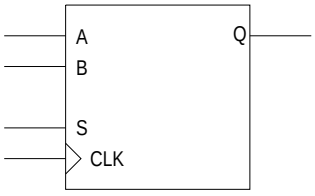
IOPCL	E	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	D

Inputs
CLK, D,E, IOPCL

Outputs
Q

NOTE 1: The CLK pin must be driven by the IOCLKBUF macro.
NOTE 2: The IOPCL pin must be driven by the IOPCLBUF macro.
NOTE 3: Uses an I/O module.

DFM



Function
D-Type Flip-Flop with 2-input Multiplexed Data

Truth Table

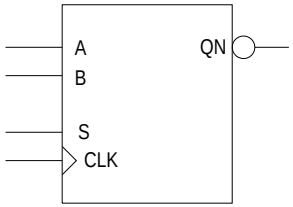
S	CLK	Q_{n+1}
0	↑	A
1	↑	B

Inputs
A, B, S, CLK

Outputs
QQ

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM1B



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

S	CLK	QN_{n+1}
0	↑	!A
1	↑	!B

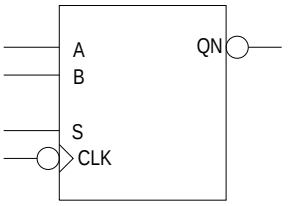
Inputs
A, B, S, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFM1C



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

S	CLK	QN_{n+1}
0	↓	!A
1	↓	!B

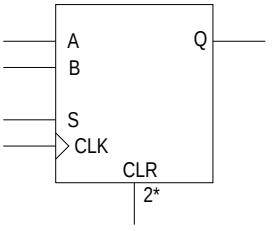
Inputs
A, B, S, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFM3



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active high Clear

Truth Table

CLR	S	CLK	Q_{n+1}
0	0	↑	A
0	1	↑	B

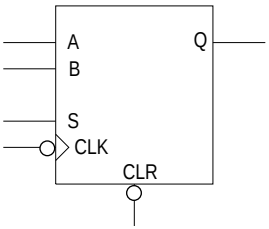
Inputs
A, B, CLR, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX.

DFM3B



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear and Clock

Truth Table

CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↓	A
1	1	↓	B

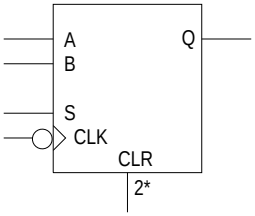
Inputs
A, B, CLR, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFM3E



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock

Truth Table

CLR	S	CLK	Q_{n+1}
1	X	X	0
0	0	↓	A
0	1	↓	B

Inputs
A, B, CLR, S, CLK

Outputs
Q

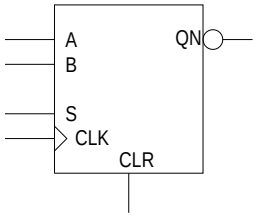
Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays except for ACT 1 and 40MX.

ACT 1

40MX

DFM3F



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Output

Truth Table

CLR	S	CLK	QN_{n+1}
1	X	X	1
0	0	↑	!A
0	1	↑	!B

Inputs
A, B, CLR, S, CLK

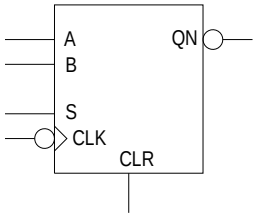
Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

DFM3G



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Clear, and active low Clock and Output

Truth Table

CLR	S	CLK	QN_{n+1}
1	X	X	1
0	0	↓	!A
0	1	↓	!B

Inputs
A, B, CLR, S, CLK

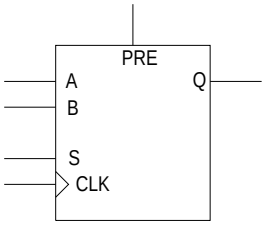
Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM4

ACT 1

40MX



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active high Preset

Truth Table

PRE	S	CLK	Q_{n+1}
1	X	X	1
0	0	↑	A
0	1	↑	B

Inputs
A, B, PRE, S, CLK

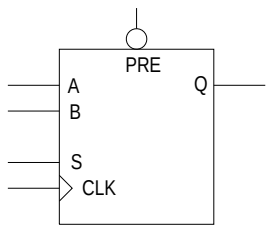
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

DFM4A

ACT 1

40MX



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset

Truth Table

PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	↑	A
1	1	↑	B

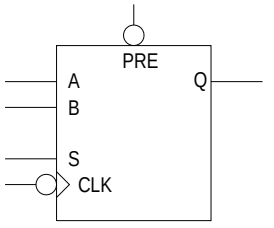
Inputs
A, B, PRE, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1
40MX

DFM4B



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Clock

Truth Table

PRE	S	CLK	Q_{n+1}
0	X	X	1
1	0	↓	A
1	1	↓	B

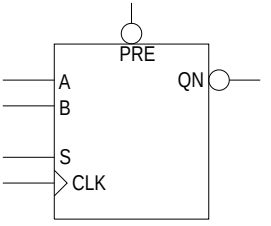
Inputs
A, B, PRE, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFM4C



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset and Output

Truth Table

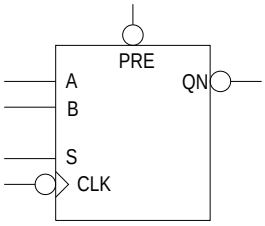
PRE	S	CLK	QN_{n+1}
0	X	X	0
1	0	↑	!A
1	1	↑	!B

Inputs
A, B, PRE, S, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM4D



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Preset, Clock and Output

Truth Table

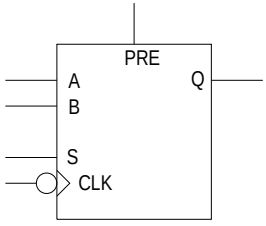
PRE	S	CLK	QN_{n+1}
0	X	X	0
1	0	↓	!A
1	1	↓	!B

Inputs
A, B, PRE, S, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFM4E



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clock

Truth Table

PRE	S	CLK	Q_{n+1}
1	X	X	1
0	0	↓	A
0	1	↓	B

Inputs
A, B, PRE, S, CLK

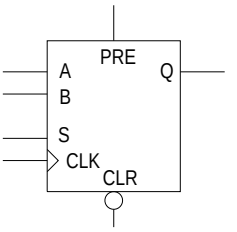
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

DFM5A



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear

Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↑	A
1	0	1	↑	B
0	1	X	X	*

Inputs
A, B, CLR, PRE, S, CLK

Outputs
Q

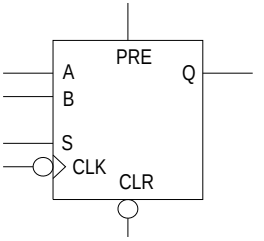
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

ACT 1

40MX

DFM5B



Function
D-Type Flip-Flop with 2-input Multiplexed Data, Preset, and active low Clear and Clock

Truth Table

CLR	PRE	S	CLK	Q_{n+1}
0	0	X	X	0
1	1	X	X	1
1	0	0	↓	A
1	0	1	↓	B
0	1	X	X	*

Inputs
A, B, CLR, PRE, S, CLK

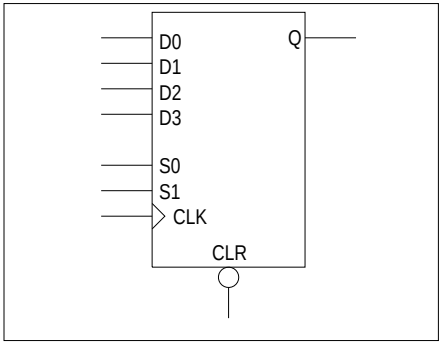
Outputs
Q

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

DFM6A

ACT 2/1200XL
ACT 3
3200DX
42MX



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

CLR	S1	S0	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↑	D0
1	0	1	↑	D1
1	1	0	↑	D2
1	1	1	↑	D3

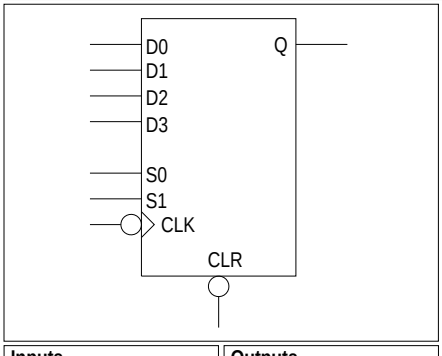
Inputs
D0, D1, D2, D3, S0, S1, CLK, CLR

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

DFM6B

ACT 2/1200XL
ACT 3
3200DX
42MX



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and Clock

Truth Table

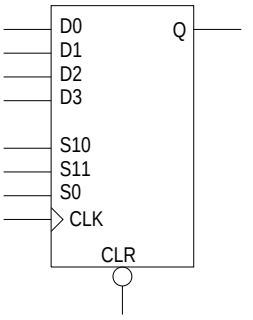
CLR	S1	S0	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↓	D0
1	0	1	↓	D1
1	1	0	↓	D2
1	1	1	↓	D3

Inputs
D0, D,1 D2, D,3 S0, S1, CLK, CLR

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

DFM7A



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

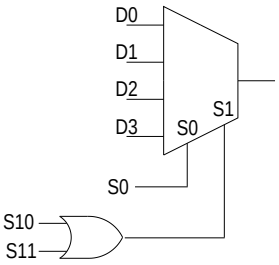
CLR	S11	S10	S0	CLK	Q_{n+1}
0	X	X	X	X	0
1	0	0	0	↑	D0
1	0	0	1	↑	D1
1	1	X	0	↑	D2
1	X	1	0	↑	D2
1	1	X	1	↑	D3
1	X	1	1	↑	D3

Inputs
D0, D1, D2, D3, S0, S10, S11, CLK, CLR

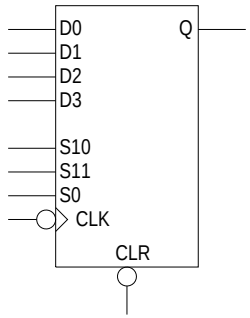
Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

NOTE 1: The DFM7A macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.



DFM7B



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

Truth Table

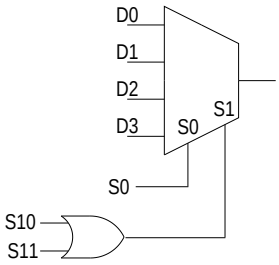
CLR	S11	S10	S0	CLK	Q_{n+1}
0	X	X	X	X	0
1	0	0	0	↓	D0
1	0	0	1	↓	D1
1	1	X	0	↓	D2
1	X	1	0	↓	D2
1	1	X	1	↓	D3
1	X	1	1	↓	D3

Inputs
D0, D1, D2, D3, S0, S10, S11, CLK, CLR

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

NOTE 1: The DFM7B macro represents the full ACT 2/1200XL, 3200DX and 42MX S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.



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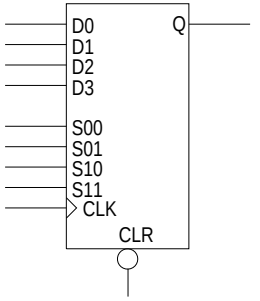
ACT 3

DFM8A



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear, and active high Clock

Truth Table

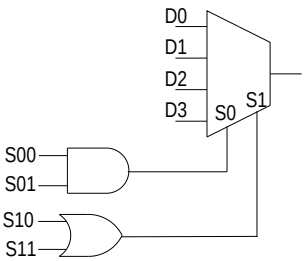
CLR	S11	S10	S01	S00	CLK	Q_{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↑	D0
1	0	0	X	0	↑	D0
1	0	0	1	1	↑	D1
1	1	X	0	X	↑	D2
1	X	1	0	X	↑	D2
1	1	X	X	0	↑	D2
1	X	1	X	0	↑	D2
1	1	X	1	1	↑	D3
1	X	1	1	1	↑	D3

Inputs
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

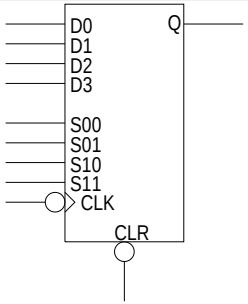
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 3	1	

NOTE 1: The DFM8A macro represents the full ACT 3 S-Module.
NOTE 2: The following schematic describes the interconnections of the select lines.



DFM8B



Function
D-Type Flip-Flop with 4-input Multiplexed Data, active low Clear and Clock

Truth Table

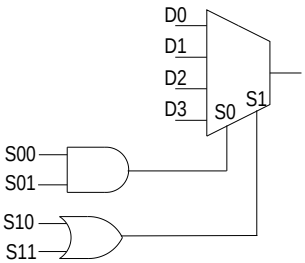
CLR	S11	S10	S01	S00	CLK	Q_{n+1}
0	X	X	X	X	X	0
1	0	0	0	X	↓	D0
1	0	0	X	0	↓	D0
1	0	0	1	1	↓	D1
1	1	X	0	X	↓	D2
1	X	1	0	X	↓	D2
1	1	X	X	0	↓	D2
1	X	1	X	0	↓	D2
1	1	X	1	1	↓	D3
1	X	1	1	1	↓	D3

Inputs
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

Outputs
Q

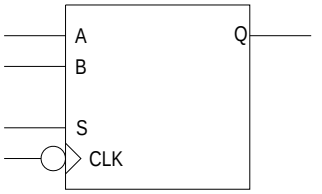
Family	Modules	
	Seq	Comb
ACT 3	1	

NOTE 1:DFM8B macro represents the full ACT 3 S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.



ACT 3
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFMA



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

S	CLK	Q_{n+1}
0	↓	A
1	↓	B

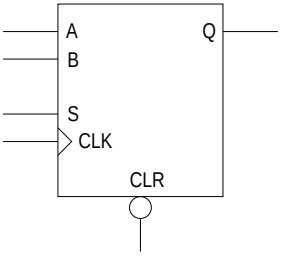
Inputs
A, B, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFMB



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clear

Truth Table

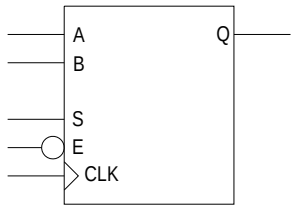
CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↑	A
1	1	↑	B

Inputs
A, B, CLR, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFME1A



Function
2-bit D-Type Flip-Flop with Multiplexed Data, and active low Enable

Truth Table

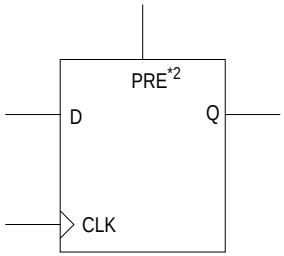
E	S	CLK	Q_{n+1}
1	X	X	Q
0	0	↑	A
0	1	↑	B

Inputs
A, B, E, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFP1



Function
D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↑	D

Inputs
D, PRE, CLK

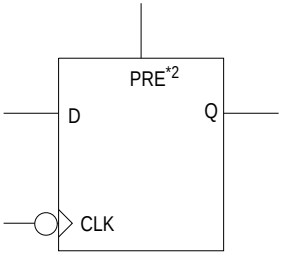
Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DFP1A



Function
D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↓	D

Inputs
D, PRE, CLK

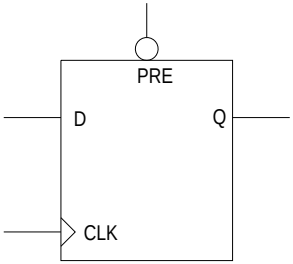
Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DFP1B



Function
D-Type Flip-Flop with active low Preset

Truth Table

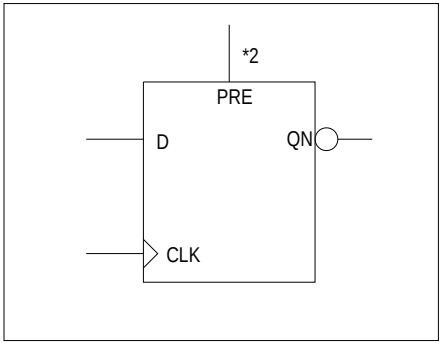
PRE	CLK	Q_{n+1}
0	X	1
1	↑	D

Inputs
D, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	
Others		2

DFP1C



Function
D-Type Flip-Flop with active high Preset, and active low Output

Truth Table

PRE	CLK	QN_{n+1}
1	X	0
0	↑	!D

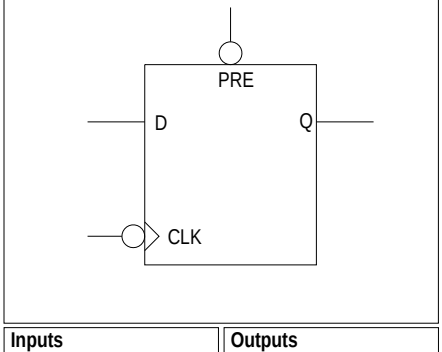
Inputs
D, PRE, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

* A 2 on the symbol implies 2 logic module delays on all families except ACT 1 and 40MX.

DFP1D



Function
D-Type Flip-Flop with active low Preset and Clock

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↓	D

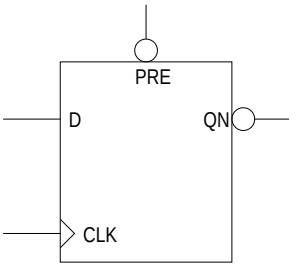
Inputs
D, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	
Others		2

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFP1E



Function
D-Type Flip-Flop with active low Preset and Output

Truth Table

PRE	CLK	QN_{n+1}
0	X	0
1	↑	!D

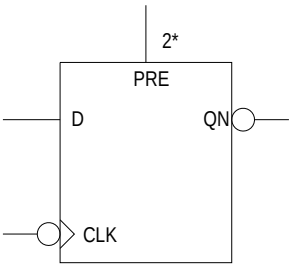
Inputs
D, PRE, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFP1F



Function
D-Type Flip-Flop with active high Preset, and active low Clock and Output

Truth Table

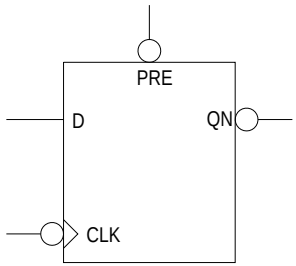
PRE	CLK	QN_{n+1}
1	X	0
0	↓	!D

Inputs
D, PRE, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	1

DFP1G



Function
D-Type Flip-Flop with active low Preset, Clock and Output

Truth Table

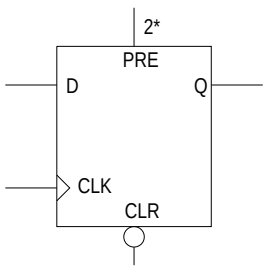
PRE	CLK	QN_{n+1}
0	X	0
1	↓	!D

Inputs
D, PRE, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others	1	

DFPC



Function
D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↑	D
0	1	X	**

Inputs
CLR, D, PRE, CLK

Outputs
Q

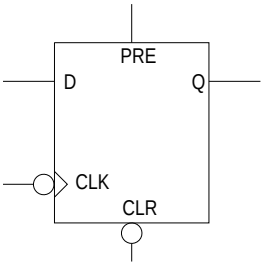
Family	Modules	
	Seq	Comb
54SX	1	1
Others		2

* A 2 on the symbol implies 2 logic module delays only for 54SX.

** In ACT 1/40MX, your design should not allow both PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DFPCA



Function
D-Type Flip-Flop with active high Preset, active low Clear, and Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	*

Inputs
CLR, D, PRE, CLK

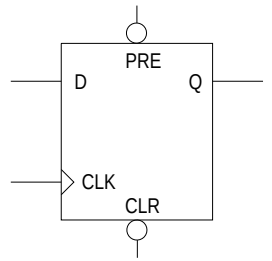
Outputs
Q

Family	Modules	
	Seq	Comb
All		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

54SX

DFPCB



Function
D-Type Flip-Flop, with active low Clear, and Preset

Truth Table

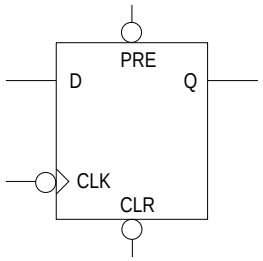
CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	0	X	1
1	1	↑	D

Inputs
CLR, D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	

DFPCC



Function
D-Type Flip-Flop, with active low Preset, Clear and Clock

Truth Table

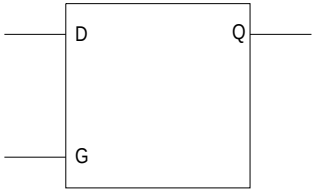
CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	0	X	1
1	1	↓	D

Inputs
CLR, D, E, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
54SX	1	

DL1



Function
Data Latch

Truth Table

G	Q_{n+1}
0	Q
1	D

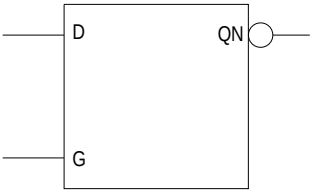
Inputs
D, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DL1A



Function
Data Latch, with active low Output

Truth Table

G	QN_{n+1}
0	QN
1	!D

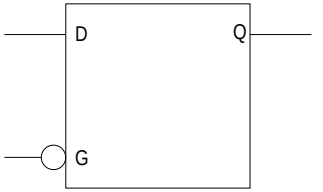
Inputs
D, G

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DL1B



Function
Data Latch, with active low Clock

Truth Table

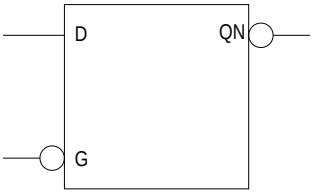
G	Q_{n+1}
1	Q
0	D

Inputs
D, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

DL1C



Function
Data Latch, with active low Clock, and Output

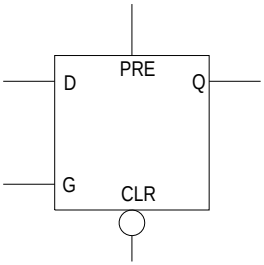
G	QN_{n+1}
1	QN
0	!D

Inputs
D, G

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DL2A



Function
Data Latch with active low Clear, and active high Preset

Truth Table

CLR	PRE	G	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	0	Q
1	0	1	D
0	1	X	*

Inputs
CLR, D, G, PRE

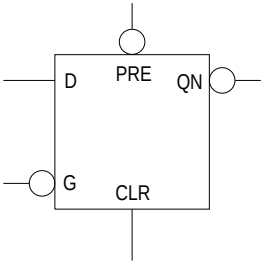
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DL2B



Function
Data Latch with active high Clear, and active low Preset, Clock and Output

CLR	PRE	G	QN_{n+1}
1	1	X	1
0	0	X	0
0	1	1	QN
0	1	0	!D
1	0	X	*

Inputs
CLR, D, G, PRE

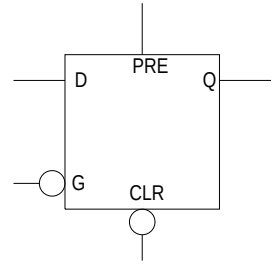
Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DL2C



Function
Data Latch with active low Clear, active high Preset, and active low Clock

Truth Table

CLR	PRE	G	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	1	Q
1	0	0	D
0	1	X	*

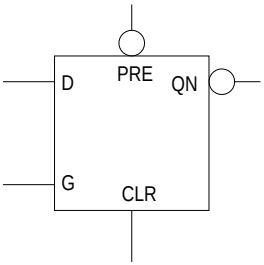
Inputs
CLR, D, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

DL2D



Function
Data Latch with active high Clear, and active low Preset, and Output

Truth Table

CLR	PRE	G	QN_{n+1}
1	1	X	1
0	0	X	0
0	1	0	QN
0	1	1	!D
1	0	X	*

Inputs
CLR, D, G, PRE

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* In ACT 1 and 40MX, your design should not allow PRE and CLR to be asserted at the same time. In other families, CLR has priority over PRE.

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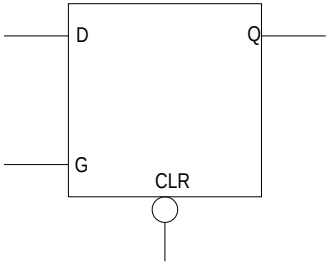
DLC



Function
Data Latch with active low Clear

Truth Table

CLR	G	Q_{n+1}
0	X	0
1	0	Q
1	1	D

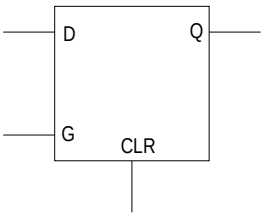
Inputs
CLR, D, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DLC1



Function
Data Latch with active high Clear

Truth Table

CLR	G	Q_{n+1}
1	X	0
0	0	Q
0	1	D

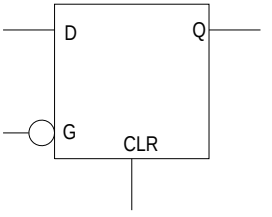
Inputs
CLR, D, G

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DLC1A



Function
Data Latch with active high Clear, and active low Clock

Truth Table

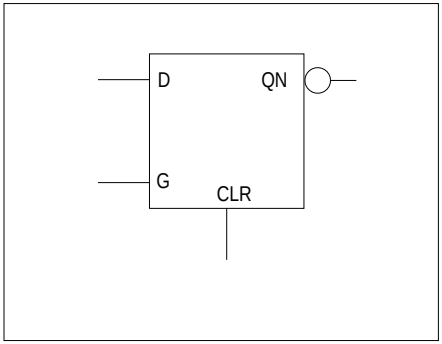
CLR	G	Q_{n+1}
1	X	0
0	1	Q
0	0	D

Inputs
CLR, D, G

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

DLC1F



Function
Data Latch with active high Clear, and active low Output

Truth Table

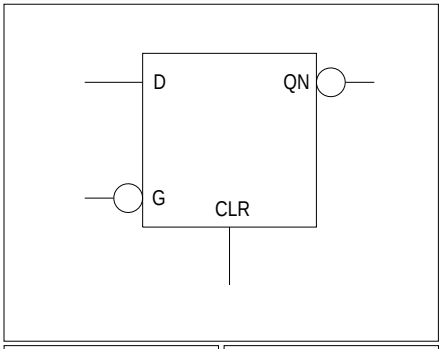
CLR	G	QN_{n+1}
1	X	1
0	0	QN
0	1	!D

Inputs
CLR, D, G

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

DLC1G



Function
Data Latch with active high Clear, and active low Clock and Output

Truth Table

CLR	G	QN_{n+1}
1	X	1
0	1	QN
0	0	!D

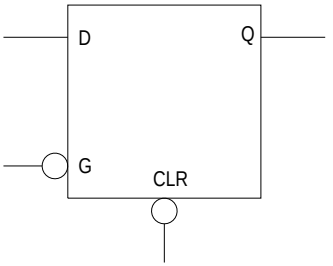
Inputs
CLR, D, G

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DLCA



Function
Data Latch with active low Clear and Clock

Truth Table

CLR	G	Q_{n+1}
0	X	0
1	1	Q
1	0	D

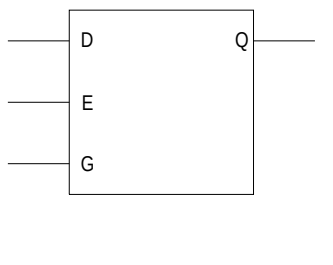
Inputs
CLR, D, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
54SX		1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DLE



Function
Data Latch with active high Enable

Truth Table

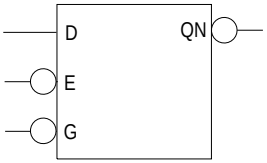
E	G	Q_{n+1}
0	X	Q
X	0	Q
1	1	D

Inputs
D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLE1D



Function
Data Latch with active low Enable and Clock, and active low Output

Truth Table

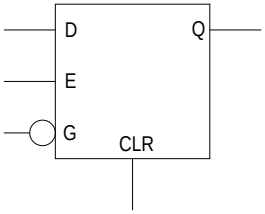
E	G	QN_{n+1}
1	X	QN
X	1	QN
0	0	!D

Inputs
D, E, G

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40fMX		1
Others	1	

DLE2A



Function
Data Latch with active high Enable and Clear, and active low Clock

Truth Table

CLR	E	G	Q_{n+1}
1	X	X	0
0	0	X	Q
0	X	1	Q
0	1	0	D

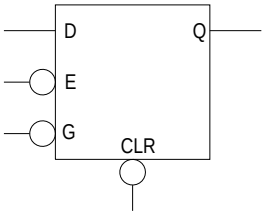
Inputs
CLR, D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DLE2B



Function
Data Latch with active low Enable, Clear and Clock

Truth Table

CLR	E	G	Q_{n+1}
0	X	X	0
1	1	X	Q
1	X	1	Q
1	0	0	D

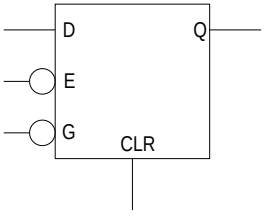
Inputs
CLR, D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DLE2C



Function
Data Latch with active low Enable and Clock, and active high Clear

Truth Table

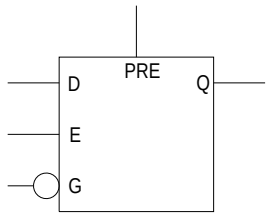
CLR	E	G	Q_{n+1}
1	X	X	0
0	1	X	Q
0	X	1	Q
0	0	0	D

Inputs
CLR, D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

DLE3A



Function
Data Latch with active high Enable and Preset, and active low Clock

Truth Table

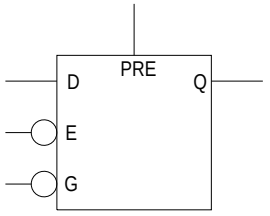
PRE	E	G	Q_{n+1}
1	X	X	1
0	0	X	Q
0	1	0	D
0	X	1	Q

Inputs
D, E, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

DLE3B



Function
Data Latch with active low Enable and Clock, and active low Preset

Truth Table

PRE	E	G	Q_{n+1}
1	X	X	1
0	1	X	Q
0	X	1	Q
0	0	0	D

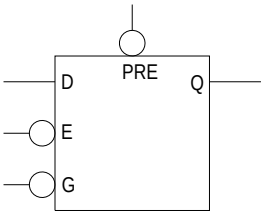
Inputs
D, E, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DLE3C



Function
Data Latch with active low Enable, Preset and Clock

Truth Table

PRE	E	G	Q_{n+1}
0	X	X	1
1	1	X	Q
1	X	1	Q
1	0	0	D

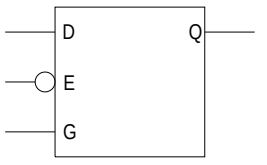
Inputs
D, E, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DLEA



Function
Data Latch with active low Enable, and active high Clock

Truth Table

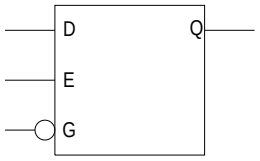
E	G	Q_{n+1}
1	X	Q
X	0	Q
0	1	D

Inputs
D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLEB



Function
Data Latch with active high Enable, and active high Clock

Truth Table

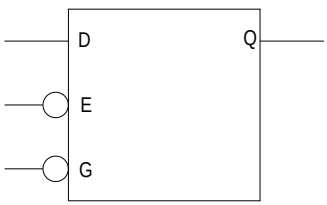
E	G	Q_{n+1}
0	X	Q
X	1	Q
1	0	D

Inputs
D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLEC



Function
Data Latch with active low Enable, and Clock

Truth Table

E	G	Q_{n+1}
1	X	Q
X	1	Q
0	0	D

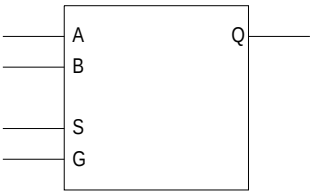
Inputs
D, E, G

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DLM



Function
Data Latch with 2-input Multiplexed Data

Truth Table

S	G	Q_{n+1}
X	0	Q
0	1	A
1	1	B

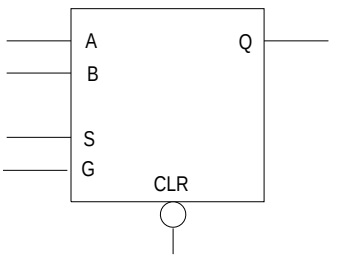
Inputs
A, B, G, S

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 2/1200XL
ACT 3
3200DX
42MX

DLM2



Function
Data Latch with 2-input Multiplexed Data and Active-Low Clear

Truth Table

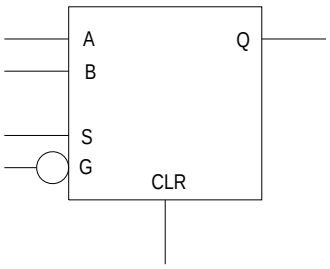
CLR	S	G	Q_{n+1}
0	X	X	0
1	X	0	Q
1	0	1	A
1	1	1	B

Inputs
A, B, CLR, G, S

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

DLM2A



Function
Data Latch with 2-input Multiplexed Data and Clear, and Active-Low Clock

Truth Table

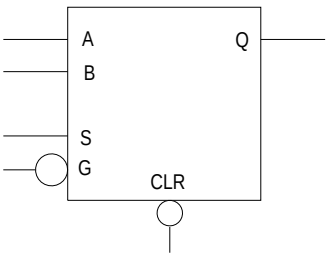
CLR	S	G	Q_{n+1}
1	X	X	0
0	X	1	Q
0	0	0	A
0	1	0	B

Inputs
A, B, CLR, G, S

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1

DLM2B



Function
Data Latch with 2-input Multiplexed Data and Active-Low Clock and Clear

Truth Table

CLR	S	G	Q_{n+1}
0	X	X	0
1	X	1	Q
1	0	0	A
1	1	0	B

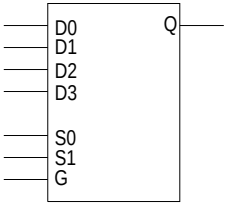
Inputs
A, B, CLR, G, S

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

ACT 2/1200XL
ACT 3
3200DX
42MX

DLM3



Function
Data Latch with 4-input Multiplexed Data

Truth Table

S1	S0	G	Q_{n+1}
X	X	0	Q
0	0	1	D0
0	1	1	D1
1	0	1	D2
1	1	1	D3

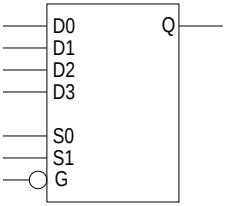
Inputs
D0, D1, D2, D3, S0, S1, G

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

ACT 2/1200XL
ACT 3
3200DX
42MX

DLM3A



Function
Data Latch with 4-input Multiplexed Data, and active low Clock

Truth Table

S1	S0	G	Q_{n+1}
X	X	1	Q
0	0	0	D0
0	1	0	D1
1	0	0	D2
1	1	0	D3

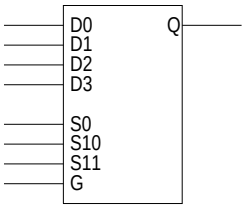
Inputs
D0, D1, D2, D3, S0, S1, G

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

DLM4

ACT 2/1200XL
ACT 3
3200DX
42MX



Function
Data Latch with 4-input Multiplexed Data

Truth Table

S10	S11	S0	G	Q_{n+1}
X	X	X	0	Q
0	0	0	1	D0
0	0	1	1	D1
X	1	0	1	D2
1	X	0	1	D2
X	1	1	1	D3
1	X	1	1	D3

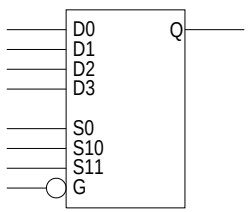
Inputs
D0, D1, D2, D3, D0, S0, S10, S11, G

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

DLM4A

ACT 2/1200XL
ACT 3
3200DX
42MX



Function
Data Latch with 4-input Multiplexed Data

Truth Table

S10	S11	S0	G	Q_{n+1}
X	X	X	1	Q
0	0	0	0	D0
0	0	1	0	D1
X	1	0	0	D2
1	X	0	0	D2
X	1	1	0	D3
1	X	1	0	D3

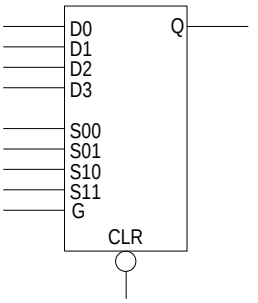
Inputs
D0, D1, D2, D3, D0, S0, S10, S11, G

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

ACT 3

DLM8A



Function
D-Type Latch with 4-input Multiplexed Data and active low Clear

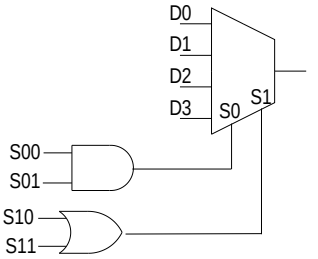
Truth Table

CLR	S11	S10	S01	S00	G	Q_{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	0	Q
1	0	0	0	X	1	D0
1	0	0	X	0	1	D0
1	0	0	1	1	1	D1
1	1	X	0	X	1	D2
1	X	1	0	X	1	D2
1	1	X	X	0	1	D2
1	X	1	X	0	1	D2
1	1	X	1	1	1	D3
1	X	1	1	1	1	D3

Inputs
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

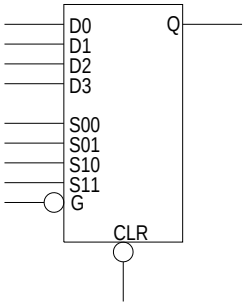
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 3	1	



NOTE 1: The DLM8A macro represents the full ACT 3 S-Module.
NOTE 2: The following schematic describes the interconnections of the select lines.

DLM8B



Function
D-Type Latch with 4-input Multiplexed Data and active low Clear

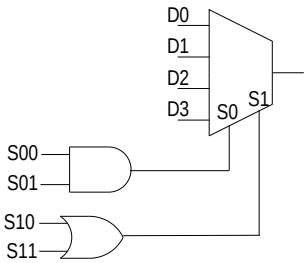
Inputs
D0, D1, D2, D3, S00, S01, S10, S11, CLK, CLR

Outputs
Q

Truth Table

CLR	S11	S10	S01	S00	G	Q_{n+1}
0	X	X	X	X	X	0
1	X	X	X	X	1	Q
1	0	0	0	X	0	D0
1	0	0	X	0	0	D0
1	0	0	1	1	0	D1
1	1	X	0	X	0	D2
1	X	1	0	X	0	D2
1	1	X	X	0	0	D2
1	X	1	X	0	0	D2
1	1	X	1	1	0	D3
1	X	1	1	1	0	D3

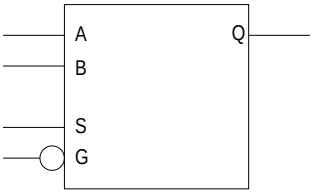
Family	Modules	
	Seq	Comb
ACT 3	1	



NOTE 1: The DLM8B macro represents the full ACT 3 S-module.
NOTE 2: The following schematic describes the interconnections of the select lines.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DLMA



Function
Data Latch with 2-input Multiplexed Data, and active low Clock

Truth Table

S	G	Q_{n+1}
X	1	Q
0	0	A
1	0	B

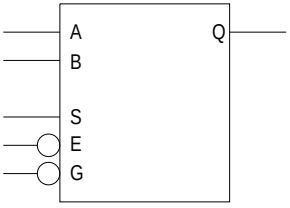
Inputs
A, B, G, S

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

DLME1A



Function
2-bit Data Latch with Multiplexed Data and Enable, and active low Clock

Truth Table

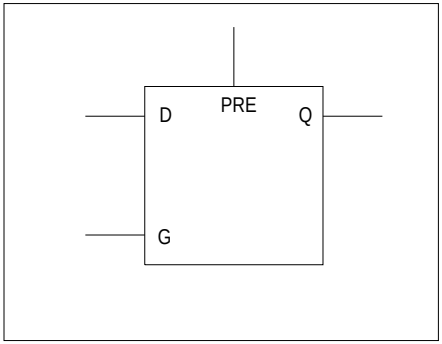
E	S	G	Q_{n+1}
1	X	X	Q
X	X	1	Q
0	0	0	A
0	1	0	B

Inputs
A, B, E, G, S

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLP1



Function
Data Latch with active high Preset, and Clock

Truth Table

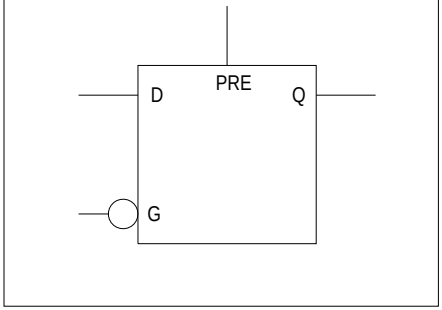
PRE	G	Q_{n+1}
1	X	1
0	0	Q
0	1	D

Inputs
D, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

DLP1A



Function
Data Latch with active high Preset, and active low Clock

Truth Table

PRE	G	Q_{n+1}
1	X	1
0	1	Q
0	0	D

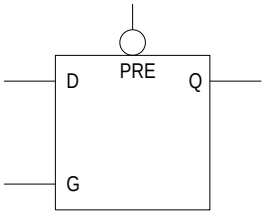
Inputs
D, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DLP1B



Function
Data Latch with active low Preset, and active high Clock

Truth Table

PRE	G	Q_{n+1}
0	X	1
1	0	Q
1	1	D

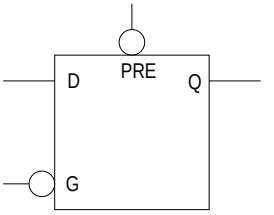
Inputs
D, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

DLP1C



Function
Data Latch with active low Preset and Clock

Truth Table

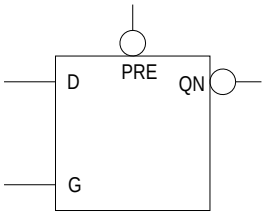
PRE	G	Q_{n+1}
0	X	1
1	1	Q
1	0	D

Inputs
D, G, PRE

Outputs
Q

Family	Modules	
	Seq	Comb
All		1

DLP1D



Function
Data Latch with active low Preset and Output, and active high Clock

Truth Table

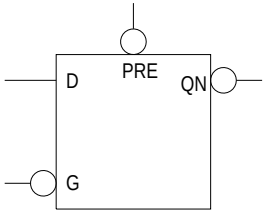
PRE	G	QN_{n+1}
0	X	0
1	0	QN
1	1	!D

Inputs
D, G, PRE

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

DLP1E



Function
Data Latch with active low Preset, Clock and Output

Truth Table

PRE	G	Q_{n+1}
0	X	0
1	0	!D
1	1	QN

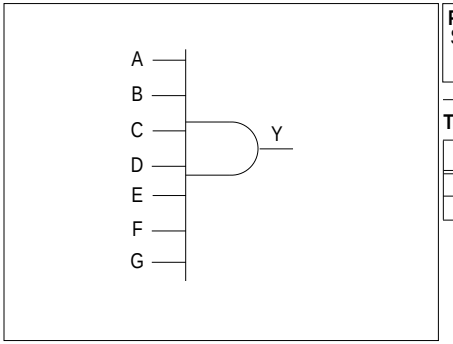
Inputs
D, G, PRE

Outputs
QN

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others	1	

3200DX
42MX

DXAND7



Function
Seven-input AND Gate

Truth Table

A through G	Y
All inputs = 1	1
Any input = 0	0

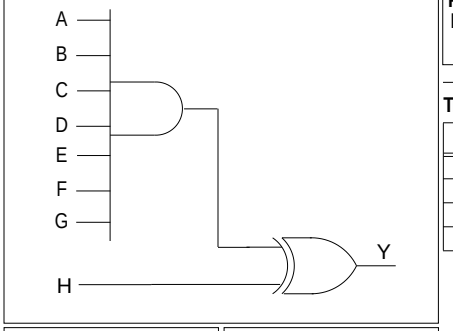
Inputs
A, B, C, D, E, F, G

Outputs
Y

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

3200DX
42MX

DXAX7



Function
Eight-input AND/Exclusive-OR Gate

Truth Table

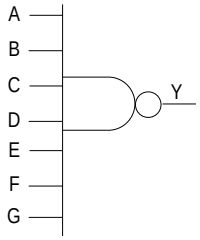
A through G	H	Y
Any input = 0	0	0
Any input = 0	1	1
All inputs = 1	0	1
All inputs = 1	1	0

Inputs
A, B, C, D, E, F, G, H

Outputs
Y

Family	Modules	
	Seq	DX
3200DX/ 42MX		1

DXNAND7



Function
Seven-input NAND Gate

Truth Table

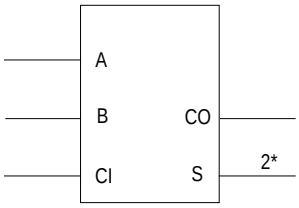
A through G	Y
All inputs = 1	0
Any input = 0	1

Inputs
A, B, C, D, E, F, G

Outputs
Y

Family	Modules	
	Seq	DX
3200DX/42MX		1

FA1



Function
1 bit adder with active high I/Os

Truth Table

A	B	CI	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Inputs
A, B, CI

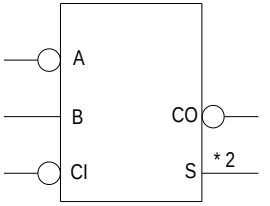
Outputs
CO, S

Family	Modules	
	Seq	Comb
ACT 1/ 40MX		3
54SX		2

* A 2 on the symbol implies 2 logic module delays only in ACT 1 and 40MX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

FA1A



Function
1-bit Adder, with active low Carry In and Carry Out, and active low A-Input

Truth Table

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Inputs
A, B, CI

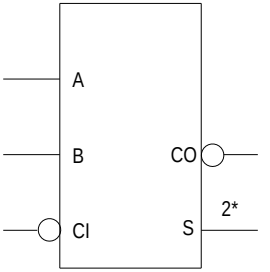
Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

FA1B



Function
1-bit Adder, with active low Carry In and Carry Out

Truth Table

A	B	CI	CO	S
0	0	0	1	1
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0

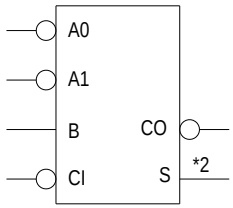
Inputs
A, B, CI

Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families except 54SX.

FA2A



Function
1-bit Adder, with active low Carry In and Carry Out, and active low A0 and A1 Inputs, used in multipliers

Inputs
A0, A1, B, CI

Outputs
CO, S

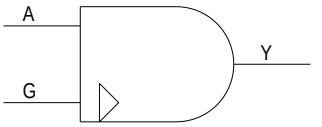
A0	A1	B	CI	CO	S
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	1	1

Family	Modules	
	Seq	Comb
All		2

* A 2 on the symbol implies 2 logic module delays in all families.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

GAND2



Function
2-Input AND Clock Net

Truth Table

A	G	Y
X	0	0
0	X	0
1	1	1

Inputs
A, G

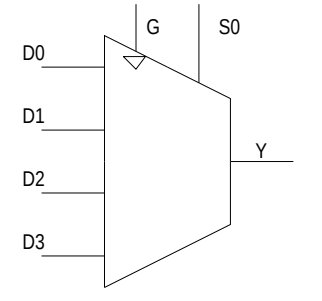
Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

GMX4



Function
4-to-1 Mux Clock Net

Truth Table

G	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

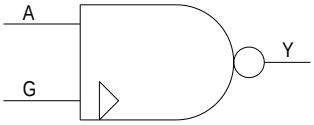
Inputs
D0, D1, D2, D3, S0, G

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GNAND2



Function
2-Input NAND Clock Net

Truth Table

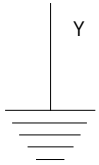
A	G	Y
X	0	1
0	X	1
1	1	0

Inputs	Outputs
A, G	Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GND



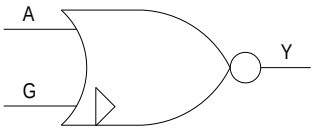
Function
Ground

Inputs	Outputs
	Y

NOTE: GND does not use any modules.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

GNOR2



Function
2-Input NOR Clock Net

Truth Table

A	G	Y
0	0	1
X	1	0
1	X	0

Inputs
A, G

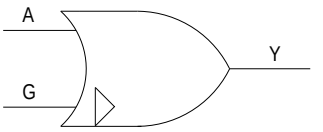
Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

GOR2



Function
2-Input OR Clock Net

Truth Table

A	G	Y
0	0	0
X	1	1
1	X	1

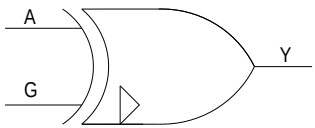
Inputs
A, G

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

GXOR2



Function

2-Input XOR Clock Net

Truth Table

A	G	Y
0	0	0
0	1	1
1	0	1
1	1	0

Inputs

A, G

Outputs

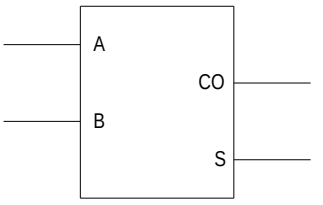
Y

Family	Modules	
	Seq	Comb
All		1

NOTE: G pin can be connected directly to a Global Clock Network.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

HA1



Function
Half-Adder

Truth Table

A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

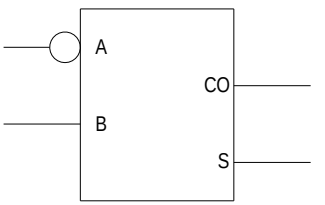
Inputs
A, B

Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

HA1A



Function
Half-Adder with active low A-Input

Truth Table

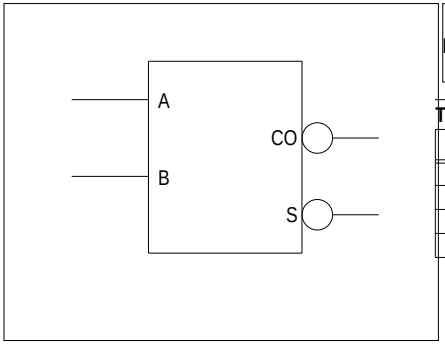
A	B	CO	S
0	0	0	1
0	1	1	0
1	0	0	0
1	1	0	1

Inputs
A, B

Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

HA1B



Function
Half-Adder with active low Carry Out and Sum

Truth Table

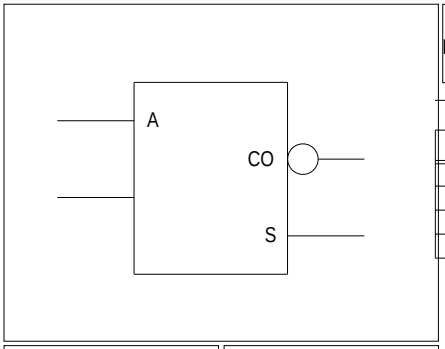
A	B	CO	S
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	1

Inputs
A, B

Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

HA1C



Function
Half-Adder with active low Carry Out

A	B	CO	S
0	0	1	0
0	1	1	1
1	0	1	1
1	1	0	0

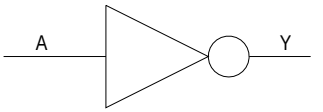
Inputs
A, B

Outputs
CO, S

Family	Modules	
	Seq	Comb
All		2

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

INV



Function
Inverter with active low Output

Truth Table

A	Y
0	1
1	0

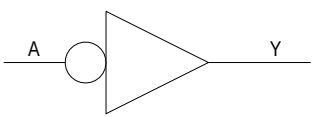
Inputs
A

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

INVA



Function
Inverter with active low Input

Truth Table

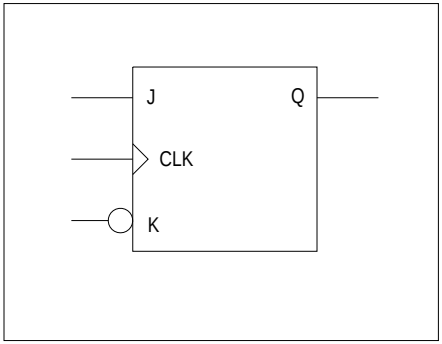
A	Y
0	1
1	0

Inputs
A

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

JKF



Function

JK Flip-Flop with active low K-Input

Truth Table

J	K	CLK	Q_{n+1}
0	0	↑	0
0	1	↑	Q
1	0	↑	!Q
1	1	↑	1

Inputs

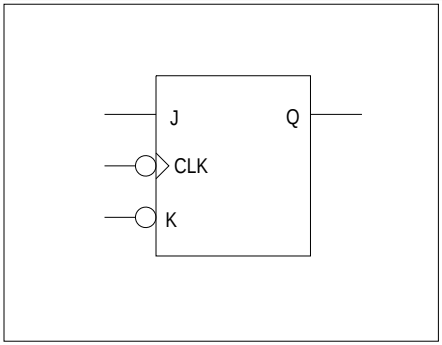
J, K, CLK

Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

JKF1B



Function

JK Flip-Flop with active low Clock and K-Input

Truth Table

J	K	CLK	Q_{n+1}
0	0	↓	0
0	1	↓	Q
1	0	↓	!Q
1	1	↓	1

Inputs

J, K, CLK

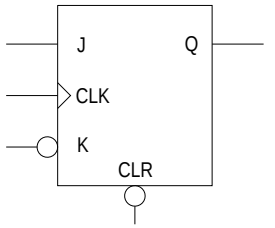
Outputs

Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

JKF2A



Function
JK Flip-Flop with active low Clear and K-Input

Truth Table

CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

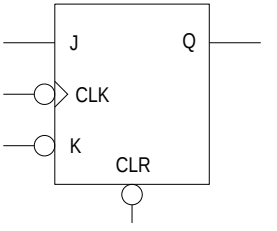
Inputs
CLR, J, K, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

JKF2B



Function
JK Flip-Flop with active low Clear, Clock and K-Input

Truth Table

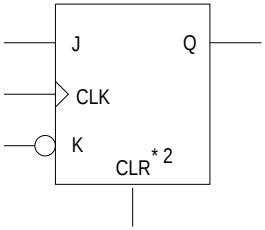
CLR	J	K	CLK	Q_{n+1}
0	X	X	X	0
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	!Q
1	1	1	↓	1

Inputs
CLR, J, K, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1
Others	1	

JKF2C



Function

JK Flip-Flop with active high Clear, and active low K-Input

Truth Table

CLR	J	K	CLK	Q_{n+1}
1	X	X	X	0
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Inputs

CLR, J, K, CLK

Outputs

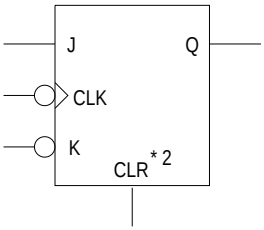
Q

Family	Modules	
	Seq	Comb
ACT 1		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

JKF2D



Function

JK Flip-Flop with active high Clear, and active low Clock and K-Input

Truth Table

CLR	J	K	CLK	Q_{n+1}
1	X	X	X	0
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Inputs

CLR, J, K, CLK

Outputs

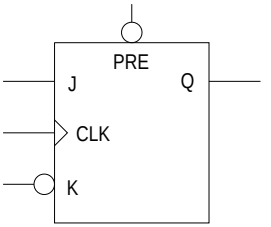
Q

Family	Modules	
	Seq	Comb
ACT 1		2
Others	1	1

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

ACT 1
40MX
54SX

JKF3A



Function
JK Flip-Flop with active low Preset and K-Input

Truth Table

PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	↑	0
1	0	1	↑	Q
1	1	0	↑	!Q
1	1	1	↑	1

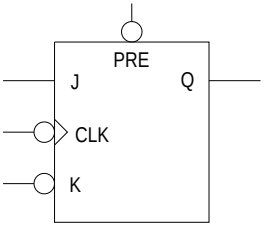
Inputs
J, K, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1

ACT 1
40MX
54SX

JKF3B



Function
JK Flip-Flop with active low Preset, Clock and K-Input

Truth Table

PRE	J	K	CLK	Q_{n+1}
0	X	X	X	1
1	0	0	↓	0
1	0	1	↓	Q
1	1	0	↓	!Q
1	1	1	↓	1

Inputs
J, K, PRE, CLK

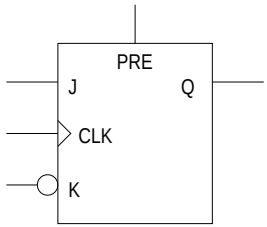
Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
54SX	1	1

JKF3C

ACT 1

40MX



Function

JK Flip-Flop with active high Preset, and active low K-Input

Truth Table

PRE	J	K	CLK	Q_{n+1}
1	X	X	X	1
0	0	0	↑	0
0	0	1	↑	Q
0	1	0	↑	!Q
0	1	1	↑	1

Inputs

J, K, PRE, CLK

Outputs

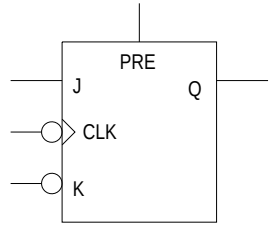
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

JKF3D

ACT 1

40MX



Function

JK Flip-Flop with active high Preset, and active low Clock and K-Inputs

Truth Table

PRE	J	K	CLK	Q_{n+1}
1	X	X	X	1
0	0	0	↓	0
0	0	1	↓	Q
0	1	0	↓	!Q
0	1	1	↓	1

Inputs

J, K, PRE, CLK

Outputs

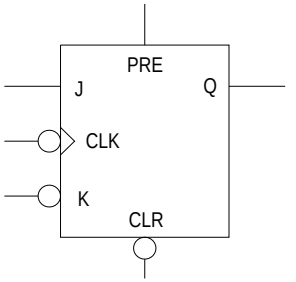
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

ACT 1

40MX

JKF4B



Function
JK Flip-Flop with active high Preset, active low Clear, Clock and K-Input

Truth Table

CLR	PRE	J	K	CLK	Q_{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↓	0
1	0	0	1	↓	Q
1	0	1	0	↓	!Q
1	0	1	1	↓	1
0	1	X	X	X	*

Inputs
CLR, J, K, PRE, CLK

Outputs
Q

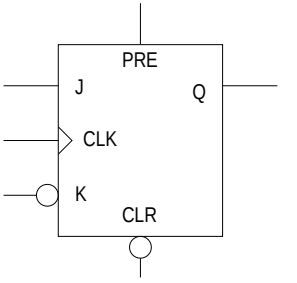
Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

ACT 1

40MX

JKFPC



Function
JK Flip-Flop with active high Preset, and active low Clear and K- Input

Truth Table

CLR	PRE	J	K	CLK	Q_{n+1}
0	0	X	X	X	0
1	1	X	X	X	1
1	0	0	0	↑	0
1	0	0	1	↑	Q
1	0	1	0	↑	!Q
1	0	1	1	↑	1
0	1	X	X	X	*

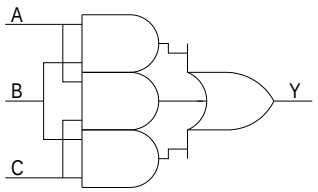
Inputs
CLR, J, K, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
ACT 1/40MX		2

* Your design should not allow both PRE and CLR to be asserted at the same time.

MAJ3



Function
3 Input majority function

Truth TableY

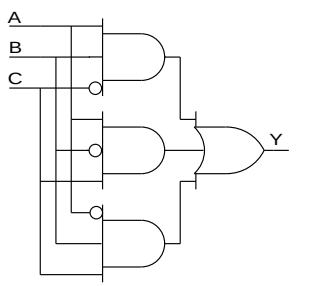
A	B	C	Y
X	0	0	0
0	0	X	0
0	X	0	0
X	1	1	1
1	X	1	1
1	1	X	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

MAJ3X



Function
2 of 3 function

Truth TableY

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

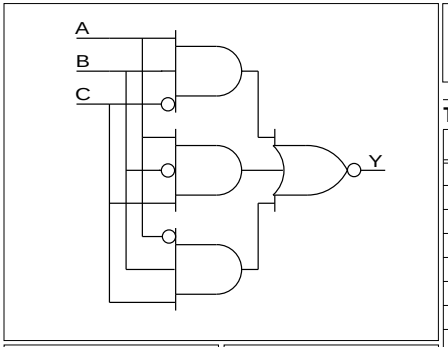
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

MAJ3XI



Function
2 of 3 function with active low output

Truth TableY

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

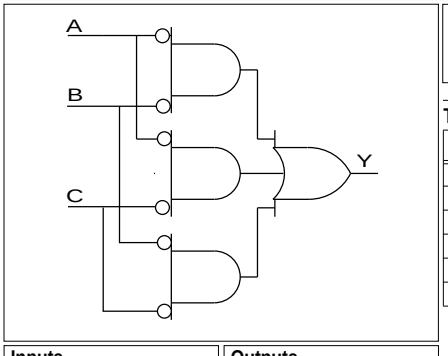
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

MIN3



Function
3 input minority function

Truth TableY

A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

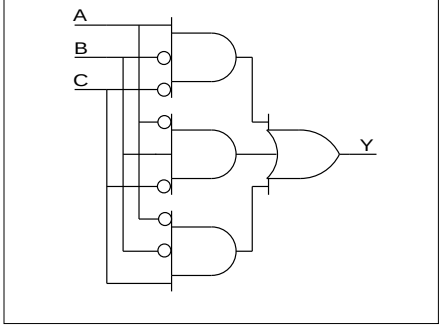
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

MIN3X

54SX



Function
1 of 3 function

Truth TableY

A	B	C	Y
X	0	0	1
0	0	X	1
0	X	0	1
X	1	1	0
1	X	1	0
1	1	X	0

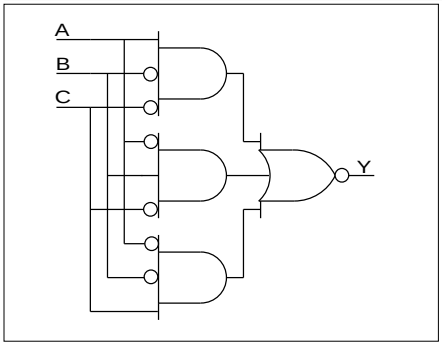
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

MIN3XI

54SX



Function
1 of 3 function with active low output

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

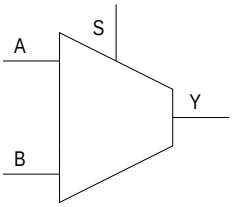
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

MX2



Function
2 to 1 Multiplexer

Truth Table

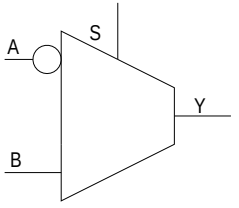
S	Y
0	A
1	B

Inputs	Outputs
A, S, B	Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

MX2A



Function
2 to 1 Multiplexer with active low A-Input

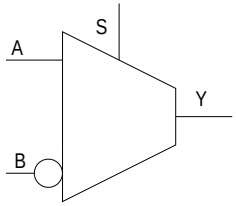
Truth Table

S	Y
0	!A
1	B

Inputs	Outputs
A, S, B	Y

Family	Modules	
	Seq	Comb
All		1

MX2B



Function
2 to 1 Multiplexer with active low B-Input

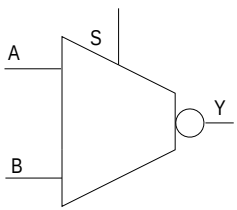
Truth Table

S	Y
0	A
1	!B

Inputs	Outputs
A, S, B	Y

Family	Modules	
	Seq	Comb
All		1

MX2C



Function
2 to 1 Multiplexer with active low Output

Truth Table

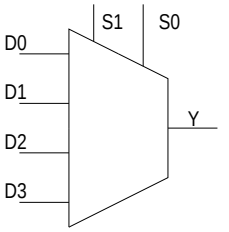
S	Y
0	!A
1	!B

Inputs	Outputs
A, S, B	Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

MX4



Function
4 to 1 Multiplexer

Truth Table

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

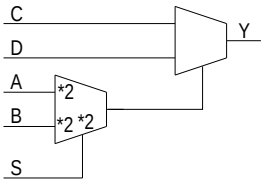
Inputs
D0, S0, S1, D1, D2, D3

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

MXC1



Function
Carry select multiplexer, used in adders

Truth Table

A	B	S	Y
0	X	0	C
1	X	0	D
X	0	1	C
X	1	1	D

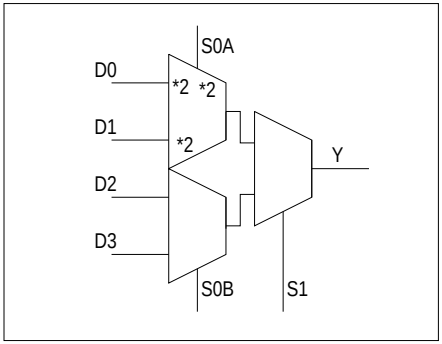
Inputs
S, A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* A 2 on the symbol implies a 2 logic module delay on all families except ACT1 and 40MX.

MXT



Function

Multiplexer with separate select lines

Truth Table

SOB	SOA	S1	Y
X	0	0	D0
X	1	0	D1
0	X	1	D2
1	X	1	D3

Inputs

D0 , D1, D2, D3, S0A, S0B, S1

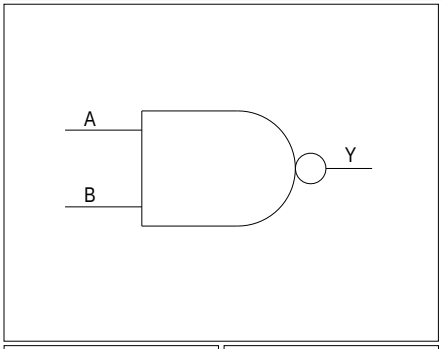
Outputs

Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		1
Others		2

* A 2 on the symbol implies a 2 logic module delay on all families except ACT 1 and 40MX.

NAND2



Function

2-Input NAND

Truth Table

A	B	Y
X	0	1
0	X	1
1	1	0

Inputs

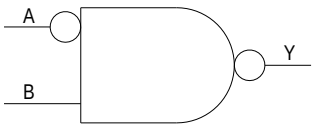
A, B

Outputs

Y

Family	Modules	
	Seq	Comb
All		1

NAND2A



Function
2-Input NAND with active low A-Input

Truth Table

A	B	Y
X	0	1
0	1	0
1	X	1

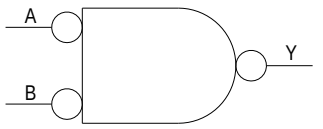
Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NAND2B



Function
2-Input NAND with active low Inputs

Truth Table

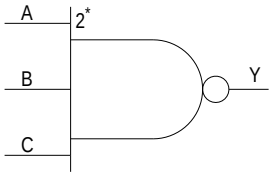
A	B	Y
0	0	0
X	1	1
1	X	1

Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NAND3



Function
3-Input NAND

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

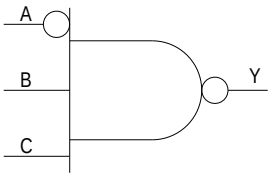
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

NAND3A



Function
3-Input NAND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	1	1	0
1	X	X	1

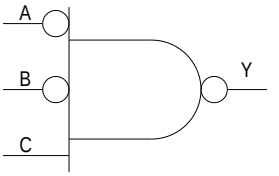
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NAND3B



Function
3-Input NAND with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	0
X	1	X	1
1	X	X	1

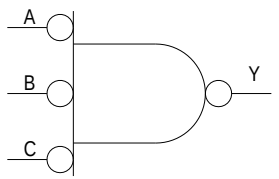
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NAND3C



Function
3-Input NAND with active low Inputs

Truth Table

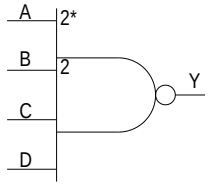
A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NAND4



Function
4-Input NAND

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

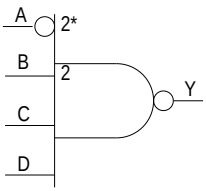
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except in 54SX.

NAND4A



Function
4-Input NAND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	1	1	1	0
1	X	X	X	1

Inputs
A, B, C, D

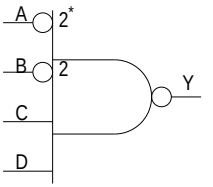
Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NAND4B



Function
4-Input NAND with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	1	1	0
X	1	X	X	1
1	X	X	X	1

Inputs
A, B, C, D

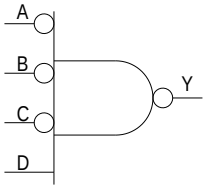
Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NAND4C



Function
4-Input NAND with active low A-, B- and C-Inputs

Truth Table

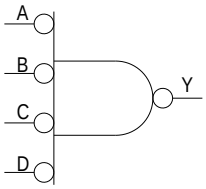
A	B	C	D	Y
X	X	X	0	1
0	0	0	1	0
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NAND4D



Function
4-Input NAND with active low Inputs

Truth Table

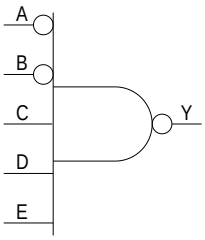
A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NAND5B



Function
5-input NAND with active low A- and B-inputs

Truth Table

A	B	C	D	E	Y
1	X	X	X	X	1
X	1	X	X	X	1
X	X	0	X	X	1
X	X	X	0	X	1
X	X	X	X	0	1
0	0	1	1	1	0

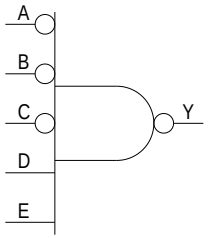
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

NAND5C



Function
5-Input NAND with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	E	Y
X	X	X	X	0	1
X	X	X	0	X	1
0	0	0	1	1	0
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1

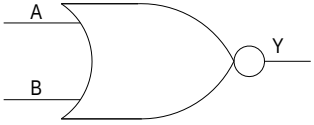
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NOR2



Function
2-Input NOR

Truth Table

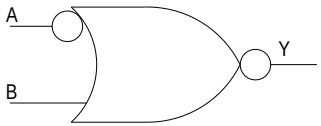
A	B	Y
0	0	1
X	1	0
1	X	0

Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOR2A



Function
2-Input NOR with active low A-Input

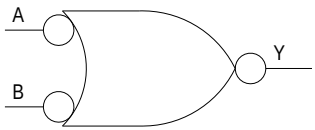
Truth Table

A	B	Y
0	X	0
1	0	1
X	1	0

Inputs	Outputs
A, B	Y

Family	Modules	
	Seq	Comb
All		1

NOR2B



Function
2-Input NOR with active low Inputs

Truth Table

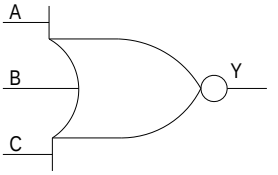
A	B	Y
X	0	0
0	X	0
1	1	1

Inputs	Outputs
A, B	Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NOR3



Function
3-Input NOR

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

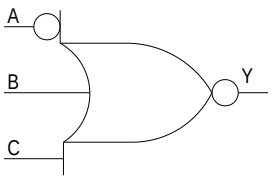
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NOR3A



Function
3-Input NOR with active low A-Input

Truth Table

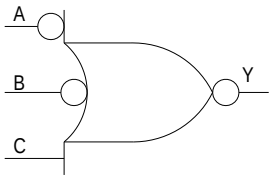
A	B	C	Y
0	X	X	0
1	0	0	1
X	X	1	0
X	1	X	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOR3B



Function
3-Input NOR with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	0	X	0
0	X	X	0
1	1	0	1
X	X	1	0

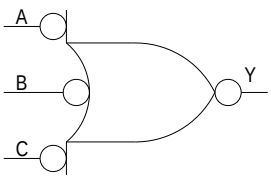
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NOR3C



Function
3-Input NOR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	0
X	0	X	0
0	X	X	0
1	1	1	1

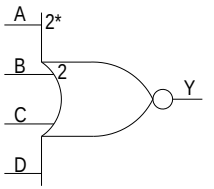
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NOR4



Function
4-Input NOR

Truth Table

A	B	C	D	Y
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Inputs
A, B, C, D

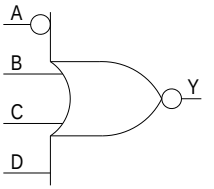
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except 54SX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NOR4A



Function
4-Input NOR with active low A-Input

Truth Table

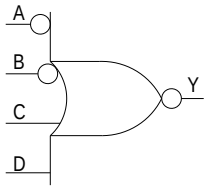
A	B	C	D	Y
0	X	X	X	0
1	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOR4B



Function
4-Input NOR with active low A- and B-Inputs

Truth Table

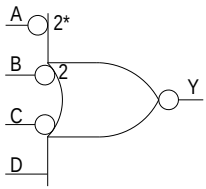
A	B	C	D	Y
X	0	X	X	0
0	X	X	X	0
1	1	0	0	1
X	X	X	1	0
X	X	1	X	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

NOR4C



Function
4-Input NOR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	0	1
X	X	X	1	0

Inputs
A, B, C, D

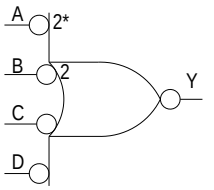
Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

NOR4D



Function
4-Input NOR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
X	0	X	X	0
0	X	X	X	0
1	1	1	1	1

Inputs
A, B, C, D

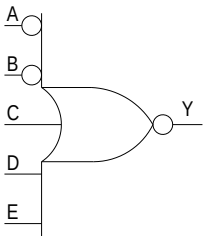
Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

54SX

NOR5B



Function
5-Input NOR with active low A- and B-Inputs

Truth Table

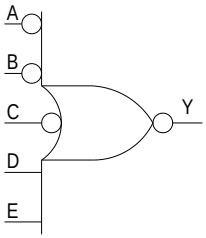
A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	1	X	X	0
X	X	X	0	X	0
X	X	X	X	1	0
1	1	0	0	0	1

Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

NOR5C



Function
5-Input NOR with active low A-, B- and C-Inputs

Truth Table

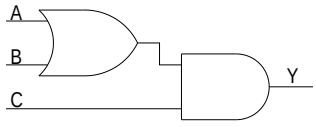
A	B	C	D	E	Y
0	X	X	X	X	0
X	0	X	X	X	0
X	X	0	X	X	0
X	X	X	1	X	0
X	X	X	X	1	0
1	1	1	0	0	1

Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OA1



Function
3 Input OR-AND

Truth Table

A	B	C	Y
X	X	0	0
0	0	X	0
X	1	1	1
1	X	1	1

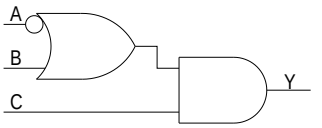
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OA1A



Function
3 Input OR-AND with active low A-Input

Truth Table

A	B	C	Y
X	X	0	0
0	X	1	1
1	0	X	0
X	1	1	1

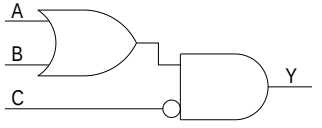
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OA1B



Function
3 Input OR-AND with active low C-Input

Truth Table

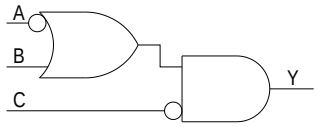
A	B	C	Y
0	0	X	0
X	1	0	1
X	X	1	0
1	X	0	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OA1C



Function
3 Input OR-AND with active low A- and C-Inputs

Truth Table

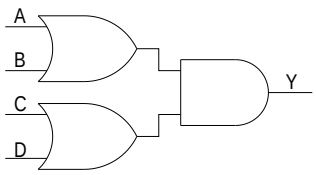
A	B	C	Y
0	X	0	1
X	X	1	0
1	0	X	0
X	1	0	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OA2



Function
2-wide 4-Input OR-AND

Truth Table

A	B	C	D	Y
X	X	0	0	0
0	0	X	X	0
X	1	X	1	1
X	1	1	X	1
1	X	X	1	1
1	X	1	X	1

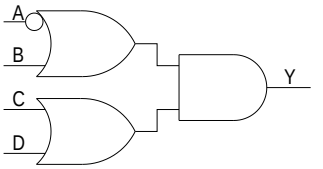
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OA2A



Function
2 wide 4-Input OR-AND with active low A-Input

Truth Table

A	B	C	D	Y
X	X	0	0	0
0	X	X	1	1
0	X	1	X	1
1	0	X	X	0
X	1	X	1	1
X	1	1	X	1

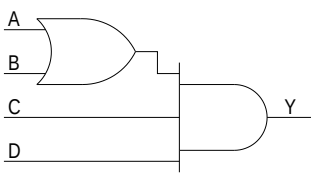
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OA3



Function
4 Input OR-AND

Truth Table

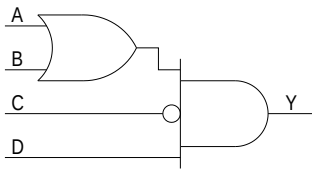
A	B	C	D	Y
X	X	X	0	0
X	X	0	X	0
0	0	X	X	0
X	1	1	1	1
1	X	1	1	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OA3A



Function
4 Input OR-AND with active low C-Input

Truth Table

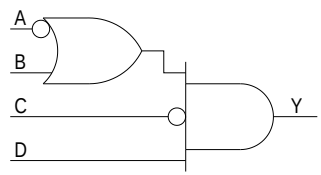
A	B	C	D	Y
X	X	X	0	0
0	0	X	X	0
X	1	0	1	1
X	X	1	X	0
1	X	0	1	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OA3B



Function
4 Input OR-AND with active low A- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	X	0	1	1
X	X	1	X	0
1	0	X	X	0
X	1	0	1	1

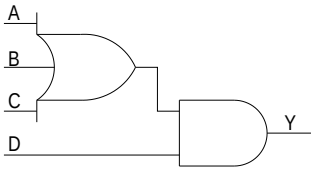
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

OA4



Function
4 Input OR-AND

Truth Table

A	B	C	D	Y
X	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	1	1

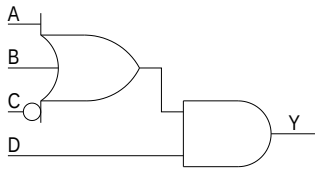
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OA4A



Function
4 Input OR-AND with active low C-Input

Truth Table

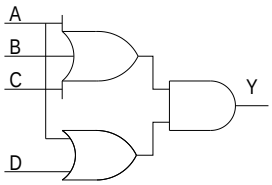
A	B	C	D	Y
X	X	X	0	0
X	X	0	1	1
0	0	1	X	0
X	1	X	1	1
1	X	X	1	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OA5



Function
4 Input complex OR-AND

Truth Table

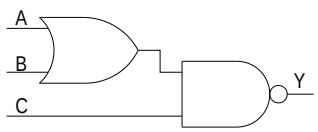
A	B	C	D	Y
0	X	X	0	0
0	0	0	X	0
X	X	1	1	1
X	1	X	1	1
1	X	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OAI1



Function
3 Input OR-AND-INVERT

Truth Table

A	B	C	Y
X	X	0	1
0	0	X	1
X	1	1	0
1	X	1	0

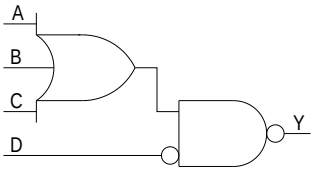
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OAI2A



Function
4 Input OR-AND-INVERT with active low D-Input

Truth Table

A	B	C	D	Y
0	0	0	X	1
X	X	1	0	0
X	X	X	1	1
X	1	X	0	0
1	X	X	0	0

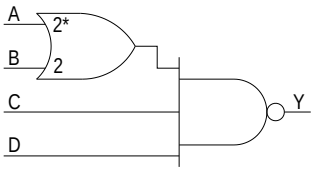
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OAI3



Function
4 Input OR-AND-INVERT

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
0	0	X	X	1
X	1	1	1	0
1	X	1	1	0

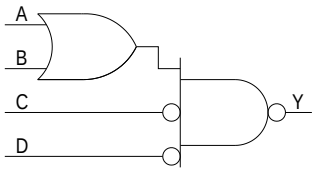
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OAI3A



Function
4 Input OR-AND-INVERT with active low C- and D-Inputs

Truth Table

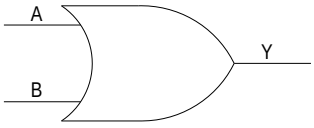
A	B	C	D	Y
0	0	X	X	1
X	1	0	0	0
X	X	X	1	1
X	X	1	X	1
1	X	0	0	0

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OR2



Function
2-Input OR

Truth Table

A	B	Y
0	0	0
X	1	1
1	X	1

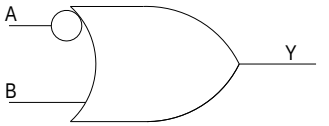
Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OR2A



Function
2-Input OR with active low A-Input

Truth Table

A	B	Y
0	X	1
1	0	0
X	1	1

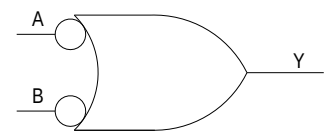
Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OR2B



Function
2-Input OR with active low Inputs

Truth Table

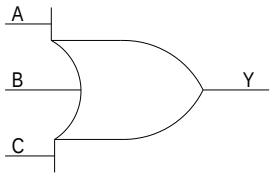
A	B	Y
X	0	1
0	X	1
1	1	0

Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OR3



Function
3-Input OR

Truth Table

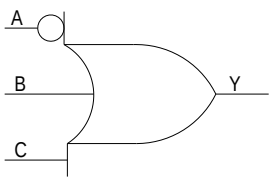
A	B	C	Y
0	0	0	0
X	X	1	1
X	1	X	1
1	X	X	1

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OR3A



Function
3-Input OR with active low A-Input

Truth Table

A	B	C	Y
0	X	X	1
1	0	0	0
X	X	1	1
X	1	X	1

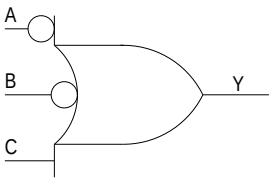
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OR3B



Function
3-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	Y
X	0	X	1
0	X	X	1
1	1	0	0
X	X	1	1

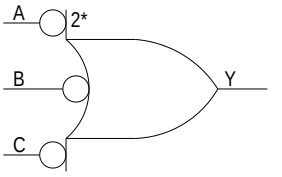
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OR3C



Function
3-Input OR with active low Inputs

Truth Table

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

Inputs
A, B, C

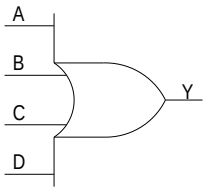
Outputs
Y

Combinational, OR

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4



Function
4-Input OR

Truth Table

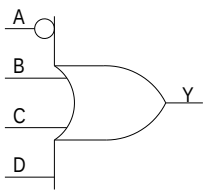
A	B	C	D	Y
0	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1
1	X	X	X	1

Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

OR4A



Function
4-Input OR with active low A-Input

Truth Table

A	B	C	D	Y
0	X	X	X	1
1	0	0	0	0
X	X	X	1	1
X	X	1	X	1
X	1	X	X	1

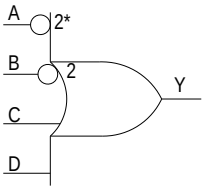
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OR4B



Function
4-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	D	Y
X	0	X	X	1
0	X	X	X	1
1	1	0	0	0
X	X	X	1	1
X	X	1	X	1

Inputs
A, B, C, D

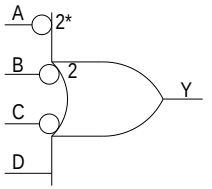
Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OR4C



Function
4-Input OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	Y
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	0	0
X	X	X	1	1

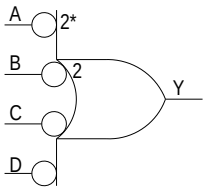
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
ACT 1/40MX		2
Others		1

* A 2 on the symbol implies 2 logic module delays only for ACT 1 and 40MX.

OR4D



Function
4-Input OR with active low Inputs

Truth Table

A	B	C	D	Y
X	X	X	0	1
X	X	0	X	1
X	0	X	X	1
0	X	X	X	1
1	1	1	1	0

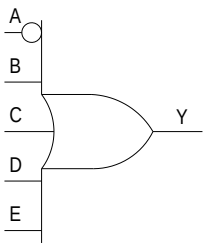
Inputs
A, B, C, D

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1
Others		2

* A 2 on the symbol implies 2 logic module delays except for 54SX.

OR5A



Function
5-Input OR with active low A- and B-Inputs

Truth Table

A	B	C	D	E	Y
0	X	X	X	1	1
X	1	X	X	X	1
X	X	1	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	0	0	0	0	0

Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ACT 2/1200XL

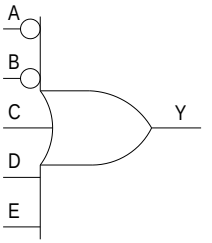
ACT 3

3200DX

42MX

54SX

OR5B



Function
5-Input OR with active low A-Input

Truth Table

A	B	C	D	E	Y
X	0	X	X	X	1
0	X	X	X	X	1
1	1	0	0	0	0
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1

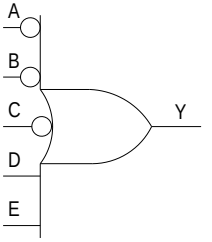
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

54SX

OR5C



Function
5-Input OR with active low A-, B- and C-Inputs

Truth Table

A	B	C	D	E	Y
0	X	X	X	X	1
X	0	X	X	X	1
X	X	0	X	X	1
X	X	X	1	X	1
X	X	X	X	1	1
1	1	1	0	0	0

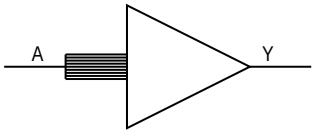
Inputs
A, B, C, D, E

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

QCLKINT

3200DX
42MX



Function
Internal Clock Interface

Truth Table

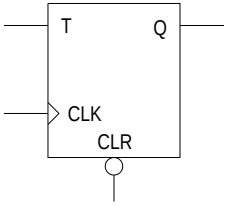
A	Y
0	0
1	1

Inputs	Outputs
A	Y

NOTE: QCLKINT does not use any modules.
For more information on the Global Clock Network, refer to Actel's Databook.

TF1A

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX



Function
T-Type Flip-Flop with active low Clear

Truth Table

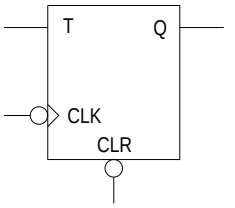
CLR	T	CLK	Q_{n+1}
0	X	X	0
1	1	↑	!Q
1	0	↑	Q

Inputs	Outputs
CLR, T, CLK	Q

Family	Modules	
	Seq	Comb
All	1	

ACT 2/1200XL
ACT 3
3200DX
42MX
54SX

TF1B



Function
T-Type Flip-Flop with active low Clear and Clock

Truth Table

CLR	T	CLK	Q_{n+1}
0	X	X	0
1	1	↓	!Q
1	0	↓	Q

Inputs
CLR, T, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All	1	

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

VCC

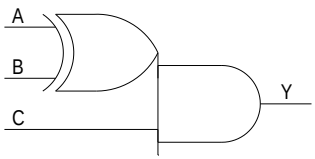
Function
Power

Inputs

Outputs
Y

NOTE: VCC does not use any module.

XA1



Function
3 Input XOR-AND

Truth Table

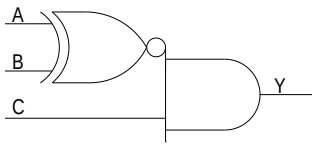
A	B	C	Y
X	X	0	0
0	0	X	0
0	1	1	1
1	0	1	1
1	1	X	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

XA1A



Function
3 Input XNOR-AND

Truth Table

A	B	C	Y
X	X	0	0
0	0	1	1
0	1	X	0
1	0	X	0
1	1	1	1

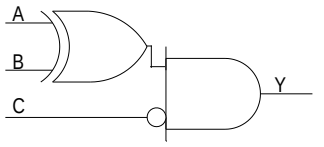
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

54SX

XA1B



Function
3 Input XNOR-AND with active low C-input

Truth Table

A	B	C	Y
X	X	1	0
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0

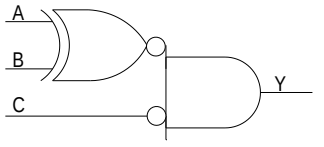
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

54SX

XA1C



Function
3 Input XNOR-AND with active low C-input

Truth Table

A	B	C	Y
X	X	1	0
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1

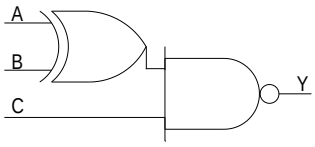
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

XAI1

54SX



Function
3 Input XNOR-NAND

Truth Table

A	B	C	Y
X	X	0	1
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

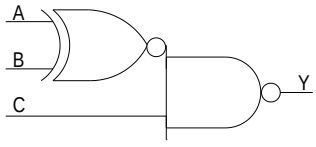
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

XAI1A

54SX



Function
3 Input XNOR-NAND

Truth Table

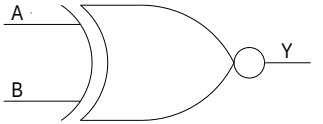
A	B	C	Y
X	X	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

XNOR2



Function
2 Input XNOR

Truth Table

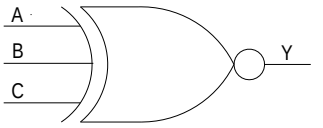
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Inputs
A, B Y

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

XNOR3



Function
3 Input XNOR

Truth Table

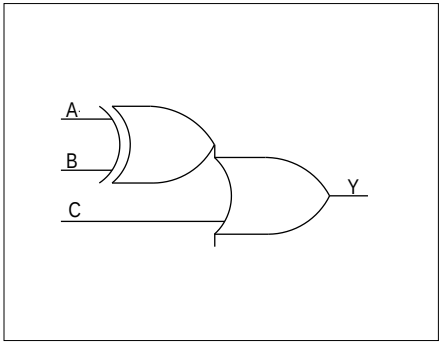
A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

XO1



Function
3 Input XOR-OR

Truth Table

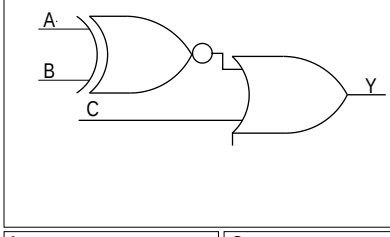
A	B	C	Y
0	0	0	0
X	X	1	1
0	1	X	1
1	0	X	1
1	1	0	0

Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

XO1A



Function
3 Input XOR-OR

Truth Table

A	B	C	Y
0	0	0	1
X	X	1	1
0	1	0	0
1	0	0	0
1	1	0	1

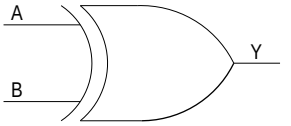
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

XOR2



Function
2 INput XOR

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

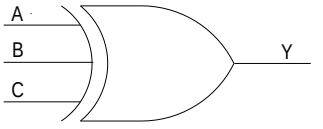
Inputs
A, B

Outputs
Y

Family	Modules	
	Seq	Comb
All		1

54SX

XOR3



Function
3 Input XOR

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	0
0	0	1	1
1	0	1	0
0	1	1	0
1	1	1	1

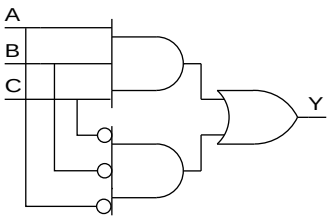
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ZOR3

54SX



Function
3 Input function

Truth Table

A	B	C	Y
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

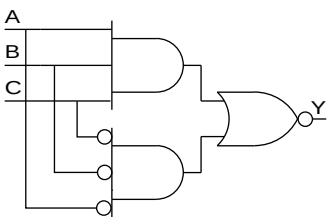
Inputs
A, B, C

Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

ZOR3I

54SX



Function
3 Input function

Truth Table

A	B	C	Y
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

Inputs
A, B, C

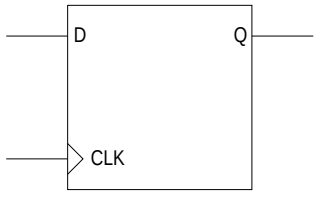
Outputs
Y

Family	Modules	
	Seq	Comb
54SX		1

CC-Module Flip Flops

These macros are useful in some radiation hostile applications. They sacrifice area in exchange for a lower single-event upset (SEU) rate caused by ion particle collisions. These special cells use two combinational modules to implement a register instead of using the dedicated registers in the array. (See the application note titled, *Design Techniques for RadHard Field Programmable Gate Arrays*.)

DF1_CC



Function
D-Type Flip-Flop

Truth Table

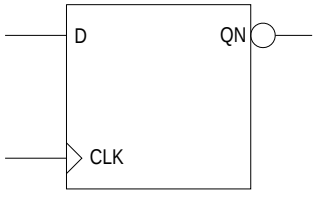
CLK	Q_{n+1}
↑	D

Inputs	Outputs
D, CLK	Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DF1A_CC



Function
D-Type Flip-Flop with active low Output

Truth Table

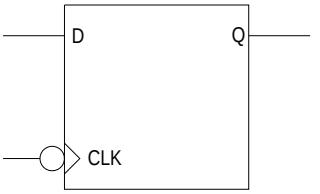
CLK	QN_{n+1}
↑	!D

Inputs	Outputs
D, CLK	QN

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DF1B_CC



Function
D-Type Flip-Flop with active low Clock

Truth Table

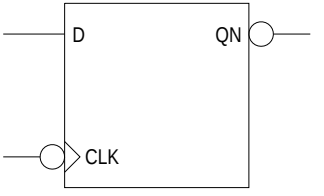
CLK	Q_{n+1}
↓	D

Inputs	Outputs
D, CLK	Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DF1C_CC



Function
D-Type Flip-Flop with active low Clock and Output

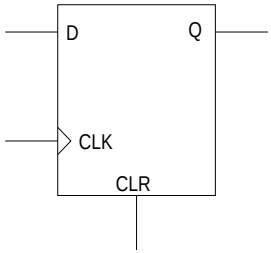
Truth Table

CLK	QN_{n+1}
↓	!D

Inputs	Outputs
D, CLK	QN

Family	Modules	
	Seq	Comb
All		2

DFC1_CC



Function
D-Type Flip-Flop, with active high Clear

Truth Table

CLR	CLK	Q_{n+1}
1	X	0
0	↑	D

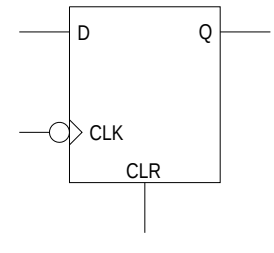
Inputs
CLR, D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFC1A_CC



Function
D-Type Flip-Flop, with active high Clear, and active low Clock

Truth Table

CLR	CLK	Q_{n+1}
1	X	0
0	↓	D

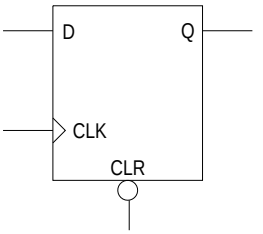
Inputs
CLR, D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFC1B_CC



Function
D-Type Flip-Flop, with active low Clear

Truth Table

CLR	CLK	Q_{n+1}
0	X	0
1	↑	D

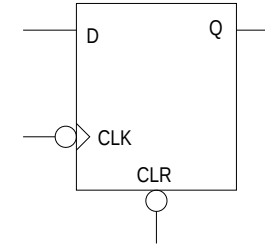
Inputs
CLR, D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFC1D_CC



Function
D-Type Flip-Flop, with active low Clear and Clock

Truth Table

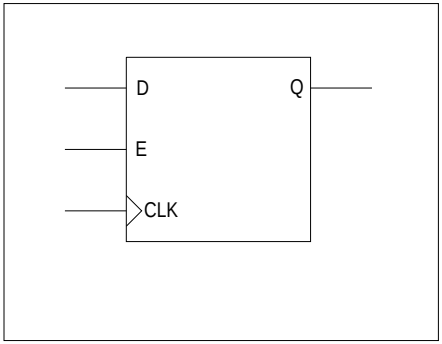
CLR	CLK	Q_{n+1}
0	X	0
1	↓	D

Inputs
CLR, D, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

DFE_CC



Function

D-Type Flip-Flop, with active high Enable

Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↑	D

Inputs

D, E, CLK

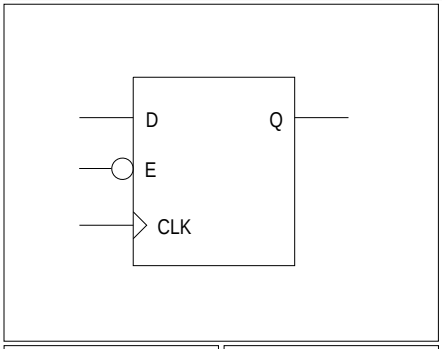
Outputs

Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFE1B_CC



Function

D-Type Flip-Flop, with active low Enable

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↑	D

Inputs

D, E, CLK

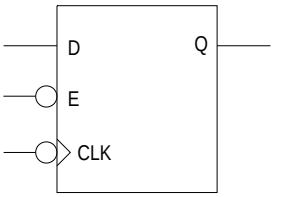
Outputs

Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFE1C_CC



Function
D-Type Flip-Flop, with active low Enable and Clock

Truth Table

E	CLK	Q_{n+1}
1	X	Q
0	↓	D

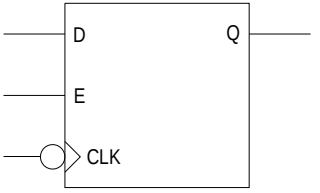
Inputs
D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFEA_CC



Function
D-Type Flip-Flop, with Enable, and active low Clock

Truth Table

E	CLK	Q_{n+1}
0	X	Q
1	↓	D

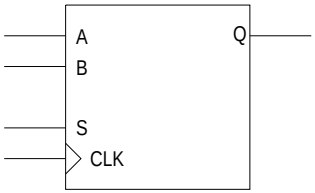
Inputs
D, E, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFM_CC



Function
D-Type Flip-Flop with 2-input Multiplexed Data

Truth Table

S	CLK	Q_{n+1}
0	↑	A
1	↑	B

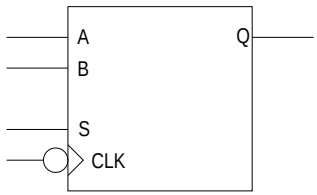
Inputs
A, B, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFMA_CC



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock

Truth Table

S	CLK	Q_{n+1}
0	↓	A
1	↓	B

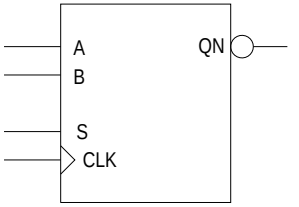
Inputs
A, B, S, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFM1B_CC



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Output

Truth Table

S	CLK	QN_{n+1}
0	↑	!A
1	↑	!B

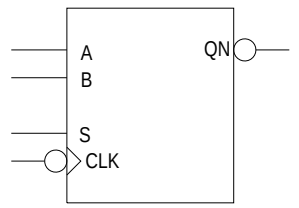
Inputs
A, B, S, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFM1C_CC



Function
D-Type Flip-Flop with 2-input Multiplexed Data, and active low Clock and Output

Truth Table

S	CLK	QN_{n+1}
0	↓	!A
1	↓	!B

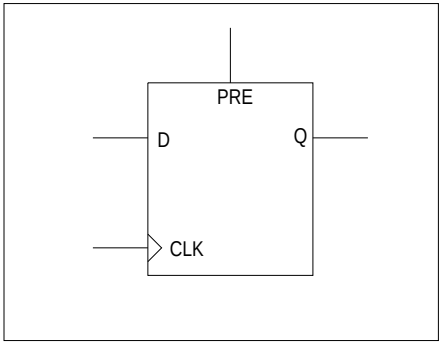
Inputs
A, B, S, CLK

Outputs
QN

Family	Modules	
	Seq	Comb
All		2

ACT 2/1200XL
ACT 3
3200DX
42MX

DFP1_CC*



Function
D-Type Flip-Flop with active high Preset

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↑	D

Inputs
D, PRE, CLK

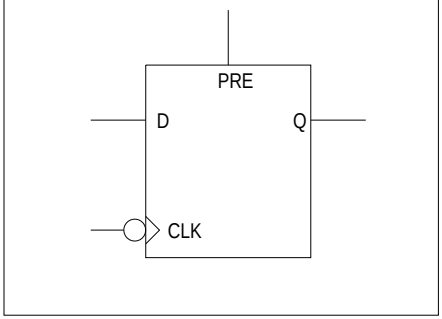
Outputs
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1.

ACT 2/1200XL
ACT 3
3200DX
42MX

DFP1A_CC*



Function
D-Type Flip-Flop with active high Preset, and active low Clock

Truth Table

PRE	CLK	Q_{n+1}
1	X	1
0	↓	D

Inputs
D, PRE, CLK

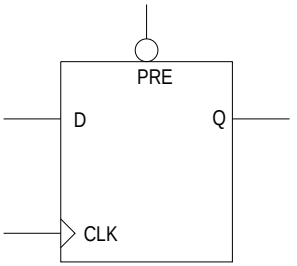
Outputs
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1A.

ACT 2/1200XL
ACT 3
3200DX
42MX

DFP1B_CC*



Function
D-Type Flip-Flop with active low Preset

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↑	D

Inputs
D, PRE, CLK

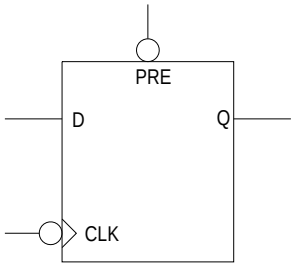
Outputs
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1B.

ACT 2/1200XL
ACT 3
3200DX
42MX

DFP1D_CC*



Function
D-Type Flip-Flop with active low Preset and Clock

Truth Table

PRE	CLK	Q_{n+1}
0	X	1
1	↓	D

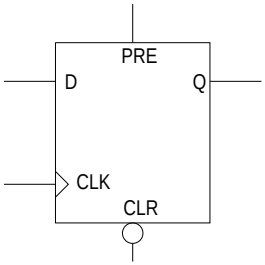
Inputs
D, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to macro DFP1D.

DFPC_CC*



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active high Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	X	X	0
1	1	X	1
1	0	↓	D

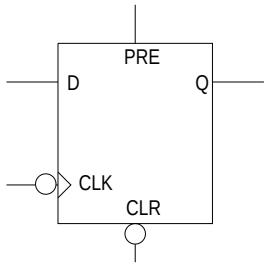
Inputs
CLR, D, PRE, CLK

Outputs
Q

Family	Modules	
	Seq	Comb
All		2

* Identical to DFPC

DFPCA_CC*



Function

D-Type Flip-Flop with active high Preset, active low Clear, and active low Clock

Truth Table

CLR	PRE	CLK	Q_{n+1}
0	0	X	0
1	1	X	1
1	0	↓	D
0	1	X	**

Inputs
CLR, D, PRE, CLK

Outputs
Q

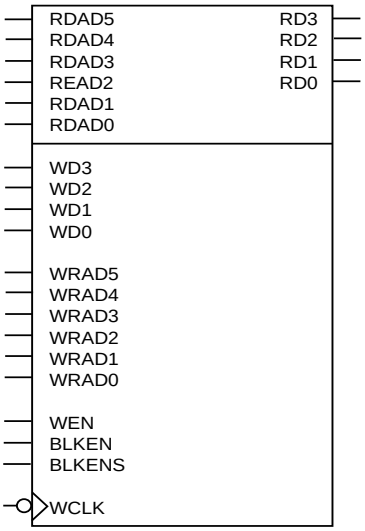
Family	Modules	
	Seq	Comb
All		2

* Identical to Macro DFPCA

** Your design should not allow both PRE and CLR to be asserted at the same time.

RAM Macros

RAM4FA



Function

64X4 dual-port RAM with falling Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

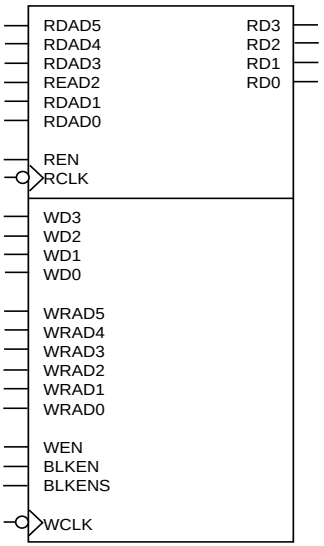
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM4FF



Function

64X4 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

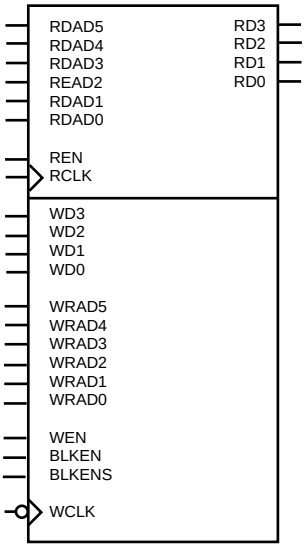
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM4FR



Function

64X4 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

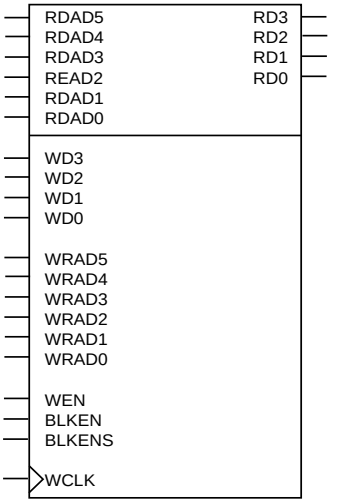
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM4RA



Function

64X4 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

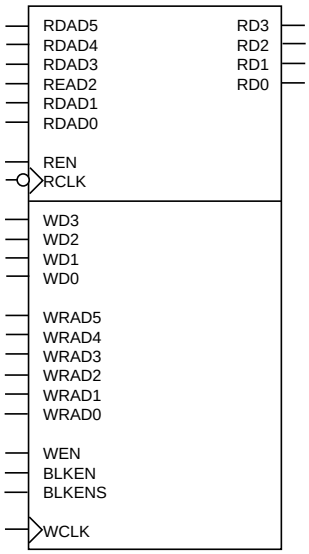
RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM4RF



Function

64X4 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

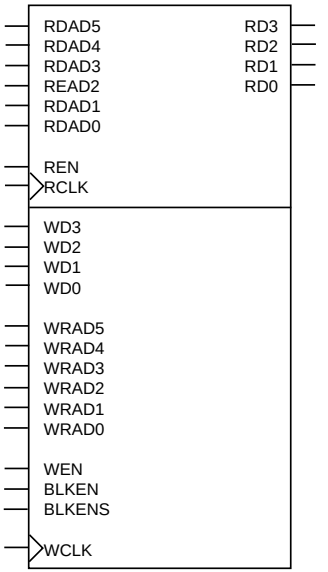
RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM4RR



Function

64X4 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Inputs

RDAD5, RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD5, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

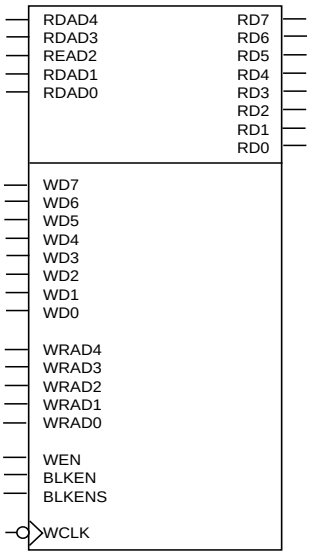
RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

RAM8FA



Function

32X8 dual-port RAM with falling Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

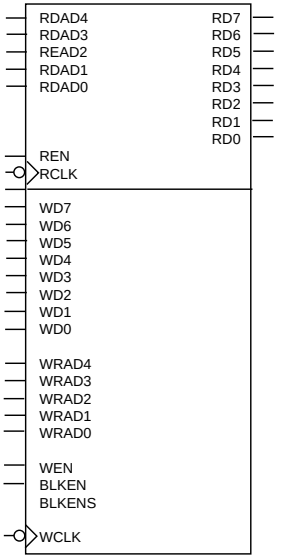
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM8FF



Function

32X8 dual-port RAM with falling Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

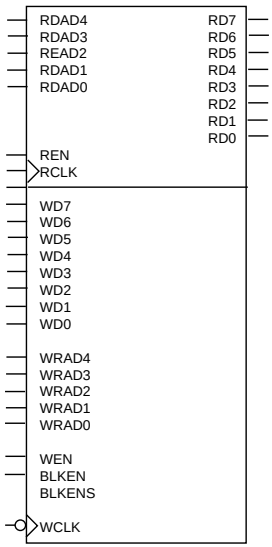
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM8FR



Function

32X8 dual-port RAM with falling Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↓	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

NOTE 1: BLKENS must be driven by a GND or VCC macro.

NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

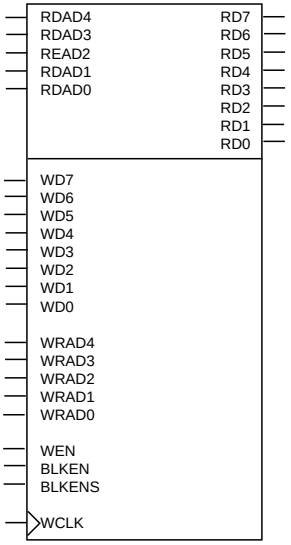
RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

3200DX

42MX

RAM8RA



Function

32X8 dual-port RAM with rising Write clock and asynchronous Read

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

NOTE 1: RDAD contents always appear at RD.

NOTE 2: BLKENS must be driven by a GND or VCC macro.

NOTE 3: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Inputs

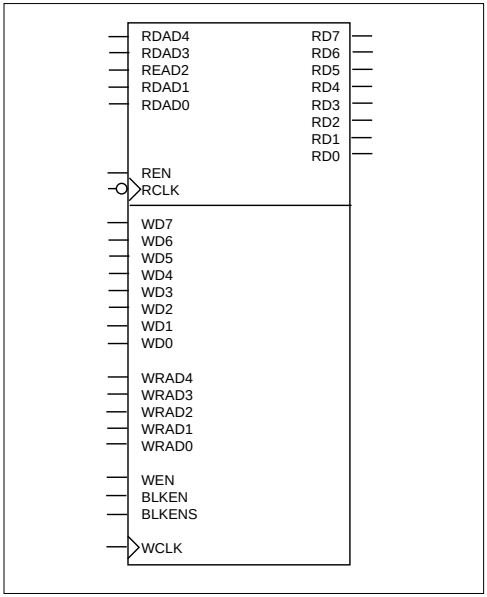
RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

RAM8RF



Function

32X8 dual-port RAM with rising Write clock and falling Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↓	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

NOTE 1: BLKENS must be driven by a GND or VCC macro.

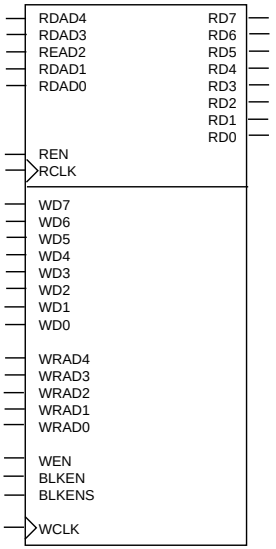
NOTE 2: The use of ACTgen RAM blocks is recommended over direct use of RAM macros because ACTgen includes buffering to achieve optimal performance.

Family	Modules
	RAM
All	1

3200DX

42MX

RAM8RR



Function

32X8 dual-port RAM with rising Write clock and rising Read clock

Write Truth Table

WCLK	BLKEN	WEN	Action
↑	BLKENS	1	WD written to WDAD
0	X	X	none
1	X	X	none
X	!BLKENS	X	none
X	X	0	none

Read Truth Table

RCLK	REN	Action
↑	1	RDAD contents appear at RD
0	X	RD is unchanged
1	X	RD is unchanged
X	0	RD is unchanged

Inputs

RDAD4, RDAD3, RDAD2, RDAD1, RDAD0, REN, RCLK, WD7, WD6, WD5, WD4, WD3, WD2, WD1, WD0, WRAD4, WRAD3, WRAD2, WRAD1, WRAD0, WEN, BLKEN, BLKENS, WCLK

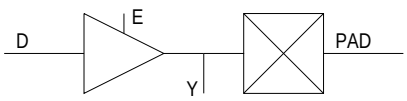
Outputs

RD7, RD6, RD5, RD4, RD3, RD2, RD1, RD0

Family	Modules
	RAM
All	1

I/O Macros

BIBUF



Function

Bidirectional Buffer, High Slew (with Hidden Buffer at Y pin)

Truth Table

MODE	E	D	PAD	Y
OUTPUT	1	X	D	D
INPUT	0	X	X	PAD

Inputs

D, E, PAD

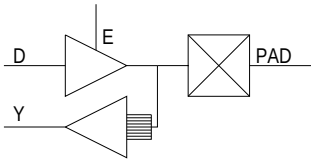
Outputs

PAD, Y

Family	Modules	
	Seq	I/O
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX

CLKBIBUF



Function
Biderctional with Input Dedicated to routed Clock Network

Truth Table

D	E	PAD	Y
X	0	Z	X
X	0	0	0
X	0	1	1
0	1	0	0
1	1	1	1

Inputs
D, E, PAD

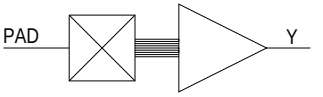
Outputs
PAD, Y

NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

CLKBUF



Function
Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

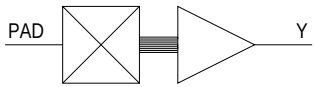
Inputs
PAD

Outputs
Y

NOTE 1: For an internal Clock net, refer to the CLKINT macro.
NOTE 2: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

HCLKBUF



Function
Dedicated high-speed S-Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

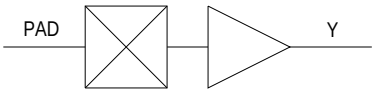
Inputs
PAD

Outputs
Y

NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

INBUF



Function
Input Buffer

Truth Table

PAD	Y
0	0
1	1

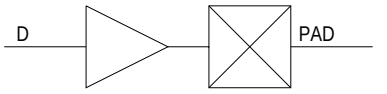
Inputs
PAD

Outputs
Y

Family	Modules	
	Seq	I/O
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

OUTBUF



Function
Output Buffer, High Slew

Truth Table

D	PAD
0	0
1	1

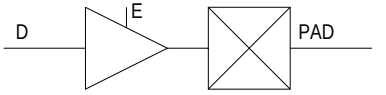
Inputs
D

Outputs
PAD

Family	Modules	
	Seq	I/O
All		1

ACT 1
ACT 2/1200XL
ACT 3
3200DX
40MX
42MX
54SX

TRIBUFF



Function
Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

Inputs
D, E

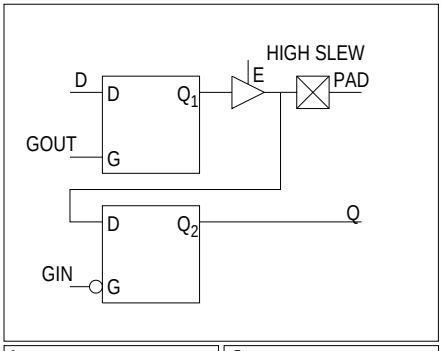
Outputs
PAD

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

Family	Modules	
	Seq	I/O
All		1

ACT 2/XL/DX/42MX I/O Macros

BBDLHS



Function
Bidirectional with Input Latch and Output Latch

Truth Table

MODE	E	GOUT	GIN	PAD	Q
OUTPUT	1	0	1	PAD_{n-1}	Q_{n-1}
	1	1	0	D	D
INPUT	0	X	1	X	Q_{n-1}
	0	X	0	X	PAD

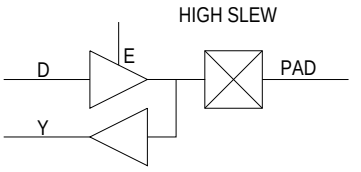
Inputs
D, E, GOUT, GIN, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX

BBHS



Function
Bidirectional Buffer, High Slew

Truth Table

MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Inputs
D, E, PAD

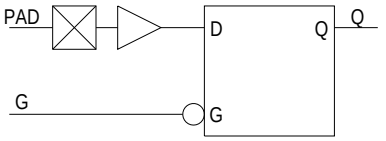
Outputs
PAD, Y

Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of BBHS we recommend that you use BIBUF on page 221.

ACT 2/1200XL
3200DX
42MX

IBDL



Function
Input Buffer with Input Latch, with active low Clock

Truth Table

G	Q
1	Q_{n-1}
0	PAD

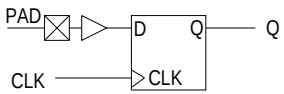
Inputs
G, PAD

Outputs
Q

Family	Modules	
	Seq	I/O
All		1

IR

ACT 2/1200XL
3200DX
42MX



Function
Input Register

Truth Table

CLK	Q
↑	PAD

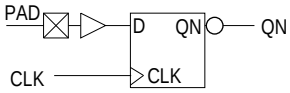
Inputs
PAD, CLK

Outputs
Q

Family	Modules	
	Seq	I/O
All	1	1

IRI

ACT 2/1200XL
3200DX
42MX



Function
Input register with active Low output

Truth Table

CLK	QN
↑	!PAD

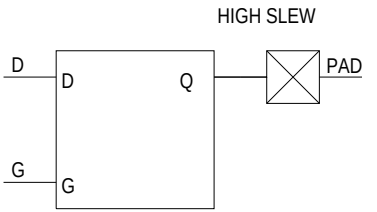
Inputs
PAD, CLK

Outputs
QN

Family	Modules	
	Seq	I/O
All	1	1

ACT 2/1200XL
3200DX
42MX

OBDLHS



Function
Output Buffer with Output Latch, High Slew

Truth Table

G	PAD
0	PAD_{n-1}
1	D

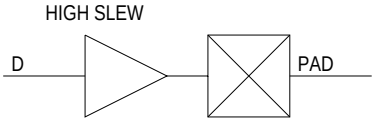
Inputs
D, G

Outputs
PAD

Family	Modules	
	Seq	I/O
All		1

ACT 2/1200XL
ACT 3
3200DX
42MX

OBHS



Function
Output Buffer, High Slew

Truth Table

D	PAD
0	0
1	1

Inputs
D

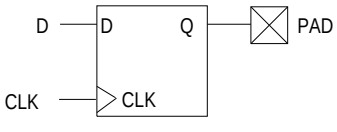
Outputs
PAD

Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of OBHS we recommend that you use OUTBUF on page 224.

ORH

ACT 2/1200XL
3200DX
42MX



Function
Output Register, High Slew

Truth Table

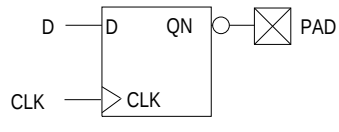
CLK	PAD_{n+1}
↑	D

Inputs	Outputs
D, CLK	PAD

Family	Modules	
	Seq	I/O
All	1	1

ORIH

ACT 2/1200XL
3200DX
42MX



Function
Inverted Output Register, High Slew

Truth Table

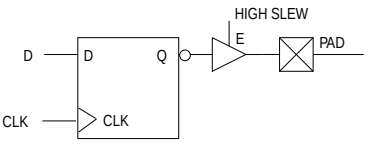
CLK	PAD_{n+1}
↑	!D

Inputs	Outputs
D, CLK	PAD

Family	Modules	
	Seq	I/O
All	1	1

ACT 2/1200XL
3200DX
42MX

ORITH



Function
Inverted Output Register, Tristate Enable, High Slew

Truth Table

E	CLK	PAD_{n+1}
0	X	Z
1	↑	!D

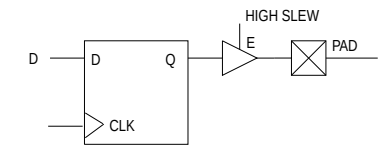
Inputs
D, E, CLK

Outputs
PAD

Family	Modules	
	Seq	I/O
All	1	1

ACT 2/1200XL
3200DX
42MX

ORTH



Function
Output Register, Tristate Enable, High Slew

Truth Table

E	CLK	PAD_{n+1}
0	X	Z
1	↑	D

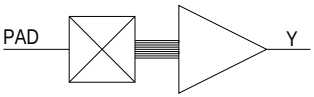
Inputs
D, E, CLK

Outputs
PAD

Family	Modules	
	Seq	I/O
All	1	1

QCLKBUF

3200DX
42MX



Function
Input for Dedicated Routed Clock Network

Truth Table

PAD	Y
0	0
1	1

Inputs
PAD

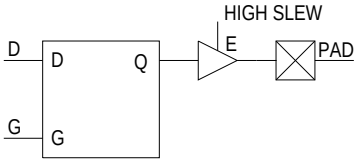
Outputs
Y

NOTE 1: For an internal Clock net, refer to the CLKINT macro.
NOTE 2: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
All		1

TBDLHS

ACT 2/1200XL
3200DX
42MX



Function
Tristate Output with Latch, High Slew

Truth Table

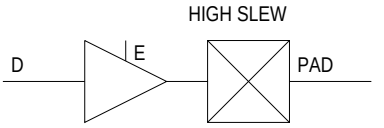
E	G	PAD
0	X	Z
1	1	D
1	0	PAD_{n-1}

Inputs
D, E, G

Outputs
PAD

Family	Modules	
	Seq	I/O
All		1

TBHS



Function
Tristate Output, High Slew

Truth Table

E	PAD
0	Z
1	D

Inputs
D, E

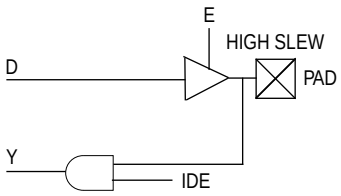
Outputs
PAD

NOTE: Refer to Actel's Databook for internal tristate implementation using multiplexers.

Family	Modules	
	Seq	I/O
All		1

NOTE: For new designs, instead of TBHS we recommend that you use TRIBUFF on page 224.

BBHSA



Function
Bidirectional buffer with AND gate, High Slew

Truth Table

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

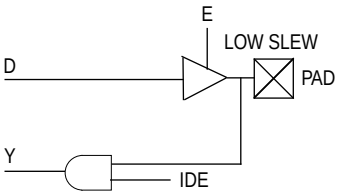
Inputs
D, E, IDE, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BBLSA



Function
Bidirectional buffer with AND gate, Low Slew

Truth Table

MODE	E	IDE	PAD	Y
OUTPUT	1	1	D	D
	1	0	D	0
INPUT	0	1	X	PAD
	0	0	X	0

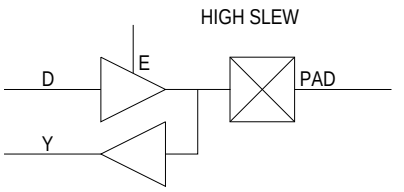
Inputs
D, E, IDE, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BBUFTH



Function
Bidirectional Buffer, Tristate Enable, High Slew

Truth Table

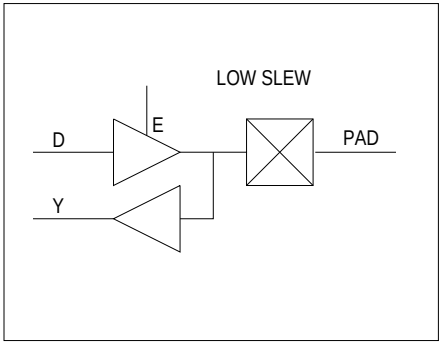
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Inputs
D, E, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BBUFTL



Function
Bidirectional Buffer, Tristate Enable, Low Slew

Truth Table

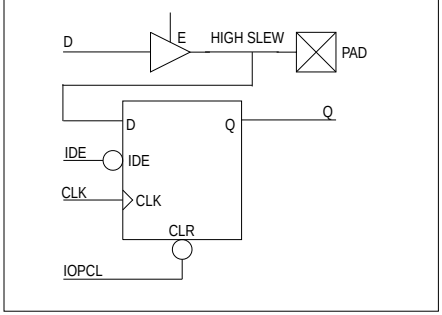
MODE	E	PAD	Y
OUTPUT	1	D	D
INPUT	0	X	PAD

Inputs
D, E, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BIECTH



Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

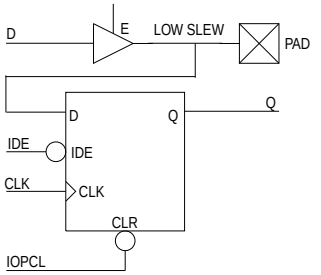
Inputs
D, E, IDE, CLK, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BIECTL



Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	0
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	0
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

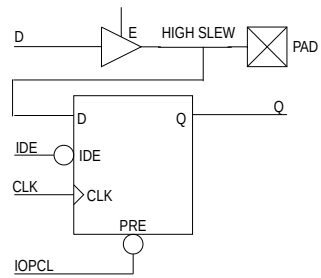
Inputs
D, E, IDE, CLK, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BIEPTH



Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, High Slew

Truth Table

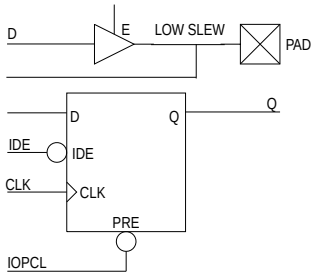
MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

Inputs
D, E, IDE, CLK, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BIEPTL



Function
Bidirectional Input Register with Clear, Input Data Enable, Tristate Enable, Low Slew

Truth Table

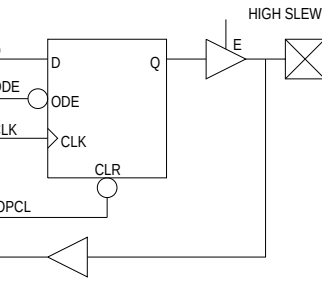
MODE	E	IOPCL	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	D	1
	1	1	0	↑	D	D
	1	1	1	↑	D	Q_{n-1}
INPUT	0	0	X	X	X	1
	0	1	0	↑	X	PAD
	0	1	1	↑	X	Q_{n-1}

Inputs
D, E, IDE, CLK, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

BRECTH



Function
Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

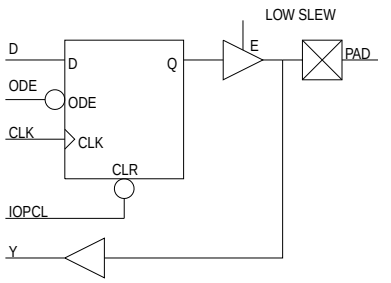
Inputs
CLK, D, ODE, IOPCL, E, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BRECTL



Function
Bidirectional Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	0	0
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

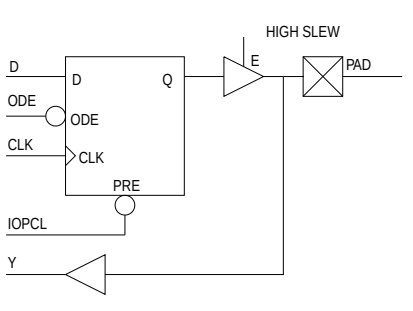
Inputs
CLK, D, ODE, IOPCL, E, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

BREPTH



Function
Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

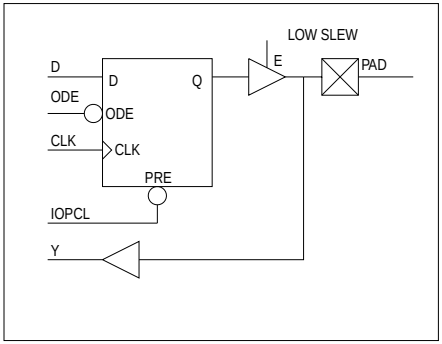
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Inputs
CLK, D, ODE, IOPCL, E, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

BREPTL



Function
Bidirectional Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

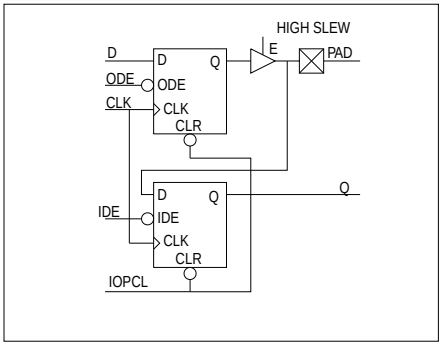
MODE	E	IOPCL	ODE	CLK	PAD	Y
OUTPUT	1	0	X	X	1	1
	1	1	1	↑	PAD_{n-1}	Y_{n-1}
	1	1	0	↑	D	D
INPUT	0	X	X	X	X	PAD

Inputs
CLK, D, ODE, IOPCL, E, PAD

Outputs
PAD,. Y

Family	Modules	
	Seq	I/O
ACT 3		1

DECETH



Function
Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q_{n-1}

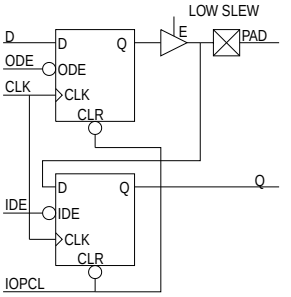
Inputs
D, E, ODE, CLK, IDE, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

DECETL



Function
Bidirectional Double Registered, with Clear, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Truth Table

MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	0	0
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	0
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q_{n-1}

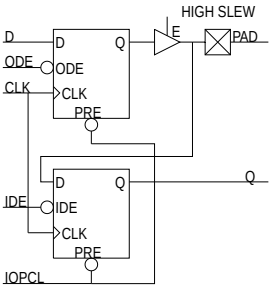
Inputs
D, E, ODE, CLK, IDE, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

DEPETH



Function
Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, High Slew, Output Data Enable

Truth Table

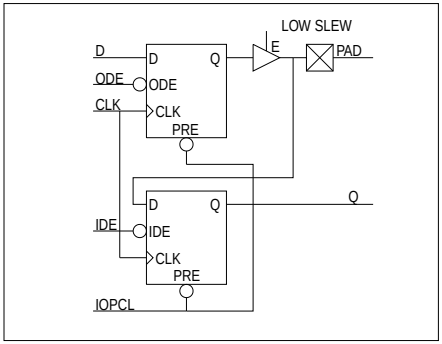
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q_{n-1}

Inputs
D, E, ODE, CLK, IDE, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

DEPETL



Function
Bidirectional Double Registered, with Preset, Input Data Enable, Tristate Enable, Low Slew, Output Data Enable

Truth Table

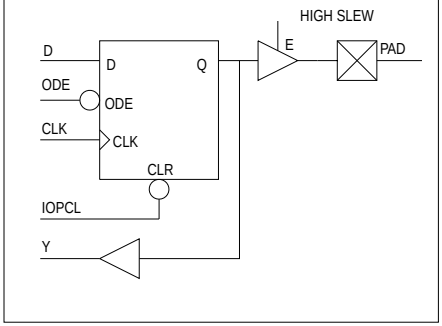
MODE	E	IOPCL	ODE	IDE	CLK	PAD	Q
OUTPUT	1	0	X	X	X	1	1
	1	1	0	0	↑	D	PAD
	1	1	1	1	↑	PAD_{n-1}	Q_{n-1}
INPUT	0	0	X	X	X	X	1
	0	1	X	0	↑	X	PAD
	0	1	X	1	↑	X	Q_{n-1}

Inputs
D, E, ODE, CLK, IDE, IOPCL, PAD

Outputs
PAD, Q

Family	Modules	
	Seq	I/O
ACT 3		1

FECTH



Function
Output Register with feedback, Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

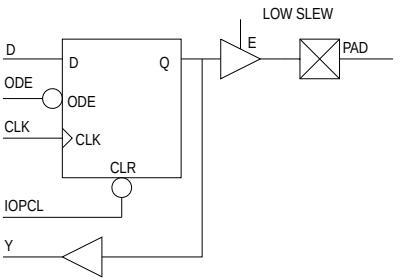
Inputs
D, E, ODE, CLK, IOPCL, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FECTL



Function
Output Register with feedback, Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	0	0
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	0	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

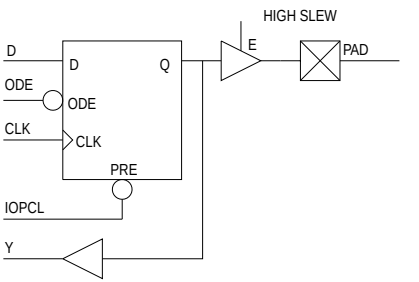
Inputs
D, E, ODE, CLK, IOPCL, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FEPTH



Function
Output Register with feedback, Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

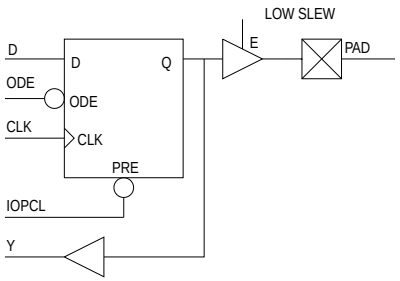
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Inputs
D, E, ODE, CLK, IOPCL, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTL



Function
Output Register with feedback, Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

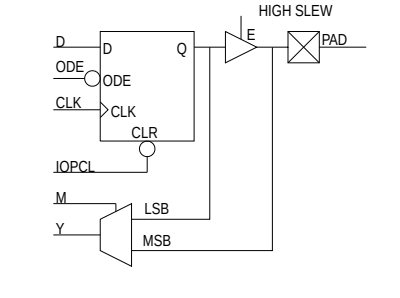
E	IOPCL	ODE	CLK	Y	PAD
1	0	X	X	1	1
1	1	0	↑	D	D
1	1	1	X	Y_{n-1}	Y_{n-1}
0	0	X	X	1	Z
0	1	0	↑	D	Z
0	1	1	X	Y_{n-1}	Z

Inputs
D, E, ODE, CLK, IOPCL, PAD

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

FECTMH



Function
Output Register with Muxed Feedback, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

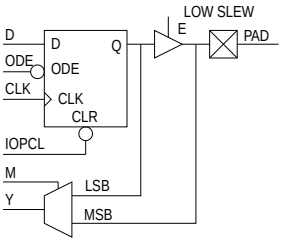
Inputs
D, E, ODE, CLK, IOPCL, PAD, M

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FECTML



Function
Output Register with Muxed Feedback, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	0	X	0
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

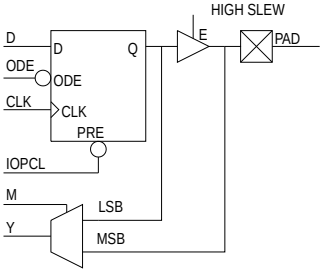
Inputs
D, E, ODE, CLK, IOPCL, PAD , M

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

FEPTMH



Function
Output Register with Muxed Feedback, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

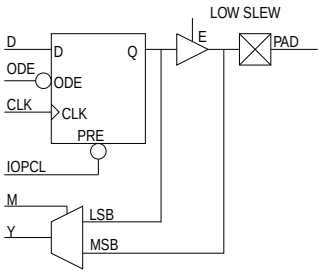
NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

Inputs
D, E, ODE, CLK, IOPCL, PAD, M

Outputs
PAD, Y

Family	Modules	
	Seq	I/O
ACT 3		1

FEPTML



Function
Output Register with Muxed Feedback, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

MODE	E	IOPCL	ODE	CLK	PAD	M	Y
OUTPUT	1	0	X	X	1	X	1
	1	1	0	↑	D	X	D
	1	1	1	↑	PAD_{n-1}	X	Y_{n-1}
INPUT	0	1	0	↑	X	0	D
	0	1	X	X	X	1	PAD

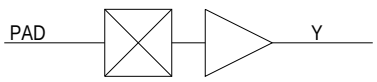
Inputs
D, E, ODE, CLK, IOPCL, PAD, M

Outputs
PAD, Y

NOTE: When M = 0, LSB is selected. When M = 1, MSB is selected.

Family	Modules	
	Seq	I/O
ACT 3		1

IBUF



Function
Input Buffer

Truth Table

PAD	Y
0	0
1	1

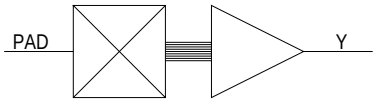
Inputs
PAD

Outputs
Y

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

IOCLKBUF



Function
Dedicated I/O Module Clock Buffer

Truth Table

PAD	Y
0	0
1	1

Inputs
PAD

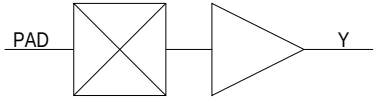
Outputs
Y

NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

IOPCLBUF



Function
Dedicated I/O Preset Clear Buffer

Truth Table

PAD	Y
0	0
1	1

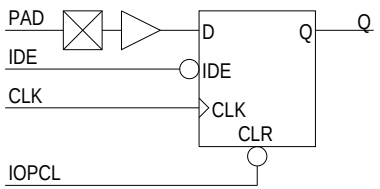
Inputs
PAD

Outputs
Y

NOTE: Refer to Actel's Databook for more Clock Network information.

Family	Modules	
	Seq	I/O
ACT 3		1

IREC



Function
Input Register, with Clear, Input Data Enable

Truth Table

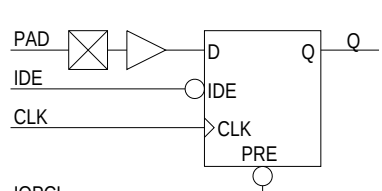
IOPCL	IDE	CLK	Q_{n+1}
0	X	X	0
1	1	X	Q
1	0	↑	PAD

Inputs
PAD, IDE, CLK, IOPCL

Outputs
Q

Family	Modules	
	Seq	I/O
ACT 3		1

IREP



Function
Input Register, with Preset, Input Data Enable

Truth Table

IOPCL	IDE	CLK	Q_{n+1}
0	X	X	1
1	1	X	Q
1	0	↑	PAD

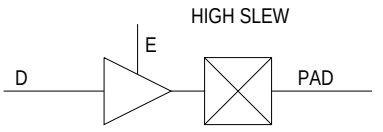
Inputs
PAD, IDE, CLK, IOPCL

Outputs
Q

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

OBUFTH



Function
Output Buffer, Tristate Enable, High Slew

Truth Table

D	E	PAD
X	0	Z
0	1	0
1	1	1

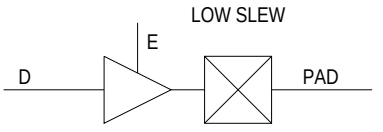
Inputs
D, E

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

OBUFTL



Function
Output Buffer, Tristate Enable, Low Slew

Truth Table

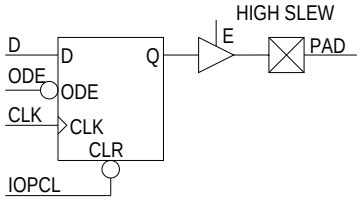
D	E	PAD
X	0	Z
0	1	0
1	1	1

Inputs
D, E

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTH



Function
Output Register, with Clear, Output Data Enable, Tristate Enable, High Slew

Truth Table

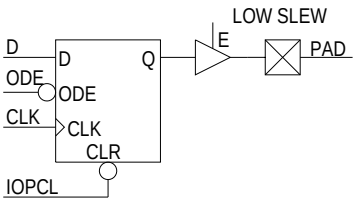
IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

Inputs
D, ODE, CLK, IOPCL, E

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ORECTL



Function
Output Register, with Clear, Output Data Enable, Tristate Enable, Low Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	0
X	0	X	X	Z
1	1	0	↑	D

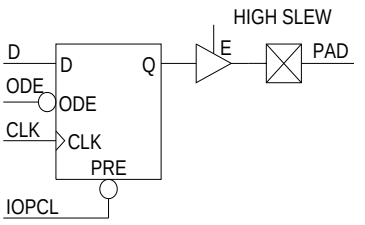
Inputs
D, E, ODE, CLK, IOPCL

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

OREPTH



Function
Output Register, with Preset, Output Data Enable, Tristate Enable, High Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

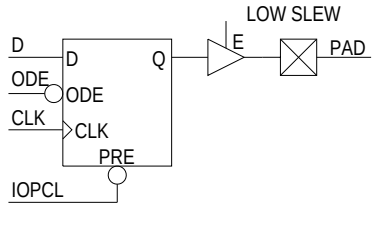
Inputs
D, E, ODE, CLK, IOPCL

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1

ACT 3

OREPTL



Function
Output Register, with Preset, Output Data Enable, Tristate Enable, Low Slew

Truth Table

IOPCL	E	ODE	CLK	PAD
0	1	X	X	1
X	0	X	X	Z
1	1	0	↑	D

Inputs
D, E, ODE, CLK, IOPCL

Outputs
PAD

Family	Modules	
	Seq	I/O
ACT 3		1