Mentor Graphics®

Interface Guide

Actel

UNIX ® Environments

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Introduction

This *Mentor Graphics Interface Guide* contains detailed information about using Mentor Graphics software to create designs for Actel devices. Refer to the *Designing with Actel* manual for additional information about using the Designer software and the Mentor Graphics documentation for information about using Mentor Graphics tools.

Document Organization

The *Mentor Graphics Interface Guide* is divided into the following chapters:

Chapter 1 - Setup contains information and procedures about setting up Mentor Graphics tools to create Actel Designs.

Chapter 2 - Actel-Mentor Graphics Design Flow illustrates and describes the design flow for creating Actel Designs using Mentor Graphics CAE tools.

Chapter 3 - Actel-Design Architect Design Considerations contains information and procedures to allow you to create designs with Design Architect.

Chapter 4 - Simulation Using QuickSim II contains information and procedures about simulating Actel designs with QuickSim II.

Chapter 5 - Static Timing Analysis Using QuickPath contains information and procedures about static timing analysis with QuickPath.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Assumptions

The information in this manual is based on the following assumptions:

1. You have installed the Designer Series software.
2. You have installed the Mentor Graphics software.
3. You are familiar with UNIX operating system environments.
4. You are familiar with Actel FPGA architecture and Actel design software.

Document Conventions

The following conventions are used throughout this manual.

Information that is meant to be input by the user is formatted as follows:

```
keyboard input
```

The contents of a file is formatted as follows:

```
file contents
```

Messages that are displayed on the screen appear as follows:

```
Screen Message
```

The following variables are used throughout this manual.

- Actel FPGA family libraries are shown as <act_fam>. Substitute the desired Actel FPGA family (act1, act2 (for ACT 2 and 1200XL devices), act3, 3200dx, 40mx, 42mx, and 54sx) as needed. For example:

  ```
  mgc2edn fam:<act_fam> <design_name>
  ```

- The Actel installation directory is shown as <alsdir>.

Designer Series Manuals

The Designer Series software includes printed and on-line manuals. The on-line manuals are in PDF format on the CD-ROM in the "/doc" directory. These manuals are also installed onto your system when you install the Designer software. To view the on-line manuals, you must have Adobe® Acrobat Reader® installed. Actel provides Reader on the Designer Series CD-ROM.

The Designer Series includes the following manuals, which provide additional information on designing Actel FPGAs:

Designing with Actel. This manual describes the design flow and user interface for the Actel Designer Series software, including information about using the ACTgen Macro Builder and ACTmap VHDL Synthesis software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

ACTmap VHDL Synthesis Methodology Guide. This guide contains information, optimization techniques, and procedures to assist designers in the design of Actel devices using ACTmap VHDL.

Silicon Expert User's Guide. This guide contains information and procedures to assist designers in the use of Actel's Silicon Expert tool.

Cadence® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

MOTIVE™ Static Timing Analysis Interface Guide. This guide contains information and procedures to assist designers in the use of the MOTIVE software to perform static timing analysis on Actel designs.

Synopsys® Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information and procedures to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Viewlogic® Powerview Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Powerview CAE software and the Designer Series software.

Viewlogic Workview® Office Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Workview Office CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog® Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Silicon Explorer Quick Start. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Designer Series Development System Conversion Guide UNIX® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for UNIX to be compatible with later versions of Designer Series.

Designer Series Development System Conversion Guide Windows® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for Windows to be compatible with later versions of Designer Series.

FPGA Data Book and Design Guide. This guide contains detailed specifications on Actel device families. Information such as propagation delays, device package pinout, derating factors, and power calculations are found in this guide.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

1

Setup

This chapter contains information about setting up Mentor Graphics software to create Actel designs.

Included in this chapter are software requirements, details about how to set up your UNIX account to access Actel and Mentor Graphics software, and details about how to launch individual applications using the Mentor Graphics Design Manager icons. Refer to the Mentor Graphics documentation for detailed information about using Mentor Graphics software.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R2-1998 or later, and the following third party software:

- **Mentor Graphics software,** including Design Architect, DVE, QuickSim II, QuickPath, and QuickHDL.
- **Synopsys Integrator,** which is required for integrating Synopsys designs with Mentor Graphics using Actel libraries.

For specific information about which versions are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

User Setup

Before you create designs with the Actel library, you must set up your account to properly access the Actel and Mentor Graphics software. The following sections describe how to configure your user account for Designer Series in the Mentor Graphics environment for the C-Shell.

Note For Designer Series environment setup, refer to the *Designing With Actel* manual.

Creating an MGC Location Map File

The MGC Location Map file is an ASCII file that maps soft prefixes to hard path names. It allows flexibility in managing designs in both homogeneous and heterogeneous networks. With location maps, designs can be moved to different directories, and/or different workstations without changing internal design references.

The MGC Location Map file is required by the Mentor Graphics tools to determine relative path names. The Mentor Graphics and Actel tools locate this file with the MGC_LOCATION_MAP environment variable. Other variables, including the $MGC_GENLIB variable are declared in the MGC Location Map file.

The MGC Location Map file is user-definable. The name that you give this file is inconsequential as long as you reference its locations correctly in the MGC_LOCATION_MAP environment variable. See "Configuring User's Accounts for the C-Shell" on page 5, for details.

To create an MGC Location Map file:

To create an MGC Location Map file, follow the design of the listing for the MGC_LOCATION_MAP file provided as follows:

```
MGC_LOCATION_MAP_1
$ALSDIR
<alsdir>
$MGC_GENLIB
<mentor_lib_dir>/gen_lib
$MYDESIGNS
<project_dir>
```

For Design Manager encapsulation, include the following:

```
$ALS_TOOLBOX
<alsdir>/lib/me/toolbox
```

For more information regarding location maps, refer to your Mentor Graphics documentation.

Mentor Graphics Library Organization

In addition to the standard Actel libraries, Actel provides a set of migration macros. These are macros that were supported in earlier versions of the Designer Series software and macros that may be needed to retarget designs to a different Actel family. Actel does not recommend using migration macros in new designs

Standard libraries

In the Mentor Graphics design kit, standard libraries are located in $ALSDIR/lib/mgc/<act_fam>. Migration macros are located in different locations for different families. For families that did not exist as of Actel Software release R1-1998, migration macros are in $ALSDIR/lib/mgc/<act_fam>_mig.

Legacy library

Migration macros are included in the legacy library for families that existed as of Actel Software release R1-1998. The legacy library is a single shared library located in $ALSDIR/lib/me. The legacy library was the only Mentor Graphics library in Actel Software release R1-1998 and previous releases. You may still use the legacy library for old designs. Blocks containing legacy macros may be mixed with blocks containing macros from the standard library.

Environment Variable Summary Check List

Before you continue, make sure that you have set the necessary environment variables.

Table 1-1, “Environment Variables,” shows the variables for all UNIX shell types. For details, see “User Setup” on page 1.

Table 1-1. Environment Variables

Variable	Description
☐ ALSDIR	The directory where you have installed the Designer software.
☐ MGC_HOME	The directory where you have installed the Mentor Graphics software.
☐ PATH	The path to access the Designer Series and Mentor Graphics binary files.
☐ AMPLE_PATH	The directory where you have installed the Actel userware. Directory path is as follows: **`$ALSDIR/lib/mgc/userware`**
☐ MGC_LOCATION_MAP	The MGC location MAP file.
☐ TYPE_REGISTRY	The file that contains the registry types for Design Manager. Directory path is as follows: **`$ALSDIR/lib/me/als.rgy`**
☐ MGC_WD	Optional working directory.

Table 1-2, “MGC Location Map File Variables,” shows the variables for the **MGC Location Map File**. For details, see “Creating an MGC Location Map File” on page 2.

Table 1-2. MGC Location Map File Variables

Variable	Description
$ALSDIR	The directory where you have installed the Designer Series software.
$MGC_GENLIB	The directory where you have installed the Mentor Graphics generic libraries.
$MYDESIGNS	The directory where your user-design sub-directories reside.
$ALS_TOOLBOX	The directory that contains the Actel toolbox components for Design Manager. Directory path is as follows: **$ALSDIR/lib/me/toolbox**

Configuring User's Accounts for the C-Shell

This section describes how to configure your accounts for the C-Shell.

You configure your accounts by setting various environment variables. You set these environment variables by editing either the “.cshrc” file, or the “.login” file (not both) to include the following:

```
setenv ALSDIR <alsdir>
setenv MGC_HOME <mentor_install_dir>
set path = ($ALSDIR/bin $MGC_HOME/bin $path)
setenv AMPLE_PATH $ALSDIR/lib/mgc/userware
setenv MGC_LOCATION_MAP <mgc_loc_map_file>
```

To access Design Manager icons, include:

```
setenv TYPE_REGISTRY $ALSDIR/lib/me/als.rgy
```

Designer Series Mentor Graphics Symbol Libraries

Actel provides symbol libraries specificially for Mentor Graphics. The Designer Series symbol libraries appear in the Design Architect library pull-down menu as Actel Libraries.

The Designer Series library components are located in the "$ALSDIR/lib/mgc/<act_fam>/parts" directory.

After selecting Actel Libraries, a family library menu can be selected.

When designing with Actel's software, you are required to use the Mentor Graphics Genlib library components. To do so, the gen_lib directory must be installed. This library includes bus rippers, portin and portout symbols, etc.

Design Manager Encapsulation Flow

Designer supports Mentor Graphics Design Manager. The Design Manager allows you to invoke the individual applications by selecting and clicking on appropriate icons.

Table 1-3, "Mentor Graphics Icons," shows the icons displayed with Design Manager:

Table 1-3. Mentor Graphics Icons

Icon	Description
 act_gen	Invokes ACTgen, which allows designers to create their own macros for use within Design Architect.
 act_map	Invokes ACTmap, which compiles VHDL and Palasm and optimizes designs as well as allowing translation between different netlist formats.
 act_edn2mgc	Converts edif to Mentor Graphics netlists for use in Design Architect, QuickSim II, and other Mentor Graphics applications. A symbol can be generated for the netlist using Design Architect's symbol generation.
 act_da	Invokes Design Architect.
 act_presimvpt	Creates a viewpoint for use in Quicksim II. This step is only required for functional simulation of designs that use the legacy library. Refer to "Mentor Graphics Library Organization" on page 3 for further information.
 act_mgc2edn	Creates an edif netlist from a Mentor design for use in Actel's Designer.

Table 1-3. Mentor Graphics Icons (Continued)

Icon	Description
	Creates an adl netlist from a Mentor design for use in Actel's Designer. (For Designer 3.0 and above, mgc2edn replaces this step.)
	Creates a VHDL file from DA design for use in QuickHDL or ModelSim.
	Invokes Designer, Actel's software to place and route your design for an Actel device.
	Creates QuickSim II and QuickPath compatible delay files for back annotation.

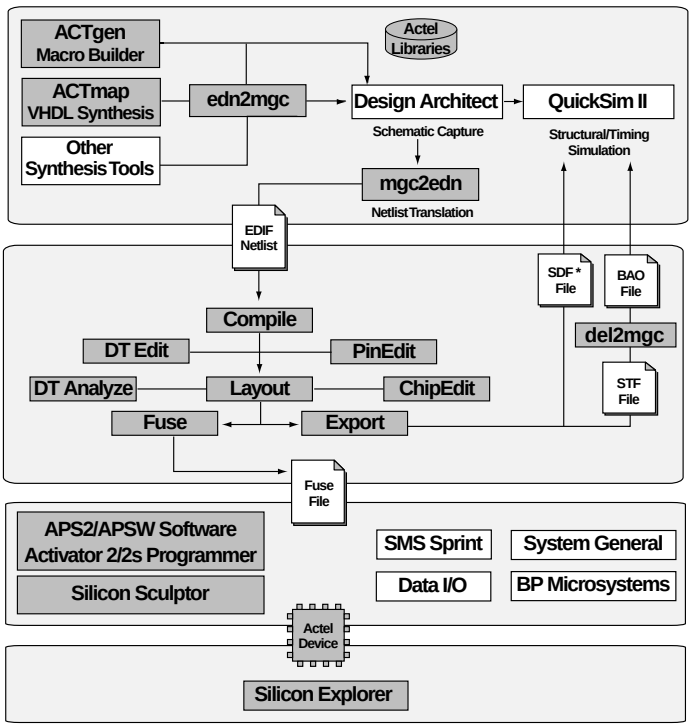
2

Actel-Mentor Graphics Design Flow

This chapter illustrates and describes the design flow for creating Actel designs using Mentor Graphics Design Architect schematic capture tool, QuickSim II simulator, and Actel Designer.

Schematic-Based Design Flow Illustrated

Figure 2-1 shows the schematic-based design flow for an Actel FPGA using Designer software and Mentor Graphics software.[1]



* sdf flow available only in Mentor Graphics sofware versions B.1 or later.

Figure 2-1. Schematic-Based Design Flow

1. Actel-specific utilities/tools are denoted by the grey boxes in Figure 2-1.

Schematic-Based Design Flow Overview

The following describes the design flow for creating a design using the Design Architect Schematic capture program, QuickSim II simulator, and Actel Designer Series software. For instructions on how to use the Designer Series software and its tools, refer to the *Designing with Actel* manual.

Design Creation/ Verification

Design Creation/Verification consists of Schematic Capture, Functional Simulation, and EDIF netlist generation.

Schematic Capture

Enter your design in Design Architect. Use one of the Actel family symbol libraries. Save the design. Refer to Mentor Graphics documentation for more information.

EDIF Netlist

After you create the schematic, use mgc2edn to create an EDIF ".edn" netlist. Refer to "Creating an EDIF Netlist" on page 24 for more information.

Functional Simulation

Use QuickSim II to perform a functional simulation of your design. Refer to Mentor Graphics documentation for more information.

Note: The functional simulation sets all delays to one nanosecond.

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, static timing analysis may be performed in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with QuickSim II.

Place and Route

Use Designer to place and route your design. Refer to the *Designing With Actel* manual for information about using Designer.

Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis on your design. Refer to the *Designing With Actel* manual for information about using DT Analyze.

You can also perform static timing analysis using Mentor Graphics QuickPath. Refer "Static Timing Analysis Using QuickPath" on page 35 for more information.

Timing Simulation

You perform a timing simulation on your design using QuickSim II after placing and routing it. Timing simulation verifies that the design meets your timing requirements. Timing simulation requires information extracted and back annotated from Designer. Refer to "Timing Simulation with BAO Back annotation" on page 27 and to "Timing Simulation with SDF Back annotation" on page 28 for detailed information.

Programming

You program a device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designing With Actel* manual and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information on programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Action Probe or Silicon Explorer. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information on using Action Probe or Silicon Explorer.

3

Actel-Design Architect Design Considerations

This chapter describes various conventions that should be observed when creating a design for Actel devices using Mentor Graphics Design Architect. Included in this chapter are details about schematic naming conventions, designing using multiple page designs, adding input and output macros to your desgin, adding ACTgen macros, adding ACTmap blocks, and adding Synopsys blocks. Also included is information about creating an EDIF netlist and importing an EDIF netlist into Mentor Graphics.

Schematic Naming Conventions

A new set of Actel properties can be added to schematics in Mentor Graphics' Design Architect. Once a property is attached to a net or an instance, the property name and value will propagate to the proper location in the Actel design files.

When creating a schematic for Actel devices, there are some conventions you must observe as described in the following sections:

Specifying Properties in Design Architect

Properties can be assigned on the desired object directly in the schematic. After saving the design, the "netlist" command (mgc2edn) reads the schematic and attaches the property name and value to the corresponding net in the .edn file.

Follow the procedure below to add a net property in the schematic:

1. **Open the schematic in Design Architect.**
2. **Select one end of the NET.**
3. **Choose the "Add" command from the "Properties" menu.** A new menu will appear.

4. **For the "property name" type the property name.** For example:

   ```
   alspin
   ```

5. **For the "property value" enter the property value.** Refer to Table 3-1 for description of the available Properties.
6. **Select "Ok" and attach the property to the Net.**

Naming Conventions

Use only alphanumeric and underscore "_" characters for schematic net and instance names.

Note: Do *not* use asterisks, forward and backward slashes, or spaces.

Top-Level Symbol

You may create a top-level symbol for the entire design. The pin names on the symbol must match the underlying dangling net names on the top level schematic or the symbols "portin/portout" names on the I/O pads. Remember to update the symbol if the pins on the schematic change. If a top level symbol is not created then portin/portout from Genlib must be used on all of the I/O pins.

Note: The top level symbol must only contain pins for I/O buffers. Do not add power, ground, pra, or prb pins, etc. to the symbol. Doing so will cause errors during netlisting.

Preserve

One of the Combiner's function is to combine (optimize) combinatorial functions into sequential macros for Actel devices families. Combining logic does not affect the function of the circuit. To prevent such combining, an ALSPRESERVE property may be added to the net connecting the macros that would otherwise be combined. The ALSPRESERVE property information is copied into the <design_name>.edn, see Table 3-1.

Table 3-1. Properties

Property Name	Property Value	Attached to
ALSPIN	package pin number	NET (net connecting a port with an I/O buffer)
ALSPRESERVE	(none)	NET (any net)

Multiple Sheet Design

For a multiple-page design, each sheet is treated as a part of a schematic and is not considered as a level of hierarchy. Use “offpag.in” and “offpag.out” connectors to connect sheets.

Adding Input and Output Macros

This section describes adding input and output macros.

Adding I/O Pins to the Schematic

The procedure for adding I/O buffers is to place the buffer on the schematic sheet and add a net to the pad side of the buffer as shown in Figure 3-1. Then, either an MGC Genlib component, portin or portout, may be attached to the net and labeled, or the existing net may be labeled. It is recommended to place all Input and Output buffers on the top level sheet of the design. If the Input and Output buffers are buried within the design, a net for every I/O signal has to be pulled to the top level sheet and should be connected to the corresponding port. If portin and portout are not used, a top level symbol that contains a pin for every I/O buffer must be created.

The labels attached to the net or portin or portout will appear as pin names in Pin Edit.

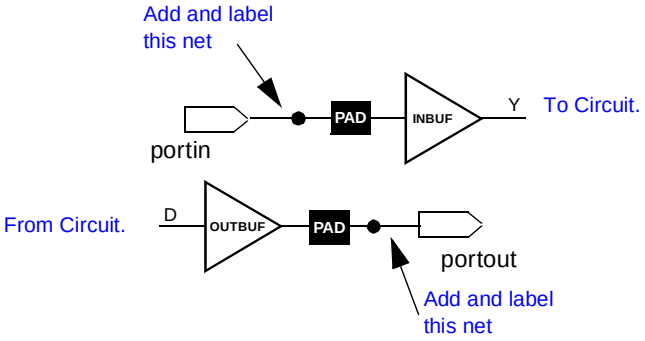


Figure 3-1. I/O Pins in a Mentor Graphics Design

Assigning I/O Pins to the Schematic

One way of assigning I/O pins is to use Pin Edit within Designer. Another way is to assign a property (a pin property called ALSPIN with the corresponding package pin number) to the net connecting a port to an I/O buffer, as shown in Figure 3-2.

The labels attached to the net or portin or portout will appear as pin names in Pin Edit.

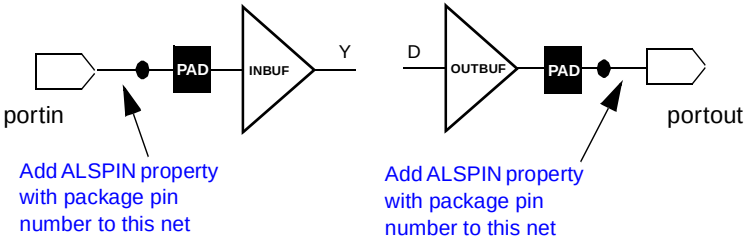


Figure 3-2. Adding I/O Pins to a Mentor Graphics Design

Note: PinEdit does not change the Mentor Graphics netlist or schematic information. Pin locations modified with PinEdit are not backannotated to the schematic.

Adding ACTgen Macros

With the ACTgen Macro Builder you can create macros using a simple description. The ACTgen Macro Builder can produce counters, adders, decoders, RAM, and FIFO, in a very short time. In addition, you can easily integrate ACTgen based blocks, with schematics and symbols into a Mentor Graphic's Design Architect design.

ACTgen Macro Generation

To integrate a macro generated using ACTgen with schematic capture using Design Architect, instantiate the generated symbol into your design.

Generating an ACTgen Macro

Refer to the *Designing with Actel* manual for information regarding using the ACTgen software. Be sure to specify MGC as the CAE type.

Instantiating the Macro

Perform the following steps to instantiate a macro generated by ACTgen.

1. **In Design Architect, choose the "Symbol By Path" command from the "Instance" pop-up menu.** Use the navigator to instantiate the symbol. The symbol is instantiated from its directory and should appear on the schematic sheet. Place it on the sheet by clicking the left mouse button.
2. **Complete the <design_name> by adding the rest of the schematic components, including I/O buffers, CLKBUF (if a clock signal is present) from the Actel Library, and Portins and Portouts from Mentor Graphics Genlib library.** Check and save the <design_name> design.

   Note: ACTgen expects the macro to be generated within your design directory. For example, if your design is called design_name, ACTgen expects to create the macro under the design_name directory. After creation, ACTgen will create the file design_name/<macro_name>.gen.
3. **Exit Design Architect.**

Adding ACTmap Blocks

ACTmap reads VHDL netlists and compiles files into EDDM databases using “edn2mgc.” These files can be used by Design Architect.

VHDL Integration with Schematics

To integrate a VHDL design from ACTmap into Design Architect, perform the following steps.

1. **Generate an EDIF netlist file by compiling VHDL source into an EDIF netlist.** Refer to the *Designing With Actel* manual for more information.
2. **Run edn2mgc.** Type the following command:

   ```
   edn2mgc fam:<act_fam> [ednin:<edif_file>] <block_name>
   ```

Instantiating the ACTmap Block

The following procedure shows how to integrate an ACTmap block with Mentor Graphics schematics:

1. **Invoke Design Architect.** Type the following command:

   ```
   da
   ```

2. **Open an existing or create a new design.** From the Palette, click the “Open Schematic” icon.
3. **Name the block that is to contain the ACTmap block.** In the “Component Name” field, type:

   ```
   $MYDESIGNS/<design_name>
   ```

   Where “$MYDESIGNS” is a soft prefix defined in the Mentor Graphic’s location map file, and “<design_name>” is the design. The design will include the symbol that represents the ACTmap block. For example, “black_box.” Click the OK command button.

4. **Create a new symbol:**
   - Iconize the schematic sheet.
   - From the Palette, click on the “Open Symbol” icon.
   - Next, click on the “Navigator” icon. This displays the Navigator Window.
   - In the Navigator Window select black_box and then hit the down arrow to go under and select the black_box component represented with a “c” character.
   - Click on OK. The symbol automatically generates from the “black_box” component.
5. **Add Properties to the new symbol.** Select the ACTmap symbol, then choose the “Add Single Property” command from the “Properties-Add” pop-up menu.
   - From the existing Property Name table, select COMP.
   - In the Property Value field type the symbol name, i.e. black_box. Click on OK.
   - Place the property on or near the black_box symbol.
6. **Unselect the symbol.**
7. **Check the component.** Choose the “With Defaults” command from the “Check” pull-down menu. The Transcript window reports 0 errors and n warnings. The warnings are due to properties that are not registered yet to the interface.
8. **Save the symbol.** Choose the “Default Registration” command from the “File-Save Symbol” pull-down menu.

   Note: The following message may appear:

   ```
   “Symbol doesn't match interface. Should the interface be updated?”
   ```

   Click on YES. The black_box symbol is now registered. Check the symbol sheet again and the warnings should disappear. The symbol sheet can be closed now.

9. **Instantiate the macro.** De-iconize the <design_name> schematic sheet by double clicking on the icon. From the Pop Up menu, select Instance > Symbol By Path and use the navigator to instantiate the black_box symbol. The black_box symbol is instantiated from the black_box directory and should appear on the schematic sheet. Place it on the sheet by clicking the left mouse button.

   You can now complete the <design_name> by adding the rest of the schematic components, including I/O buffers, CLKBUF (if a clock signal is present) from the Actel Library, and Portins and Portouts from Mentor Graphics GENLIB library. Check and save the <design_name> design.

10. **Exit Design Architect.**

Adding Synopsys Blocks

One technique in the EDA environment is integrating Synopsys with Mentor Graphics. The Synopsys Integrator for Falcon Framework is a tool that allows you to build a design in HDL, optimize the design with Synopsys, and convert the design from a Synopsys database to a Mentor Graphics database for simulation.

Synopsys Integrator interacts with the Mentor Graphics database. When the tool is loaded and all variables are set, you can perform the database translation with the Mentor Graphics Design Manager.

In this section, we discuss how to:

- Set the Synopsys Integrator environment variables.
- Start the Design Manager to display the Synopsys tools.
- Generate a Synopsys/Mentor Graphics compatible symbol library.
- Transfer a design from the Synopsys database to the Mentor Graphics database.

Environment Setup

Before starting the integration, you must verify that the search path is set to access the Falcon Framework software. Furthermore, you must define the following three environmental variables to run the Synopsys Integrator software from the Mentor Graphics environment:

```
$SYNOPSYS_IFF_ROOT
$TYPE_REGISTRY
```

You must set the "$SYNOPSYS_IFF_ROOT" variable in the location map file and in your ".kshrc," ".profile," or ".cshrc" start-up files. The "$SYNOPSYS_IFF_ROOT" variable must be set to the directory where the Synopsys Integrator is installed. For example, set the "$SYNOPSYS_IFF_ROOT" variable to:

```
$SYNOPSYS/platform/syn/interfaces/mentorA
```

In our example, "$SYNOPSYS" is the directory where the Synopsys software is installed, and "platform" can be either the "hp700" or "sparc" directory, depending on your workstation.

You must set the "$TYPE_REGISTRY" in the location map file and your ".kshrc," ".profile," or ".cshrc" start-up files. This variable must be equal to the following directory:

```
$SYNOPSYS_IFF_ROOT/registry/synopsys.rgy
```

Design Manager Setup

1. **Invoke Design Manager, type:**

   ```
   dmgr
   ```

2. **Create the Synopsys icons:**

   - In the Tools window, click the right mouse button to display the Tool Operation pop-up menu.
   - From the Tool Operation pop-up menu, select View Toolboxes to display the Toolboxes window.
   - From the Toolboxes pop-up menu, select Add Toolbox to display the ADD TO prompt bar.
   - In the ADD TO prompt bar, type "$SYNOPSYS_IFF_ROOT/toolbox," and press Return or click OK.

- From the Toolboxes pop-up menu, select Save. This adds the Synopsys toolbox path to the Mentor Graphics start-up file located in the "user_directory/mgc/startup/dmgr_toolbox_path.startup" file.
- From the Toolboxes pop-up menu, select View Tools. The Tools window should have the Synopsys tools displayed at the bottom of the window.
- From the "Setup" menu, choose the "Icon Layout" command. This rearranges the icon location in the Tools window.
- Close and exit the Mentor Graphic Design Manager.

DB2EDDM Database Translation

To transfer a design from the Synopsys database to the Mentor Graphics database, use the following procedure:

1. **Create a Mentor-compatible schematic.**
   - Set the symbol_library variable in the ".synopsys_dc.setup" file to the "*fam*_mntr.sdb" library. If the symbol library is set to the Actel-Synopsys symbol library, the symbols in Mentor will be offset.
   - Read in a VHDL design or "design.db" file in Synopsys.
   - Execute the "mgc_name.scr" script file found in the "<synopsys_syn_lib_loc>/scripts/<act_fam>" library directory.
   - Save design as "design.db." If you do not wish to override your old "design.db" file, save the design with a different name.
2. **Invoke Design Manager, type:**

   ```
   dmgr
   ```

3. **From the Tools window, double click on the "db2eddm" icon.** This opens the Synopsys DB to EDDM window (Figure 3-3).

4. **In the Synopsys DB to EDDM window, type the following:**
   - In the DB File field, type the "<design>.db" design name.
   - In the Add Search Path field, type the hard path to the location of the "<design>.db" file.
   - In the Map File field, type the hard path and the map file name "<act_fam>.map." The output directory is set by default to the location of the "design.db" file.
5. **Click OK.** This launches the "db2eddm" program**.**

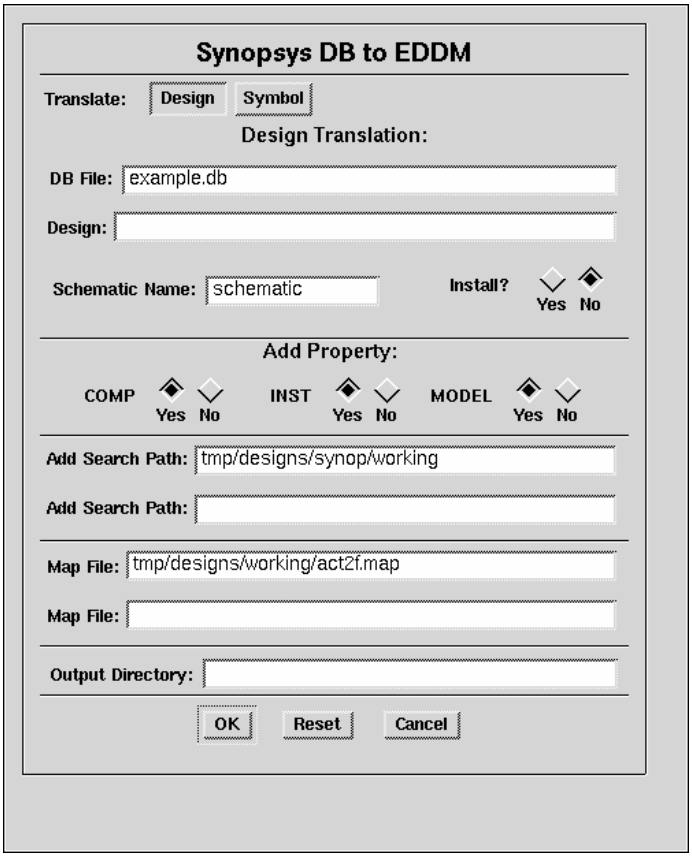


Figure 3-3. Synopsys DB to EDDM Window

Note: The following screen messages could be displayed:

```
Warning: Can't locate file `actsym.sdb' (DB-3)
```

```
Error: can't find symbol for instance xxx of design
```

If the preceding messages appear, set the “symbol_library” variable in the “.synopsys_dc.setup” file to the “<act_fam>_mntr.sdb” file location.

6. **Review your design results.** Invoke Design Architect and read in the schematic sheet.

Creating an EDIF Netlist

After entering the schematics and functionally simulating the design, create the EDIF netlist file, <design_name>.edn, which will be imported into Designer. The Actel command that generates EDIF netlist is “mgc2edn.” Invoke the “mgc2edn” command from Design Manager or from the project directory, type:

```
mgc2edn fam:<act_fam> <design_name>
```

Importing an EDIF Netlist

You can import an EDIF netlist generated by other CAE tools into the Mentor Graphics design database EDDM for simulation with QuickSim II and/or timing analysis with QuickPath.

To import a netlist into Mentor Graphics

1. **Invoke the “edn2mgc” command from the Design Manager window, or from the project directory, type:**

   ```
   edn2mgc fam:<act_fam> <design_name>
   ```

Note: The edn2mgc utility only reads EDIF netlists with supported flavors. To work around the unsupported EDIF, run edn2adl, and then run adl2edn to obtain an EDIF netlist with Actel Flavor. Then run end2mgc.

If you are running edn2mgc on the EDIF netlist created with Designer 3.1.1 or earlier, you may observe the following error message:

```
Error: Could not find external part.
```

If you get this error message, it is because these missing macros are not supported in the standard library. Call Actel Customer Applications Center to request the migration library. Refer to "Product Support" on page 37 for information about contacting Actel Customer Applications Center.

4

Simulation Using QuickSim II

This section describes steps to perform functional simulation (behavioral and structural), timing simulation, and board-level simulation for Actel devices using the Mentor Graphics QuickSim II simulator.

Functional Simulation

To simulate your design with unit delays, run Quicksim II by typing the following:

```
quicksim <design_name>
```

Note: If your design uses the legacy library (as described in "Mentor Graphics Library Organization" on page 3) you need to run the following command pior to running your first functional simulation:

```
presimvpt fam:<act_fam> <design_name>
```

If your design does not use the legacy library, presimvpt need not be run.

Timing Simulation with BAO Back annotation

After running "mgc2edn" on the top level design, run the Designer software to Layout the design and extract the back annotation delays. Exit the Actel software and from the command line, run "del2mgc" to generate the "<design_name>.bao" file. Type:

```
del2mgc <design_name>
```

To start the simulation, run Quicksim II. Type:

```
quicksim <design_name> -tim max
```

Timing Simulation with SDF Back annotation

To simulate with SDF back annotation, extract the SDF file from Designer, and perform the following steps:

1. **Type the following:**

   ```
   quicksim <design_name> -tim max
   ```

2. **In the QuickSim II window, choose Load SDF from the File menu, then specify the SDF file name for back annotation.**

   Note: Back annotation with SDF is only supported with Mentor Graphics software versions B.1 or later.

Board-Level Simulation

System designs are typically divided into functional modules that are implemented by several Actel devices. To check the functionality of the system, it is very important to simulate all of the Actel devices together. The Actel Designer Series system includes board-level, multichip simulation capability using Mentor Graphics software for Actel devices.

The software requirements are identical for chip level and board level simulations. The requirements are Mentor Graphics' Design Architect (DA), Design Viewpoint Editor (DVE), Quicksim II, and Actel's Designer Series Development System.

Board-Level Design Example

This section assumes that you know how to use Design Architect to create symbols and sheets for your chip-level designs. Consider the board level design, "board," which contains the chip level components *chip1, chip2* and *chip3*. Each component is composed of a symbol and a schematic.

In this example, the *board* schematic includes *chip1, chip2* and *chip3* symbols, which are ACT 1, ACT 2 and ACT 3 family designs respectively. The "board" design is shown in Figure 4-1.

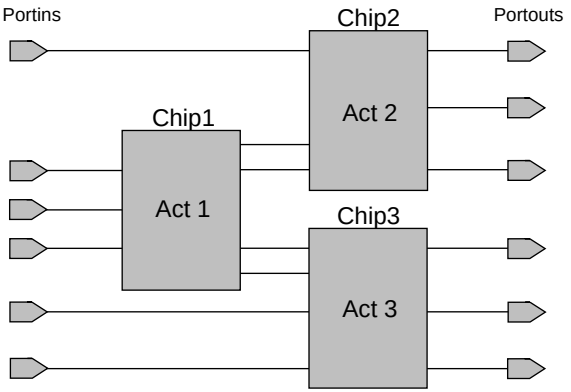


Figure 4-1. Board Schematic Sheet

1. **Create a netlist for *chip1*.** Run mgc2edn on the design to generate the Actel netlist by typing the following command:

   ```
   mgc2edn fam:<act_fam> chip1
   ```

2. **Create the Backannotation file for *chip1*.**

   - Use Designer to layout and extract post-layout delays for the device.
   - Backannotate these delays to Quicksim II by typing the following command:

     ```
     del2mgc chip1
     ```

   This step creates the back annotation file, "chip1.bao."

Note: Before you continue, repeat steps 1 through 3 for all chips in your design.

3. **In Design Architect, create the schematic sheet "board."** From the "Instance" pop-up menu, select the "Choose Symbol" command:
   - Use the Navigator to select and place *chip1* on the schematic sheet. Repeat this procedure for all chips in your design.
   - Connect the symbols and add Portins and Portouts to the schematic.
   - Execute the "Check Sheet" command and save the changes.
   - Open a new symbol sheet and create the board symbol.
   - Execute the "Check Sheet" command and save the changes.

DVE Configuration

Next, configure the Design Viewpoint Editor to setup the design with backannotated post-layout delays, using the following procedure:

1. **From the board directory, invoke DVE for the design as follows:**

   ```
   dve <viewpoint_file_name>
   ```

   If <*viewpoint file name*> is not specified, DVE uses the default viewpoint file, *default*.

2. **Open your board-level schematic.** Choose the "Open Sheet" icon from the palette. The board-level shematic sheet is displayed, as shown in Figure 4-2.

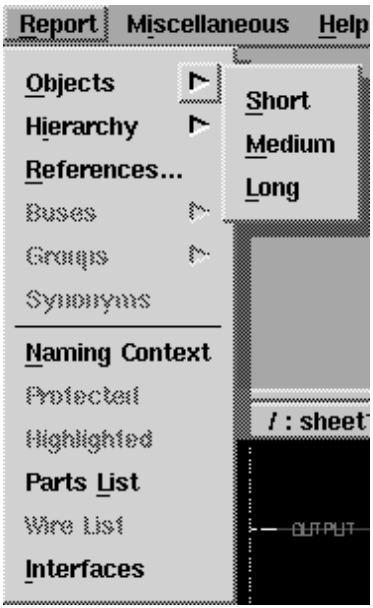


Figure 4-2. Board Level Schematic Sheet

3. **Display the path context.** Select the chip1, chip2, and chip3 symbols and choose the "Long" command from the Reports Objects submenu. An Object window opens and lists the path contexts for the symbols, including references and property information.

   Note: Verify that the path contexts are of the form: /I$1, /I$2, and /I$3 in the Objects window.

4. **Close the Objects window.**

5. **Make the Design Configuration window active by clicking on its title bar, as shown in Figure 4-3.**

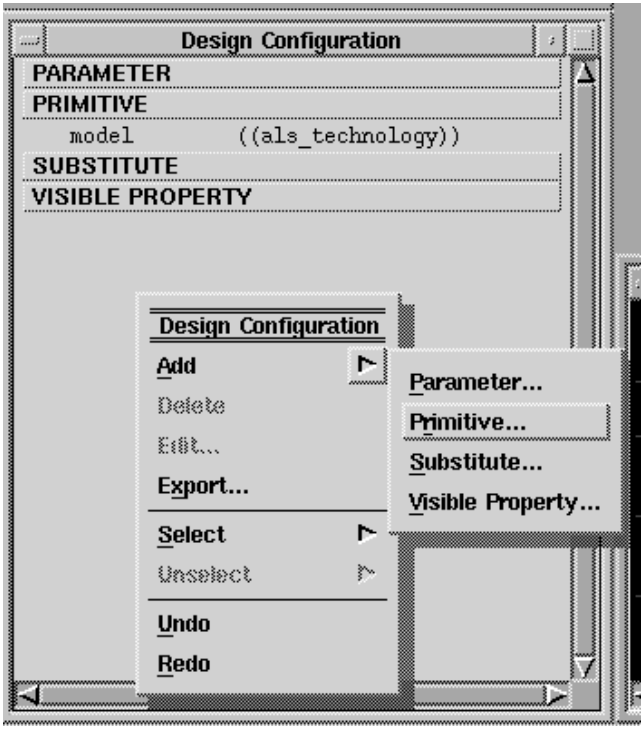


Figure 4-3. Design Configuration Window

6. **Set Primitive.** Open an Add Primitive window. Enter the "model" primitive name in the Add Primitive window's Name field. Set the Value to the following:

   <act_fam>

   Set the Primitive Type to String.

7. **Open an Import Back Annotation window.** Select "Back Annotation" from the File menu. From the pull-down menu click on Import, as shown in Figure 4-4.

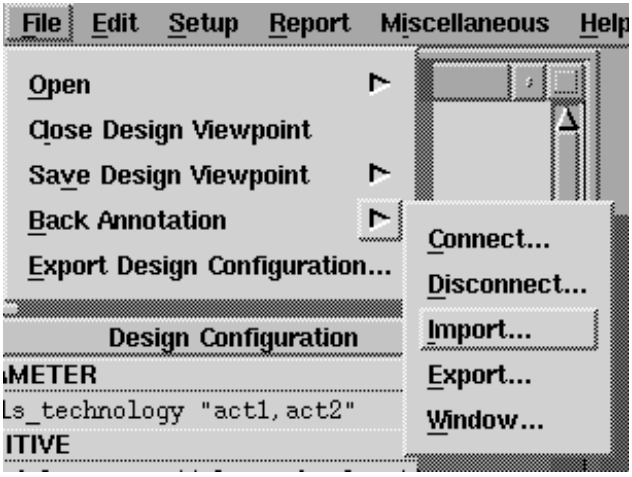


Figure 4-4. File Pull-Down Menu

In the ASCII BA field, shown in Figure 4-5, enter the path to the *chip1.bao* file. Leave the BA Name field set to the default viewpoint. In the Import Context field, add the path context of *chip1*. Repeat this step for all chips in your design. Click on the OK button to import the delays to DVE.

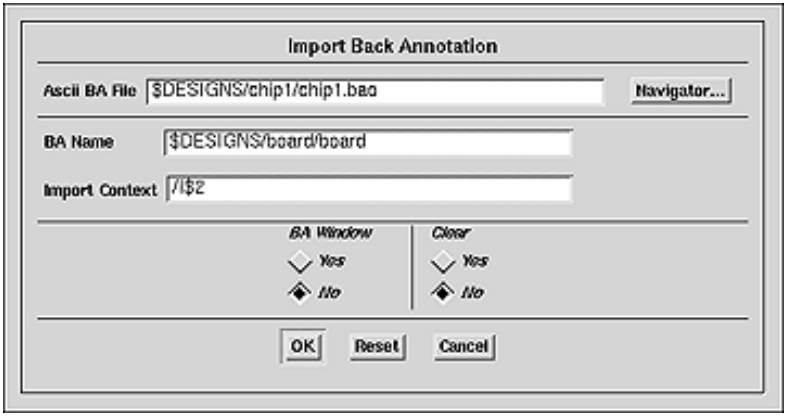


Figure 4-5. Import Back Annotation Window

8. **Save the viewpoint information.** Select "Save Design Viewpoint" from the file menu. Exit DVE.

   The board-level design is ready for simulation with post-layout, backannotated delays from Designer.

9. **Invoke Quicksim II with back annotated delays by entering the following command:**

   ```
   quicksim <board> -tim max <viewpoint file name>
   ```

For board level simulation with designs created with Designer 3.1.1 or earlier, call Actel Customer Applications Center for more information. Refer to "Product Support" on page 37 for information about contacting Actel Customer Applications Center.

5

Static Timing Analysis Using QuickPath

This chapter describes how to perform static timing analysis using QuickPath. Refer to the Mentor Graphics QuickPath documentation for more information about QuickPath.

Timing Analysis

After running "mgc2edn" on the top level design, run the Designer software to layout the design and extract the backannotation delays as follows:

1. **Back annotate your delays.** At the command line, type:

   ```
   del2mgc <design_name>
   ```

   This generates "<design_name>.bao" file.

2. **Run QuickPath.** Type:

   ```
   quickpath <design_name> -tim max
   ```

Timing Analysis with SDF

After the .sdf file is extracted from Designer, you can perform timing analysis as follows:

1. **Invoke QuickPath by typing:**

   ```
   quickpath <design_name>
   ```

2. **Choose the "Load.SDF" command from the File menu and select the .sdf file for backannotation.**

A

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