Designer Series Development System R3-1998 Release Notes

This document describes the new features and enhancements of the Designer Series Development System R3-1998 release. It also contains information about discontinued features and known limitations.

For information about which versions of Cadence, Mentor Graphics, Motive, Synopsys, and Viewlogic tools, and which versions of VHDL and Verilog simulators are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com) and type "third party" (without quotes) in the Keyword box.

New Features and Enhancements

This section lists the new features and enhancements of the R3-1998 release.

Devices and Packages

The R3-1998 release supports the following new devices and packages:

54SX

A -3 speed grade has been added to all devices.

54SX16P - A new PCI compliant device, it is available in 100 VQFP, 144 TQFP, 176 TQFP, 208 PQFP, 272 BGA, and 329 BGA packages.

54SX08 - A new device, it is available in 100 VQFP, 144 TQFP, 176 TQFP, and 208 PQFP packages.

54SX16 - A 208 CQFP package has been added.

54SX32 - 144 TQFP, 176 TQFP, 208 CQFP, 256 CQFP, 272 BGA, and 329 BGA packages have been added.

42MX

42MX36 - 208 CQFP, 240 PQFP, and 256 CQFP packages have been added.

RadTolerant

The new RadTolerant (RT) family is supported in the following devices and packages:

RT1425A - A new device, it is available in a 132 CQFP package.

RT54SX16 - A new device, it is available in 208 CQFP and 256 CQFP packages.

RT54SX32 - A new device, it is available in 208 CQFP and 256 CQFP packages.

RTproto-SX16 - A new device, it is available in 208 PQFP, 208 CQFP, and 256 CQFP packages.

RTproto-SX32 - A new device, it is available in 208 PQFP, 208 CQFP, and 256 CQFP packages.

Designing with RT54SX Devices

Due to the addition of a JTAG reset pin to the RT54SX16 and RT54SX32 devices, these devices have different pinouts than comparable prototype commercial devices. The R3-1998 release provides a simple method to prototype these RT devices. The RTproto-SX16 and RTproto-SX32 devices have been added so designers can perform timing analysis and program prototype devices using commercial A54SX devices. 208 PQFP packages have also been included for the RTproto devices to allow designers to use commercial 208 PQFP devices for prototyping. The following procedure describes the design flow.

1. **Select the appropriate RT54SX device and package type in the Device Selection window in Designer.**
2. **Compile and Layout the design.**
3. **Check the functionality of the design by checking the timing and performing post-layout simulation.**
4. **Select the Device Setup Wizard command from the Options menu.** Select the appropriate RTproto device and package.
5. **Check the functionality of the design by checking the timing and performing post-layout simulation.** Since the RT54SX and RTproto-SX devices are pin-for-pin compatible there is no need to perform Compile or Layout again.

6. **Generate an RTproto device programming file (.afm) from Designer and program a commercial A54SX device.**
7. **Verify that the commercial A54SX device functions correctly.** All timing should have been verified using both the RT54SX and RTproto timing.
8. **Select the Device Setup Wizard command from the Options menu.** Select the appropriate RT54SX device and package.
9. **Generate an RT54SX device programming file (.afm) from Designer and program an RT54SX device.**

Refer to the Actel *RadHard/RadTolerant Programming Guide* on the Actel Web site for additional information about programming RadTolerant devices.

Designer

- A new file type, Probe (.prb), can be exported from Designer for use with the Analyze software and the Silicon Explorer diagnostic tool.
- The standard programming voltages have been modified for all MX devices, improving programming yield and programming times. To take advantage of these improvements, you should re-layout your design with R3-1998, making sure that Incremental Placement is set to Fixed, then regenerate your AFM file.

ACTmap

ACTmap has improved counter, comparator, and accumulator inferring in VHDL synthesis.

ACTgen

- Wide Decode, XOR tree, Adder, and Subtracter macros for the 54SX family have been improved by using Fast Connects.
- Three buttons, Open, Generate, and Report, have been added to the ACTgen toolbar.

Silicon Expert

Silicon Expert, a new tool developed to help users optimize their design for the Actel architecture, is being evaluated in R3-1998. Features include the I/O Buffer Manager, which allows designers to add, remove, or replace I/Os with the click of a mouse button. This frees designers using a synthesis flow from having to instantiate special I/Os such as CLKBUF and QCLKBUF.

Also included is the Buffer Manager. Synthesis tools generate buffer trees for many hierarchical designs. In the Actel architecture, a buffer can consume an entire logic module. The Buffer Manager can perform buffer tree balancing, correction, and replacement, and can utilize global resources such as CLKINT or QCLKINT to improve area utilization and speed of a design.

Other features include timing report generation and netlist translation. Designers can also use Silicon Expert to perform preliminary timing and fanout analysis on either a single block or an entire design.

To launch Silicon Expert:

PC

Choose Silicon Expert from the Designer group in the Programs menu under the Start menu.

UNIX

Type the following command at the prompt:

```
expert
```

Programming and Debugging

- APSW currently supports programming the 54SX device family. However, AFM files generated in non-production versions of Designer *must* be regenerated. To regenerate the AFM file, re-layout your design with R3-1998, making sure that Incremental Placement is set to Fixed, then regenerate the AFM file. Call the Actel Customer Applications Center at 1-800-262-1060 before programming for the latest patch information.
- The standard programming voltages have been modified for all MX devices, improving programming yield and programming times. To take advantage of these improvements, you should re-layout your design with R3-1998, making sure that Incremental Placement is set to Fixed, then regenerate your AFM file.

Silicon Sculptor

- The Silicon Sculptor software version 2.00 is now available from the Designer install CD (Windows 95 only). To install the software, copy the “act_soft.exe” file from the “Sculptor” directory on the CD to your hard drive, then double click “act_soft.exe.” To run the software, double click the “Sculpt.exe” file on your hard drive.
- Silicon Sculptor now supports the 54SX family.

Silicon Explorer

- The Silicon Explorer software version 3.0 is now available from the Designer install CD (Windows 95/NT only). To install the software, double click "setup.exe" in the "Silicon Explorer 3.0" directory.
- The Analyze software, used with the Silicon Explorer diagnostic tool, now runs independently from APSW. The Analyze software now uses a Probe (.prb) file from Designer. To export a .prb file from Designer, select the Export command from the file menu, then choose Auxiliary File as the File Type and Probe as the Type.
- Silicon Explorer now supports the 54SX family.
- Silicon Explorer now reads the device checksum.

Cadence

None.

Mentor Graphics

None.

MOTIVE

None.

Synopsys

- A new library, "act_rt.db," has been added to provide accurate timing for RadTolerant (RT) devices in the 54SX family. The "act.db" library should be used for all 54SX standard and PCI applications.
- Latches can now be implemented in all device families using the triple voting technique for radiation resistant designs. Previously, only flip-flops could be implemented.

Viewlogic

Versions of Workview Office that include FPGA Express are supported.

Verilog

None.

VHDL

None.

Macros

- Two new clock buffers, CLKBUFI and CLKINTI have been added to the 54SX library. These macros are identical to CLKBUF and CLKINT respectively, except they are inverting buffers. All CAE libraries support these macros.
- Eight new CMxx macros, CMA9, CMAF, CMB3, CMEA, CMF1, CMF2, CMF4, and CMF8, have been added to the 54SX library. Each is equivalent to a CM8 with one or more pins driven by a single inverted pin. All CAE libraries support these macros. Refer to the addendum to the Actel *Macro Library Guide*, available in the "/doc" directory of the install CD and your system when the Designer Series software is installed.

Documentation

- An Actel *Macro Library Guide Addenda and Errata*, which contains macro information about the macros added to the 54SX library and corrections to existing macro information, is available in the "/doc" directory of the install CD and your system when the Designer Series software is installed.
- The *Viewlogic Workview Office Interface Guide* has been updated to describe using Workview Office 7.5 and FPGA Express.

Discontinued Support

This section lists features that were supported in previous versions of the Designer Series software but are not supported in R3-1998 release.

Devices and Packages

- Support for the 42MX36 240 RQFP package has been removed.
- Support for the 54SX16 84 PLCC package has been removed.

No other features have been discontinued in the R3-1998 release.

Known Limitations

This section lists the known limitations for the R3-1998 release. For the latest information on known limitations, check the GURU on-line technical support system on the Actel Web site (http://www.actel.com).

Devices and Packages

None.

Designer

- All 54SX designs created in non-production versions of Designer must be re-compiled. Layout can be done in incremental mode to preserve placement information. Programming files also *must* be regenerated.
- Designer does not support translation to Data I/O programming format (DIO) for the 54SX device family.
- DT Layout does not support the 54SX device family.
- Clock skew is not taken into account by DT Analyze and the timing report during "shortest" calculations.
- I/O Arrival Times are not used by DT Layout.
- Only primary ports appear in the external setup and hold section of the timing report. Certain signals driven by clock buffers may not be shown.

ACTmap

- ACTmap only supports tri-state buffers on top level ports. Internal tri-state busses are not supported. All internal tri-states must be mapped to multiplexors. Refer to "Internal Tri-State to Multiplexor Mapping" in the *Actel HDL Coding Style Guide* for information.
- ACTmap cannot read filenames or directory names that have a space in the name.
- ACTmap does not support multi-dimensional arrays. Although ACTmap can compile and synthesize a VHDL design with multi-dimensional arrays, the netlist that is generated from ACTmap will be incorrect.

ACTgen

None.

Silicon Expert

- Silicon Expert does not run on HP-UX and SunOS 4.x.
- You must set the following environment variable in your UNIX shell script for Silicon Expert to run properly. The following is a C shell variable. If you are using another shell, adjust the syntax accordingly:

```
setenv WINDU $ALSDIR/windu.ini
```

- CLKINT and QCLKINT global networks are not displayed in the Network Manager.
- New 54SX CLKBUFI and CLKINTI macros are not supported.
- Silicon Expert does not insert IOCLKBUF or IOPCLBUF macros.

Silicon Explorer

- To read the checksum of an ACT 1 or A40MX devices, you must connect the SDO connector from the Probe Pilot to the PRA pin of the FPGA.

Programming and Debugging

- The 54SX family does not support silicon signatures. If a silicon signature is used, a checksum error will result during programming.
- The Debugger tool in APSW does not support the 54SX device family.
- Designer does not support translation to Data I/O programming format (DIO) for the 54SX device family.
- APSW does not run on HP-UX 10.2. Call the Actel Customer Applications Center at 1-800-262-1060 for alternative programming options.
- When using Blankcheck in APSW on programmed 54SX devices, APSW may report them as blank even though they have been programmed. However, if the correct checksum is reported for the device it has been programmed correctly. This erroneous blank message is caused by bus speed issues between some systems (PC and UNIX) and the Activators.

Cadence

Actel only supports the Concept-SCALD flow when using version PE 13.0.

Mentor Graphics

None.

MOTIVE

None.

Synopsys

None.

Viewlogic

Intelliflow or mixed schematic/HDL designs are not supported. Support is available from Viewlogic for direct Viewlogic customers.

Verilog

None.

VHDL

None.

Macros

None.

Documentation

- The June 1998 version of the Actel *Macro Library Guide* does not contain information about the macros added to the 54SX library. However, a *Macro Library Guide Addenda and Errata* is available in the "/doc" directory of the install CD and your system when the Designer Series software is installed.