VHDL VITAL™

Simulation Guide

Actel

Windows® & UNIX® Environments

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Part Number: 5579006-1

Release: July, 1998

Trademarks

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Introduction

This *VHDL Vital Simulation Guide* contains information about using the Model Technology V-System or Model Sim, Mentor Graphics QuickHDL, Cadence Leapfrog, Viewlogic SpeedWave, and Synopsys VSS to simulate designs for Actel devices. Refer to the *Designing with Actel* manual for additional information about using the Designer software. Refer to the documentation included with your simulator for information about performing simulation.

Document Organization

The *VHDL Vital Simulation Guide* is divided into the following sections:

Chapter 1 - Setup contains information and procedures about setting up Model Technology's V-System or Model Sim simulator, the Mentor Graphics QuickHDL simulator, the Cadence Leapfrog simulator, the Viewlogic SpeedWave simulator, and the Synopsys VSS simulator.

Chapter 2 - Design Flow illustrates and describes the VHDL design flow to design an Actel device using Synopsys, ACTmap, or other synthesis tool, and VHDL simulator software.

Chapter 3 - Generating Netlists contains information to allow you to generate a netlist using Synopsys, ACTmap, or other synthesis tool.

Chapter 4 - Simulation with MTI V-System or Model Sim contains information and procedures about simulating for Actel designs using the Model Technology's V-System or Model Sim simulator.

Chapter 5 - Simulation With Mentor Graphics QuickHDL contains information and procedures about simulating for Actel designs using the Mentor Graphics QuickHDL simulator.

Chapter 6 - Simulation With Cadence Leapfrog contains information and procedures about simulating for Actel designs using the Cadence Leapfrog simulator.

Chapter 7 - Simulation with Viewlogic SpeedWave contains information and procedures about simulating for Actel designs using the Viewlogic SpeedWave simulator.

Chapter 8 - Simulation with Synopsys VSS contains information and procedures about simulating for Actel designs using the Synopsys VSS simulator.

Appendix A - Product Support gives information about contacting Actel for customer and technical support.

Document Assumptions

The information in this manual is based on the following assumptions:

1. You have installed the Designer Series software.
2. You have installed your VHDL VITAL simulator.
3. You are familiar with UNIX workstations and UNIX operating systems, or with PCs and Windows operating environments.
4. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

The following conventions are used throughout this manual.

Information that is meant to be input by the user is formatted as follows:

```
keyboard input
```

The contents of a file is formatted as follows:

```
file contents
```

Messages that are displayed on the screen appear as follows:

```
Screen Message
```

The following variables are used throughout this manual.

- Actel FPGA family libraries are shown as <act_fam>. Substitute the desired Actel FPGA family (act1, act2 (for ACT 2 and 1200XL devices), act3, 3200dx, 40mx, 42mx, and 54sx) as needed. For example:

  ```
  edn2vhdl fam:<act_fam> <design_name>
  ```

- Compiled VHDL libraries are shown as <vhd_fam>. Substitute <vhd_fam> for the desired VHDL family (act1, act2 (for ACT 2 and 1200XL devices), act3, a3200dx, a40mx, a42mx, and a54sx) as needed. The VHDL language requires that the library names begin with an alpha character.

Designer Series Manuals

The Designer Series software includes printed and on-line manuals. The on-line manuals are in PDF format on the CD-ROM in the "/doc" directory. These manuals are also installed onto your system when you install the Designer software. To view the on-line manuals, you must have Adobe® Acrobat Reader® installed. Actel provides Reader on the Designer Series CD-ROM.

The Designer Series includes the following manuals, which provide additional information on designing Actel FPGAs:

Designing with Actel. This manual describes the design flow and user interface for the Actel Designer Series software, including information about using the ACTgen Macro Builder and ACTmap VHDL Synthesis software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

ACTmap VHDL Synthesis Methodology Guide. This guide contains information, optimization techniques, and procedures to assist designers in the design of Actel devices using ACTmap VHDL.

Silicon Expert User's Guide. This guide contains information and procedures to assist designers in the use of Actel's Silicon Expert tool.

Cadence® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

MOTIVE™ Static Timing Analysis Interface Guide. This guide contains information and procedures to assist designers in the use of the MOTIVE software to perform static timing analysis on Actel designs.

Synopsys® Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information and procedures to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Viewlogic® Powerview Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Powerview CAE software and the Designer Series software.

Viewlogic Workview® Office Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Workview Office CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog® Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Silicon Explorer Quick Start. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Designer Series Development System Conversion Guide UNIX® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for UNIX to be compatible with later versions of Designer Series.

Designer Series Development System Conversion Guide Windows® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for Windows to be compatible with later versions of Designer Series.

FPGA Data Book and Design Guide. This guide contains detailed specifications on Actel device families. Information such as propagation delays, device package pinout, derating factors, and power calculations are found in this guide.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

On-Line Help

The Designer Series software comes with on-line help. On-line help specific to each software tool is available in Designer, ACTgen, ACTmap, Silicon Expert, and APSW.

1 Setup

This chapter contains information on setting up the Model Technology V-System or Model Sim, Mentor Graphics QuickHDL, Cadence Leapfrog, Viewlogic SpeedWave, or Synopsys VSS simulator to simulate Actel designs.

Included in this chapter are software requirements, steps describing how to compile Actel FPGA libraries, and other setup information for the simulation tool you are using.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R2-1998 or later and IEEE-1076 compliant VHDL simulators. Additionally, this guide contains information about using MTI V-System or Model Sim, Mentor Graphics QuickHDL, Cadence Leapfrog, Viewlogic SpeedWave, and Synopsys VSS simulators.

For specific information about which versions are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

User Setup

Before using the Actel VHDL VITAL models with your VHDL simulator, you must compile the Actel FPGA library models.

In addition to the standard Actel libraries, Actel provides a set of migration libraries. These libraries contain macros that were supported in earlier versions of the Designer Series software and macros that may be needed to retarget designs to a different Actel family. Actel does not recommend using the migration libraries on new designs.

This section describes the compilation procedures for each of the supported simulators.

Compiling Libraries for Model Technology's V-System or Model Sim Simulator (same for both UNIX and PC)

The following procedures describe how to compile libraries for the Model Technology V-System or Model Sim simulator.

Note: The procedure shown is for PC. The same setup procedures work similarly for UNIX. Use forward slashes in place of back slashes. For PC, commands are typed into the MTI window. On UNIX, commands are typed at the UNIX command line.

To compile an Actel VITAL library:

This procedure compiles an Actel VITAL library in the "$ALSDIR\lib\vtl\95\mti" directory. The FPGA library models must be compiled for the Actel VITAL 95 libraries to work properly.

Note: If there is already an MTI directory in $ALSDIR\lib\vtl\95 directory, compiled libraries may be present, and the following procedure may not need to be performed.

1. **Create a directory called "mti" in the "$ALSDIR\lib\vtl\95" directory.**
2. **Invoke the V-System simulator (PC only).**
3. **Change to the "$ALSDIR\lib\vtl\95\mti" directory.** Type:

   ```
   cd $ALSDIR\lib\vtl\95\mti
   ```

4. **Create a <vhd_fam> family library directory for your simulator.** Type the following command at the prompt:

   ```
   vlib <vhd_fam>
   ```

5. **Map the Actel VITAL libray to the <vhd_fam> directory.** Type the following command at the prompt:

   ```
   vmap <vhd_fam> $ALSDIR\lib\vtl\95\mti\<vhd_fam>
   ```

6. **Compile the library.** Type the following command at the prompt:

   ```
   vcom -work <vhd_fam> ..\<act_fam>.vhd
   ```

   For example, to compile the 40MX library for your simulator, type the following command:

   ```
   vcom -work a40mx ..\40mx.vhd
   ```

   Note: Perform the following step only if you are compiling the migration library.

7. **(Optional) Compile the migration library**. Type the following command at the prompt:

   ```
   vcom -work <vhd_fam> ..\<act_fam>_mig.vhd
   ```

Compiling Libraries for Mentor Graphics QuickHDL Simulator (UNIX)

The following procedures describe how to compile libraries for Mentor QuickHDL simulator.

To compile the Actel FPGA library models:

This procedure compiles an Actel VITAL library in the "$ALSDIR/lib/vtl/95/qhdl" directory. The FPGA library models must be compiled for the Actel VITAL 95 libraries to work properly.

1. **Create a directory called "qhdl" in the "$ALSDIR/lib/vtl/95" directory.**
2. **Change to the "$ALSDIR/lib/vtl/95/qhdl" directory.**
3. **Create a <vhd_fam> family library directory for your simulator.** Type:

   ```
   qhlib <vhd_fam>
   ```

4. **Map the Actel VITAL libray to the <vhd_fam> directory.** Type the following command at the prompt:

   ```
   qhmap <vhd_fam> $ALSDIR/lib/vtl/95/qhdl/<vhd_fam>
   ```

5. **Compile the library.** Type the following command at the prompt:
   ```
   qvhcom -work <vhd_fam> ../<act_fam>.vhd
   ```

For example, to compile the 40MX library for your simulator, type the following command:

```
qvhcom -work a40mx ../40mx.vhd
```

Note: Perform the following step only if you are compiling the migration library.

6. **(Optional) Compile the migration library.** Type the following command at the prompt:

```
qvhcom -work <vhd_fam> ../<act_fam>_mig.vhd
```

Compiling Libraries for Cadence's Leapfrog Simulator (UNIX)

The following procedures describe how to compile libraries for the Cadence Leapfrog simulator.

To compile the Actel FPGA library models:

This procedure compiles an Actel VITAL library in the "$ALSDIR/lib/vtl/95/lfrog" directory. The FPGA library models must be compiled for the Actel VITAL 95 libraries to work properly.

1. **Create a directory called "lfrog" in the "$ALSDIR/lib/vtl/95" directory.**
2. **Change to the "$ALSDIR/lib/vtl/95/lfrog" directory.**
3. **Create a directory named <vhd_fam>.**
4. **Map the library.** Compile the models and create the "cds.lib" file as follows:

```
INCLUDE $CDS/tools/leapfrog/files/cds.lib
DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/lfrog/<vhd_fam>
```

5. **Compile the library.** Type the following command at the prompt:

```
cv -work <vhd_fam> -messages -file $ALSDIR/lib/vtl/95/
<act_fam>.vhd
```

For example, to compile the 40MX library for your simulator, type the following command:

```
cv -work a40mx -messages -file $ALSDIR/lib/vtl/95/40mx.vhd
```

Note: Perform the following step only if you are compiling the migration library.

6. **(Optional) Compile the migration library.** Type the following command at the prompt:

```
cv -work <vhd_fam> -messages -file $ALSDIR/lib/vtl/95/
<act_fam>_mig.vhd
```

Compiling Libraries for Viewlogic's SpeedWave Simulator (PC only)

The following procedures describe how to compile Actel VITAL libraries for Viewlogic SpeedWave simulator.

Note: If you are using Workview Office 7.31A or 7.4 on a system that uses the FAT16 file system, each compiled Actel VITAL library may take up a large amount of disk space (e.g. over 200MB on a 2GB partition). Go to the Guru automated technical support system on the Actel Web site (http://www.actel.com/guru) for suggestions on how to improve disk space usage.

During the installation of the SpeedWave simulator, you can choose to install the Synopsys IEEE library or the Vantage IEEE library. The Synopsys library is needed for compatibility with the Actel VITAL libraries. The Synopsys library is a superset of the Vantage library.

To compile an Actel VITAL library in Workview Office 7.31A:

1. **Create a directory called "swave" in the "c:\actel\lib\vtl\95" directory.**
2. **Set your primary directory.** Invoke Project Manager and use the Browse button to set your primary directory to "c:\actel\lib\vtl\95\swave." Do not set your library search order.
3. **Save your project and exit Project Manager.**
4. **Invoke SpeedWave.**

5. **Open the VHDL Library Manager dialog box.** Choose the VHDL Manager command from the Tools menu or click the VHDL Manager button. The following message appears:

```
VSSLIB.INI does not exist in the directory you are running,
create or open one.
```

   Click OK. The VHDL Library Manager dialog box is displayed.

6. **Create an <act_fam> library.** Choose the Create Library command from the File menu. Browse to the "c:\actel\lib\vtl\95\swave" directory and select the <act_fam>.lib in the Library Path Name box and <act_fam> in the Symbolic Name box. Click OK.

7. **Add the <act_fam> library to the Project Libraries.** Choose the <act_fam>.lib in the "Libraries: *.lib" window and click the Add Lib button.

8. **Add system libraries to search order.** Click the List Sys Libs button. Add the IEEE.LIB and the SYNOPSYS.LIB by selecting each in the "Libraries: *.lib" window and clicking the Add Lib button.

9. **Set the <act_fam> library as the working library.** Select the "Library: <act_fam>.lib" in the Project Libraries window and click the Set Working button.

10. **Create the VSSLIB.INI file.** Choose the Save VSSLIB.INI command from the File menu.

11. **Compile the <act_fam> VITAL library.** Choose the File command from the Analyze menu. The Analyze VHDL File dialog box is displayed. Browse to the "c:\actel\lib\vtl\95" directory and select the <act_fam>.vhd file. Click the Analyze button.

12. **Check for compilation errors.** Close the Analyze VHDL File dialog box and return to the VHDL Library Manager dialog box. Check the output console window for warning or error messages.

13. **(Optional) Compile the <act_fam> VITAL migration library.** Choose the File command from the Analyze menu. The Analyze VHDL File dialog box is displayed. Browse to the "c:\actel\lib\vtl\95" directory and select the <act_fam>_mig.vhd file. Click the Analyze button.

14. **Check for compilation errors.** Close the Analyze VHDL File dialog box and return to the VHDL Library Manager dialog box. Check the output console window for any warning or error messages.

To compile an Actel VITAL library in Workview Office 7.4 and 7.5:

1. **Create a directory called "swave" in the "c:\actel\lib\vtl\95" directory.**
2. **Set your project directory.** Invoke Project Manager and click the New button. Enter "swave" in the Project Name box and "c:\actel\lib\vtl\95\swave" in the Project Directory box. Click the Next button three times, then click the Finish button to complete the process. Do not set your library search order.
3. **Save your project and exit Project Manager.**
4. **Invoke SpeedWave.**
5. **Open the HDL Library Manager window.** Choose the Analyze VHDL Design command from the File menu. Click Cancel in the Welcome dialog box. The HDL Manager window is displayed.
6. **Create a <vhd_fam> library.** Choose the Create User Library command from the File menu (Create command from the Library menu in 7.5). Specify "c:\actel\lib\vtl\95\swave" in the Library Path box and <vhd_fam> in the Symbolic Name box. Click OK.
7. **Add system libraries to search order.** Make sure that the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under the VHDL System Libraries section in the VHDL View window.
8. **Add the Actel VITAL library to the <vhd_fam> library.** Choose the Assign Source File command from the File menu (Add Source Files command from the Library menu in 7.5). Select the <act_fam>.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.
9. **Compile the Actel VITAL library.** Select the <act_fam>.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.

10. **(Optional) Add the Actel VITAL Migration library to the <vhd_fam> library.** Select the <act_fam>_mig.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.
11. **(Optional) Compile the Actel VITAL Migration library.** Select the <act_fam>_mig.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.

Compiling Libraries for Viewlogic's SpeedWave Simulator (UNIX only)

The following procedures describe how to compile libraries for Viewlogic's SpeedWave simulator.

During the installation of the SpeedWave simulator, you can choose to install the Synopsys IEEE library or the Vantage IEEE library. The Synopsys library is a superset of the Vantage library and needs to be used with the Actel VITAL libraries

The following procedures use the Vantage IEEE library. To use the Synopsys IEEE library, use the "-lib $VANTAGE_VSS/pgm/libs/synopsys.lib" switch in the "analyze" and "simulation" commands described below.

To compile the Actel FPGA library models:

This procedure compiles an Actel VITAL library in the "$ALSDIR/lib/vtl/95/swave" directory. The FPGA library models must be compiled for the Actel VITAL 95 libraries to work properly.

1. **Create a "swave" directory in the "$ALSDIR/lib/vtl/95" directory.**
2. **Change to the "$ALSDIR/lib/vtl/95/swave" directory.**
3. **Create and map a library directory for your simulator.** Type the following command at the prompt:

   ```
   vanlibcreate $ALSDIR/lib/vtl/95/swave/<vhd_fam> <vhd_fam>
   ```

4. **Compile the library.** Type the following command at the prompt:

   ```
   analyze -src ../<act_fam>.vhd -lib <vhd_fam> -libieee -lib
   $VANTAGE_VSS/pgm/lib/synopsys.lib
   ```

For example, to compile the 40MX library for your simulator, type the following command:

```
analyze -src ../40mx.vhd -lib a40mx -libieee -lib
$VANTAGE_VSS/pgm/lib/synopsys.lib
```

Note: Perform the following step only if you are compiling the migration library.

5. **(Optional) Compile the migration library models.** Type the following command at the prompt:

```
analyze -src ../<act_fam>_mig.vhd -lib <vhd_fam> -libieee
-lib $VANTAGE_VSS/pgm/lib/synopsys.lib
```

Compiling Libraries for Synopsys VSS Simulator (UNIX)

The following procedures describe how to compile libraries for the Synopsys VSS simulator.

To compile the Actel VITAL library models:

This procedure compiles an Actel VITAL library in the "$ALSDIR/lib/vtl/95/vss" directory. The VITAL library models must be compiled prior to using them to simulate.

1. **Create a "vss" directory in the "$ALSDIR/lib/vtl/95" directory.**
2. **Create a <vhd_fam> directory in the "$ALSDIR/lib/vtl/95/vss" directory.**
3. **Using a text editor, create a ".synopsys_vss.setup" file in the "$ALSDIR/lib/vtl/95/vss" directory.** Type the following command at the prompt:

```
<vhd_fam>: ./<vhd_fam>
default: ./<vhd_fam>
```

4. **Change to the "$ALSDIR/lib/vtl/95/vss" directory and compile the library.** Type the following command at the prompt:

```
cd $ALSDIR/lib/vtl/95/vss
vhdlan -w <vhd_fam> $ALSDIR/lib/vtl/95/<act_fam>.vhd
```

For example, to change to the "$ALSDIR/lib/vtl/95/vss" directory and compile the 40MX library for your simulator, type the following command:

```
cd $ALSDIR/lib/vtl/95/vss
vhdlan -w a40mx $ALSDIR/lib/vtl/95/40mx.vhd
```

Note: Perform the following step only if you are compiling the migration library.

5. **(Optional) Change to the "$ALSDIR/lib/vtl/95/vss" directory and compile the migration library.** Type the following command at the prompt:

```
cd $ALSDIR/lib/vtl/95/vss
vhdlan -w <vhd_fam> $ALSDIR/lib/vtl/95/<act_fam>_mig.vhd
```

6. **Check for any warning or error messages.**

Project Setup for Viewlogic SpeedWave (PC Only)

You must set up an Actel project in the Viewlogic Project Manager for each Actel design before creating your design in Viewlogic. The following procedures describe the process.

To set up a project in Workview Office 7.31A:

1. **Invoke Project Manager.**
2. **Set up a new project.** Choose the New command from the File menu.
3. **Set the Primary Directory.** Type the full path name of your design directory or use the Browse button.

4. **Open the Library Search Order dialog box.** Choose the Libraries command from the Project menu.

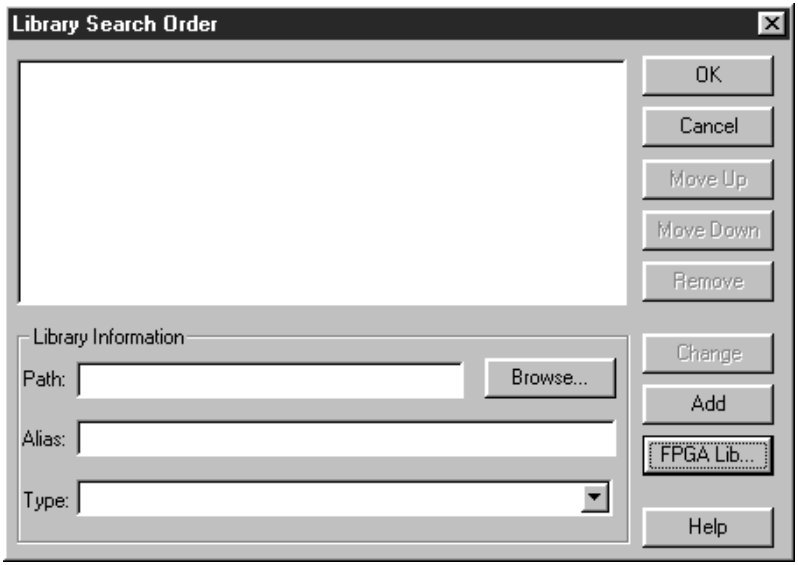

Figure 1-1. Library Search Order dialog box

5. **Select an Actel FPGA library.** Click the FPGA Lib button (see Figure 1-1). The FPGA Libraries dialog box is displayed (see Figure 1-2). Click the icon of the Actel library you want to select, then click OK.

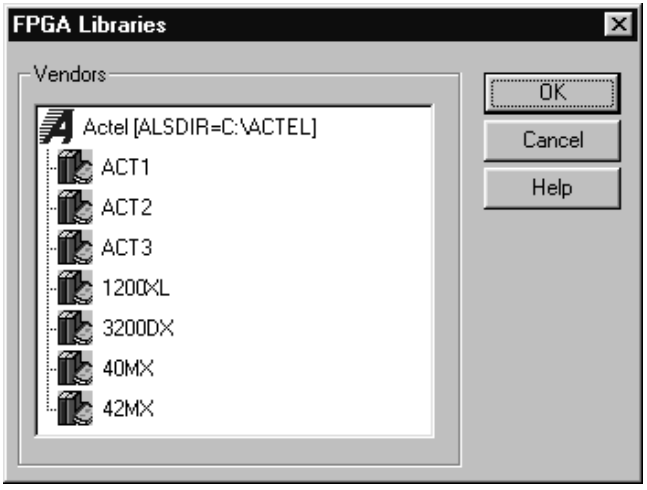

Figure 1-2. FPGA Libraries dialog box

6. **Save the project.** Choose the Save command from the File menu.

To set up a project in Workview Office 7.4 and 7.5:

1. **Invoke Project Manager.**
2. **Set up a new project.** Choose the New command from the File menu. The Creating a New Project wizard is displayed.
3. **Set the Project Directory.** Type the full path name of your design directory in the Project Directory box or use the Browse button. Type the name of your project in the Project Name box. Click the Next button.
4. **Locate your project file.** Type the full path name of your project file in the Location of Project File box or use the Browse button. Click the Next button.

5. **Select an Actel FPGA library.** Choose a library in the Configured FPGA Libraries box. Click the icon of the Actel library you want to select, then click Next.
6. **(Optional) Add additional libraries.** Click the Add button and type the full path name of the library you want to add or use the Browse button.
7. **Save the project.** Choose the Save command from the File menu.

Creating a Project Library in SpeedWave

If you use SpeedWave to simulate your designs, you must create a project library in SpeedWave, in addition to creating an Actel project in Project Manager, for each VHDL synthesis-based Actel project. The following procedures describe the process.

To create a project library in Workview Office 7.31A:

1. **Invoke SpeedWave.**
2. **Open the VHDL Library Manager dialog box.** Choose the VHDL Manager command from the Tools menu or click the VHDL Manager button. The following message appears if no VSSLIB.INI file is found in your primary directory:

```
VSSLIB.INI does not exist in the directory you are running,
create or open one.
```

   Click OK. The VHDL Library Manager dialog box is displayed.
3. **Create a project design library.** Choose the Create Library command from the File menu. The Create Library dialog box is displayed. Click the Browse button to display the Library Path Name dialog box. Make sure your primary directory is displayed. Type “user.lib” in the File Name box and click OK.
4. **Add the “user.lib” to the Project Libraries.** Click the List User Libs button. Select “user.lib” in the “Libraries: *.lib” window and click the Add Lib button.
5. **Add the compiled Actel VITAL library to the Project Libraries.** Browse to the “c:\actel\lib\vtl\95\swave” directory, select the <act_fam>.lib in the “Libraries: *.lib” window, and click the Add Lib

button. If you have not compiled the Actel VITAL library, go to "Compiling Libraries for Viewlogic's SpeedWave Simulator (PC only)" on page 5 for the procedure.

Note: Only add the <act_fam>.lib if your have referenced Actel macros in your VHDL netlist.

6. **Add system libraries to the Project Libraries.** Click the List Sys Libs button. Add the "IEEE.LIB" and the "SYNOPSYS.LIB" by selecting each in the "Libraries: *.lib" window and clicking the Add Lib button.
7. **Set the "user.lib" as the working library.** Select the "user.lib" in the Project Libraries window and click the Set Working button.
8. **Save the project library.** Choose the Save VSSLIB.INI command from the File menu.

To create a project library in Workview Office 7.4 and 7.5:

1. **Invoke SpeedWave.**
2. **Open the HDL Manager window.** Choose the Analyze VHDL Design command from the File menu. Click Cancel in the Welcome dialog box. The HDL Manager window is displayed.
3. **Setup a project.** Choose the Create User Library command from the File menu (Create command from the Library menu in 7.5). The Create Library dialog box is displayed. Make sure the path in the Library Path box is correct and already exists. Type "user" in the Symbolic Name box and click OK. Make sure no errors are reported in the Output window.
4. **Verify that the "user" library icon appears under the VHDL User Libraries section in the VHDL View window.**
5. **Add the compiled Actel VITAL library to the Project Libraries.** Choose the Add Existing User Library command from the File menu (Add to Workspace command from the Library menu in 7.5). The Add Existing Library to Workspace dialog box is displayed. Click the ellipsis box to open the Select Directory dialog box. Browse to the "c:\actel\lib\vtl\95\swave\<vhd_fam>.lib" directory and click OK. Click OK again in the Add Existing Library to Workspace dialog box. If you have not compiled the Actel VITAL library, go to

"Compiling Libraries for Viewlogic's SpeedWave Simulator (PC only)" on page 5 for the procedure.

Note: Only add the <vhd_fam>.lib if you have referenced Actel macros in your VHDL netlist.

6. **Add system libraries to the Project Libraries.** Make sure the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under VHDL System Libraries in the VHDL View window. If they are not present you must reinstall SpeedWave making sure to choose the Synopsys IEEE libraries when prompted.

7. **Save the project workspace.** Choose the Save command from the File menu.

2 Design Flow

This chapter illustrates and describes the design flow for simulating Actel designs with a VHDL VITAL compliant smulation tool.

VHDL VITAL Flow Illustrated

Figure 2-1 shows the design flow for an Actel FPGA using Designer software and a VITAL compliant VHDL simulator[1].

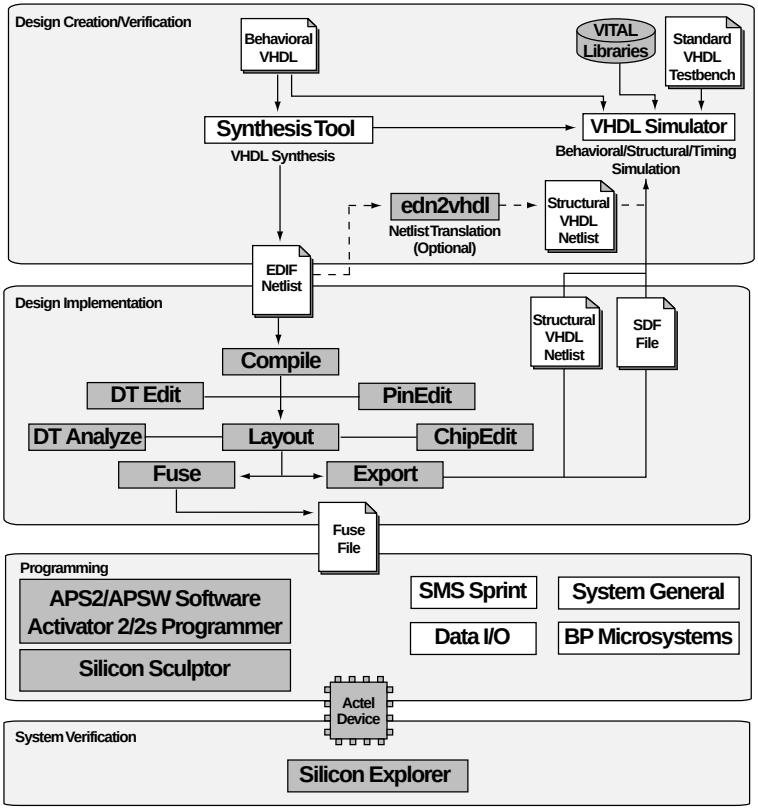

Figure 2-1. Actel-VHDL Design Flow

1. Actel-specific utilities/tools are denoted by the grey boxes in Figure 2-1.

VHDL VITAL Flow Described

The Actel VHDL VITAL design flow has four main steps; Design Creation/Verification, Design Implementation, Programming, and System Verification. These steps are described in detail in the following sections.

Design Creation/ Verification

During design creation/verification, a design is captured in an RTL-level (behavioral) VHDL source file. After capturing the design, a behavioral simulation of the VHDL file can be performed to verify that the VHDL code is correct. The code is then synthesized into an Actel gate-level (structural) VHDL netlist. After synthesis, an optional structural simulation of the design can be performed. Finally, an EDIF netlist is generated for use in Designer and a VHDL structural netlist is generated for timing simulation in a VHDL VITAL compliant simulator.

VHDL Source Entry

Enter your VHDL design source using a text editor or a context-sensitive HDL editor. Your VHDL design source can contain RTL-level constructs as well as instantiations of structural elements, such as ACTgen macros.

Behavioral Simulation

You can perform a behavioral simulation of your design before synthesis. Behavioral simulation verifies the functionality of your VHDL code. Typically, zero delays are used and a standard VHDL test bench can be used to drive simulation.

Synthesis

After you have created your behavioral VHDL design source, you must synthesize it. Synthesis translates the behavioral VHDL file into a gate-level netlist and optimizes the design for a target technology.

EDIF Netlist Generation

After you have created, synthesized, and verified your design, you must generate an Actel EDIF netlist for place and route in Designer.

This EDIF netlist is also used to generate a structural VHDL netlist for use in structural simulation.

Structural VHDL Netlist Generation

You can generate a gate-level VHDL netlist from your EDIF netlist for use in structural simulation by either exporting it from Designer or by using the Actel edn2vhdl program.

Structural Simulation

You can perform a structural simulation before placing and routing it. Structural simulation verifies the functionality of your post-synthesis structural VHDL netlist. Unit delays included in the compiled Actel VITAL libraries are used.

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, timing analysis may be performed on a design in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with a VHDL VITAL-compliant simulator.

Place and Route

Use Designer to place and route your design. Refer to the *Designing With Actel* manual for information about using Designer.

Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis on your design. Refer to the *Designing With Actel* manual for information about using DT Analyze.

Timing Simulation

You perform a timing simulation on your design after placing and routing it. Timing simulation verifies that the design meets your timing constraints.

Programming

You can program a device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designing With Actel* manual and the *APS Programming System User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Action Probe or Silicon Explorer. Refer to the *APS Programming System User's Guide* or *Silicon Explorer Quick Start* for information about using Action Probe or Silicon Explorer.

3 Generating Netlists

This chapter describes the procedures for generating EDIF and structural VHDL netlists.

Generating an EDIF Netlist

After capturing your schematic or synthesizing your design, generate an EDIF netlist from your schematic capture or synthesis tool. The EDIF netlist is used for place and route in Designer. Refer to the documentation included with your schematic capture or synthesis tool for information about generating an EDIF netlist.

Make sure to specify VHDL for the naming style when importing the EDIF netlist into Designer.

Generating a Structural VHDL Netlist

You can generate structural VHDL netlist using Designer or the "edn2vhdl" program. The structural VHDL netlist is used for structural and timing simulation.

To generate a structural netlist using Designer:

1. **Invoke Designer.**
2. **Import the EDIF netlist.** Choose the Import Netlist File command from the File menu. The Import Netlist dialog box is displayed. Specify EDIF as the Netlist Type, GENERIC as the Edif flavor, and VHDL as the Naming Style. Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK.
3. **Export a structural VHDL netlist.** Choose the Export command from the File menu. The Export dialog box is displayed. Specify Netlist File as the File Type and VHDL as the Format. Click OK.

To generate a structural netlist using "edn2vhdl":

1. **Change to the directory that contains the VHDL design files.**
2. **Type the following command at the UNIX or DOS prompt:**

```
edn2vhdl FAM:{<act_fam>}
[ EDNIN:<Edif_File1>[+<Edif_File2...>] ]
[ VHDOUT:<Vhdl_File> ]
<design_name>
```

The "EDNIN" option specifies the EDIF input file(s). You can specify multiple files with the "+" delimiter between file names. The default EDIF input file is <design_name>.edn. The "VHDOUT" option specifies the VHDL output file names. The default VHDL output file is <design_name>.vhd.

4

Simulation with MTI V-System or Model Sim

This chapter describes steps to perform Functional (Behavioral and Structural) and Timing simulation for Actel devices using the Model Technology's V-System or Model Sim simulator.

The procedures shown are for PC. The same setup procedures work similarly for UNIX. Use forward slashes in place of back slashes. For PC, commands are typed into the MTI window. On UNIX, commands are typed into a UNIX window.

Behavioral Simulation

After the VHDL descriptions of the logic blocks have been coded, test and debug the design using the MTI simulator. Use the following procedure to perform behavioral simulation.

Note: Skip step 1 for UNIX platforms.

1. **Invoke your V-System or Model Sim simulator.** For information regarding MTI usage, refer to your Model Technology V-System or Model Sim user's manual.
2. **Change directory to your project directory.** This directory must include your VHDL design files and testbench. Type:

   ```
   cd <project_dir>
   ```

3. **Map to the Actel Library.** If any Actel macros are instantiated in your VHDL source, run the following command to map them to the compiled Actel VITAL library.

   ```
   vmap <vhd_fam> $ALSDIR\lib\vtl\95\mti\<vhd_fam>
   ```

   To reference the Actel family library in your VHDL design files, add the following lines to your VHDL design files:

   ```
   library <vhd_fam>;
   use <vhd_fam>.components.all;
   ```

4. **Create a "work" directory.** Type:

   ```
   vlib work
   ```

5. **Map to the "work" directory.** Type:

```
vmap work .\work
```

6. **Perform a behavioral simulation of your design.** To perform a behavioral simulation using your V-System or Model Sim simulator, compile your VHDL design and testbench files and run a simulation. For hierarchical designs, compile the lower level design blocks before the higher level design blocks.

   Note: If you are using ACTmap Asyl Packages for synthesis you will need to compile the Asyl packages first. For more information refer to *ACTmap VHDL Synthesis Methodology Guide*.

   The following commands demonstrate how to compile VHDL design and testbench files:

```
vcom <behavioral>.vhd
vcom <test_bench>.vhd
```

   To simulate the design, type:

```
vsim <configuration_name>
```

   For example:

```
vsim test_adder_behave
```

   The entity-architecture pair specified by the configuration named test_adder_behave in the testbench will be simulated.

Structural Simulation

Use the following procedure to perform structural simulation.

1. **Generate a structural VHDL netlist.**

   If you are using Synopsys Design Compiler or ACTmap, generate the structural VHDL netlist from these tools.

   If you are using other synthesis tools, generate a gate level VHDL from your EDIF netlist by either exporting it from Designer or by using the edn2vhdl program.

To generate a netlist using edn2vhdl:

Type:

```
edn2vhdl fam:<act_fam> <design_name>
```

To generate a netlist using Designer Series software:

Select the Import Netlist command from the File menu of the Designer window. Specify EDIF as the Netlist Type, GENERIC as the Edif Flavor, and VHDL as the Naming Style. Use the Browse utility to search for the EDIF netlist of your design.

Select the Export command from the Designer File menu and select Netlist VHDL.

Note: The VHDL generated by both Designer and the edn2vhdl program will use std_logic for all ports. The bus ports will be in the same bit order as they appear in the EDIF netlist.

2. **Map to the Actel VITAL library.** Run the following command to map the compiled Actel VITAL library.

   ```
   vmap <vhd_fam> $ALSDIR\lib\vtl\95\mti\<vhd_fam>
   ```

3. **Compile the structural netlist.** Compile your VHDL design and testbench files. The following commands demonstrate how to compile VHDL design and testbench files:

   ```
   vcom <structural>.vhd -just e
   vcom <structural>.vhd -just a
   ```

```
vcom <test_bench>.vhd
```

Note: The previous steps compile the entities first, and then the architectures, as required for VHDL netlists written by some tools.

4. **Run the structural simulation.** To simulate your design, type:

```
vsim <configuration_name>
```

For example:

```
vsim test_adder_structure
```

The entity-architecture pair specified by the configuration named test_adder_structure in the testbench will be simulated.

Timing Simulation

Use the following procedure to perform timing simulation.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a (design_name>.sdf file by specifying SDF as the CAE type. Click OK.
3. **Compile the structural netlist.** To perform a timing simulation using your V-System or Model Sim simulator, compile your VHDL design and testbench files, if they have not already been compiled for a structural simulation, and run a simulation. The following commands demonstrate how to compile VHDL design and testbench files:

```
vcom <structural>.vhd -just e
vcom <structural>.vhd -just a
vcom <test_bench>.vhd
```

Note: The previous steps compile the entities first, and then the architectures, as required for VHDL netlists written by some tools.

4. **Run the back annotation simulation using the timing information in the SDF file.** Type:

```
vsim -sdf[max|typ|min] /<region>=<design name>.sdf -c
<configuration_name>
```

The <region> option specifies the region (or path) to an instance in a design where back annotation begins. You can use it to specify a particular FPGA instance in a larger system design or testbench that you wish to back annotate. For example:

```
vsim -sdfmax /uut=adder.sdf -c test_adder_structural
```

In this example, the entity “adder” has been instantiated as instance “uut” in the testbench. The entity-architecture pair specified by the configuration named “test_adder_structural” in the testbench will be simulated using the maximum delays specified in the SDF file.

5
Simulation With Mentor Graphics QuickHDL

This chapter describes steps to perform Functional (Behavioral and Structural) and Timing simulation for Actel devices using the Mentor Graphics QuickHDL simulator.

Behavioral Simulation

After the VHDL descriptions of the logic blocks have been coded, test and debug the design using the QuickHDL simulator. Use the following procedure to perform behavioral simulation.

1. **Change directory to your project directory.** This directory must include your VHDL design files and testbench.
2. **Map to the Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, run the following command to map them to the compiled Actel VITAL library in $ALSDIR.

   ```
   qhmap <vhd_fam> $ALSDIR/lib/vtl/95/qhdl/<vhd_fam>
   ```

   Add the following lines to your VHDL design files to reference the Actel Family library in your VHDL design files:

   ```
   library <vhd_fam>;
   use <vhd_fam>.components.all;
   ```

3. **Create a "work" directory.** Type:

   ```
   qhlib work
   ```

4. **Map to the "work" directory.** Type:

   ```
   qhmap work ./work
   ```

5. **Perform a behavioral simulation of your design.** To perform a behavioral simulation using QuickHDL simulator, compile your VHDL design and testbench files and run a simulation.

   Note: If you are using ACTmap Asyl Packages for synthesis you must compile the Asyl packages first. For more information on Asyl packages refer to the *ACTmap VHDL Synthesis Methodology Guide*.

The following commands demonstrate how to compile VHDL design and testbench files:

```
qvhcom <behavioral>.vhd
qvhcom <test_bench>.vhd
```

To simulate the design, type:

```
qhsim <configuration_name>
```

where <configuration_name> is the name of the configuration that binds the test bench architecture to the test bench entity.

Structural Simulation

Use the following procedure to perform structural simulation.

1. **Generate a structural VHDL netlist.**

   If you are using Synopsys Design Compiler or ACTmap, generate the structural VHDL netlist from these tools.

   If you are using other synthesis tools, generate a gate level VHDL from your EDIF netlist by either exporting it from Designer or by using the edn2vhdl program.

To generate a netlist using edn2vhdl:

Type:

```
edn2vhdl fam:<act_fam> <design_name>
```

To generate a netlist using Designer Series software:

Select the Import Netlist command from the File menu of the Designer window. Specify EDIF as the Netlist Type, GENERIC as the Edif Flavor, and VHDL as the Naming Style. Use the Browse utility to search for the EDIF netlist of your design.

Select the Export command from the Designer File menu and select Netlist VHDL.

Note: The VHDL generated by both Designer and the edn2vhdl program will use std_logic for all ports. The bus ports will be in the same bit order as they appear in the EDIF netlist.

2. **Map to the Actel VITAL library.** Run the following command to map the compiled Actel VITAL library:

```
qhmap <vhd_fam> $ALSDIR/lib/vtl/95/qhdl/<vhd_fam>
```

3. **Compile the structural netlist.** Compile your VHDL design and testbench files. The following commands demonstrate how to compile VHDL design and testbench files:

```
qvhcom <structural>.vhd -just e
qvhcom <structural>.vhd -just a
qvhcom <test_bench>.vhd
```

Note: The previous steps compile the entities first, and then the architectures, as required for VHDL netlists written by some tools.

4. **Run the structural simulation.** To simulate your design, type:

```
qhsim <configuration_name>
```

For example:

```
qhsim test_adder_structure
```

The entity-architecture pair specified by the configuration named test_adder_structure in the testbench will be simulated.

Timing Simulation

Use the following procedure to perform timing simulation.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The

Extract dialog box is displayed. Create a (design_name>.sdf file by specifying SDF as the CAE type. Click OK.

3. **Compile the structural netlist.** To perform a timing simulation using the QuickHDL simulator, compile your VHDL design and testbench files, if they have not already been compiled for a structural simulation, and run a simulation. The following commands demonstrate how to compile VHDL design and testbench files:

```
qvhcom <structural>.vhd -just e
qvhcom <structural>.vhd -just a
qvhcom <test_bench>.vhd
```

Note: The previous steps compile the entities first, and then the architectures, as required for VHDL netlists written by some tools.

4. **Run the back annotation simulation using the timing information in the SDF file.** Type:

```
qhsim -sdf[max|typ|min] /<region>=<design name>.sdf -c
<configuration_name>
```

The <region> option specifies the region (or path) to an instance in a design where backannotation begins. You can use it to specify a particular FPGA instance in a larger system design or test bench that you wish to backannotate. For example:

```
qhsim -sdfmax /uut=adder.sdf -c test_adder_structural
```

In this example, the entity “adder” has been instantiated as instance “uut” in the testbench. The entity-architecture pair specified by the configuration named “test_adder_structural” in the testbench will be simulated using the maximum delays specified in the SDF file.

6 Simulation With Cadence Leapfrog

This chapter describes steps to perform Functional (Behavioral and Structural) and Timing simulation for Actel devices using the Cadence Leapfrog simulator.

Behavioral Simulation

After the VHDL descriptions of the logic blocks have been coded, test and debug the design using the Leapfrog simulator. Use the following procedure to perform behavioral simulation.

1. **Create a work directory and a cds.lib file in the project directory.** At the UNIX prompt, enter:

   ```
   mkdir work
   ```

   Using a text editor, create a cds.lib file and enter the following lines:

   ```
   INCLUDE $CDS/tools/leapfrog/files/cds.lib
   ```

2. **Map to the Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, add the following lines to your cds.lib file to map them to the compiled Actel VITAL library.

   ```
   DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/lfrog/<vhd_fam>
   DEFINE WORK ./work
   ```

   Add the following lines to your VHDL design files to reference the Actel Family library in your VHDL design files:

   ```
   library <vhd_fam>;
   use <vhd_fam>.components.all;
   ```

3. **Compile the VHDL design and test bench files.** Type:

   ```
   cv -work work -messages -file <behavioral>.vhd
   cv -work work -messages -file <test_bench>.vhd
   ```

   Note: If you are using ACTmap Asyl Packages for synthesis you must compile the Asyl packages first. For more information on Asyl packages refer to the *ACTmap VHDL Synthesis Methodology Guide*.

4. **Elaborate the design.** Type:

   ```
   ev -work work -messages <configuration_name>
   ```

   Where <configuration_name> is the name of the configuration in the test bench.

   For example

   ```
   ev -work work -messages test_add_behave
   ```

   The entity-architecture pair specified by the configuration named test_adder_behave in the testbench will be elaborated.

   If you have instantiated Actel Library Cells in your behavioral VHDL, you must use the -compatibility switch when elaborating your design as shown below:

   ```
   ev -work work -messages -compatibility <configuration_name>
   ```

5. **Perform a behavioral simulation of your design.** Type:

   ```
   sv -batch -run <configuration_name>
   ```

   Where <configuration_name> is the name of the configuration in the test bench.

   For example:

   ```
   sv -batch -run test_add_behave
   ```

Structural Simulation

Use the following procedure to perform structural simulation.

1. **Generate a structural VHDL netlist.**

   If you are using Synopsys Design Compiler or ACTmap, generate the structural VHDL netlist from these tools.

   If you are using other synthesis tools, generate a gate level VHDL from your EDIF netlist by either exporting it from Designer or by using the edn2vhdl program.

To generate a netlist using edn2vhdl:

Type:

```
edn2vhdl fam:<act_fam> <design_name>
```

To generate a netlist using Designer Series software:

Select the Import Netlist command from the File menu of the Designer window. Specify EDIF as the Netlist Type, GENERIC as the Edif Flavor, and VHDL as the Naming Style. Use the Browse utility to search for the EDIF netlist of your design.

Select the Export command from the Designer File menu and select Netlist VHDL.

Note: The VHDL generated by both Designer and edn2vhdl will use std_logic for all ports. The bus ports will be in the same bit order as they appear in the EDIF netlist.

2. **Map to the Actel VITAL library.** Create a cds.lib file in the project directory as follows:

```
INCLUDE $CDS/tools/leapfrog/files/cds.lib
DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/lfrog/<vhd_fam>
DEFINE WORK ./work
```

3. **Compile the VHDL design and test bench files.** Type:

```
cv -work work -messages -file <structural>.vhd
cv -work work -messages -file <test_bench>.vhd
```

4. **Elaborate the design in compatibility mode.** Type:

```
ev -work work -messages -compatibility <configuration_name>
```

Where <configuration_name> is the name of your configuration that binds the test bench entity and architecture.

For example:

```
ev -work work -messages -compatibility test_adder_structure
```

In the example, “test_adder_structure” is the name of configuration for the test bench.

5. **Perform a structural simulation of your design.** Type:

```
sv -batch -run <configuration_name>
```

Where <configuration_name> is name of the test bench configuration.

For example:

```
sv -batch -run test_adder_structure
```

Here the name of the test bench configuration is test_adder_structure.

Timing Simulation

Use the following procedure to perform timing simulation.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a (design_name>.sdf file by specifying SDF as the CAE type. Click OK
3. **Map Actel VITAL library.** If not already done for structural simulation, create a cds.lib file in the project directory as follows:

```
INCLUDE $CDS/tools/leapfrog/files/cds.lib
DEFINE <vhd_fam> $ALSDIR/lib/vtl/95/lfrog/<vhd_fam>
DEFINE WORK ./work
```

4. **Compile the VHDL design and test bench files.** If not already done for structural simulation, type:

```
cv -work work -messages -file <structural>.vhd
cv -work work -messages -file <test_bench>.vhd
```

5. **Elaborate the design in compatibility mode.** Type:

```
ev -work work -messages -compatibility -bsdf ./<design
name>.sdf -bmtm [max|typ|min] -bscope <UUT>
<configuration_name>
```

Where <design_name> is name of top level entity, <UUT> is the instance of the top level entity in the test bench, and <configuration_name> is the name of your configuration that binds the test bench entity and architecture.

For example:

```
ev -work work -messages -compatibility -bsdf adder.sdf -bmtm
max -bscope dut test_adder_structure
```

In the above example, “adder” is the name of the top level entity, “test_adder_structure” is the name of configuration for the test bench and “dut” is instance of the top-level entity “adder” in the test bench.

6. **Perform a timing simulation of your design.** Type:

```
sv -batch -run <configuration_name>
```

Where <configuration_name> is name of the test bench configuration.

For example:

```
sv -batch -run test_adder_structure
```

Here the name of the test bench configuration is test_adder_structure.

7
Simulation with Viewlogic SpeedWave

This chapter describes the procedures for performing simulations on an Actel design using the Viewlogic SpeedWave simulation tool. Refer to the Viewlogic documentation for additional information about performing simulation with SpeedWave.

Behavioral Simulation (PC)

Use the following procedures to perform a behavioral simulation of an Actel design on a PC.

To simulate a design using SpeedWave 7.31A:

1. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 10 for the procedure.
2. **Invoke SpeedWave.**
3. **Open the VHDL Library Manager dialog box.** Choose the VHDL Manager command from the Tools menu. If the following message appears:

   ```
   VSSLIB.INI does not exist in the directory you are running,
   create or open one.
   ```

   You must create a project library before continuing. Go to "Creating a Project Library in SpeedWave" on page 13 for the procedure.
4. **Analyze your behavioral VHDL design files and test bench.** Choose the File command from the Analyze menu. The Analyze VHDL File dialog box is displayed. Select each file from the VHDL Source File Name window and click the Analyze button.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.
5. **Select a configuration to simulate**. Double-click the "user.lib" in the Project Libraries window to display its contents. Select the configuration you want to simulate and click the Simulate Obj button. A SCHEMLES window and a VHDL source window are displayed in the main window.

6. **Simulate your design**. Choose the Run command from the Simulate menu. The Run dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

To simulate a design using SpeedWave 7.4 and 7.5:

1. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 10 for the procedure.
2. **Invoke SpeedWave.**
3. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click the Cancel button in the Welcome dialog box and go to "Creating a Project Library in SpeedWave" on page 13 for the procedure.
4. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select a .hws file and click the Open button in the Open dialog box.
5. **Analyze your behavioral VHDL design files and test bench.** Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Assign Source Files command from the File menu (Add Source Files command from the Library menu in 7.5). The Assign Source Files dialog box is displayed. Select the behavioral VHDL and test bench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.
6. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.

7. **Simulate your design**. Choose the Run command (Run Simulation command in 7.5) from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

Structural Simulation (PC)

Use the following procedures to perform a structural simulation of an Actel design on a PC.

To simulate a design using SpeedWave 7.31A:

1. **Synthesize your design.** Refer to the documentation included with your synthesis tool for information about synthesis.
2. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 10 for the procedure.
3. **Invoke SpeedWave.**
4. **Open the VHDL Library Manager dialog box.** Choose the VHDL Manager command from the Tools menu. If the following message appears:

```
VSSLIB.INI does not exist in the directory you are running,
create or open one.
```

   You must create a project library before continuing. Go to "Creating a Project Library in SpeedWave" on page 13 for the procedure.
5. **Analyze the your structural VHDL netlist and test bench.** If you have not already generated a structural VHDL netlist, go to "Generating a Structural VHDL Netlist" on page 21 for the procedure. Choose the File command from the Analyze menu. The Analyze VHDL File dialog box is displayed. Select each file from the VHDL Source File Name window and click the Analyze button.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.

6. **Select a configuration to simulate.** Double-click the "user.lib" in the Project Libraries window to display its contents. Select the configuration you want to simulate and click the Simulate Obj button. A SCHEMLES window and a VHDL source window are displayed in the main window.

7. **Simulate your design.** Choose the Run command from the Simulate menu. The Run dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

To simulate a design using SpeedWave 7.4 and 7.5:

1. **Synthesize your design.** Refer to the documentation included with your synthesis tool for information about synthesis.

2. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 10 for the procedure.

3. **Invoke SpeedWave.**

4. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click the Cancel button in the Welcome dialog box and go to "Creating a Project Library in SpeedWave" on page 13 for the procedure.

5. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select a .hws file and click the Open button in the Open dialog box.

6. **Analyze your structural VHDL netlist and test bench.** If you have not already generated a structural VHDL netlist, go to "Generating a Structural VHDL Netlist" on page 21 for the procedure. lect the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Assign Source Files command from the File menu (Add Source Files command from the Library menu in 7.5). The Assign Source Files dialog box is displayed. Select the structural VHDL netlist and test bench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze

menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.

7. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.
8. **Simulate your design**. Choose the Run command (Run Simulation command in 7.5) from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

Timing Simulation (PC)

Use the following procedures to perform a timing simulation of an Actel design on a PC.

To simulate a design using SpeedWave 7.31A:

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design from Designer.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog is displayed. Create a <design_name>.sdf file by choosing the SDF option from the CAE pull-down menu. Click OK.
3. **Select your Actel project in Project Manager.** If you have not created a project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 10 for the procedure.
4. **Invoke SpeedWave.**

5. **Open the VHDL Library Manager dialog box.** Choose the VHDL Manager command from the Tools menu. If the following message appears:

```
VSSLIB.INI does not exist in the directory you are running,
create or open one.
```

   You must create a project library before continuing. Go to "Creating a Project Library in SpeedWave" on page 13 for the procedure.

6. **(Optional) Analyze your VHDL design files and test bench.** Skip this step if you are using the same structural VHDL netlist and test bench you analyzed for structural simulation. Choose the File command from the Analyze menu. The Analyze VHDL File dialog box is displayed. Select each file from the VHDL Source File Name window and click the Analyze button. Close the dialog box.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.

7. **Select a configuration to simulate.** Choose the Load VHDL Design command from the File menu. The Load VHDL Design dialog box is displayed. Click the Design Unit index tab to display the Select Top Level Entity, Architecture, or Configuration window. Double-click the "user.lib" in the window to display its contents. Select the configuration you want to simulate.

8. **Import the timing information for your design.** Click the VITAL Timing index tab. Click the Perform SDF Back Annotation check box and click OK. The Setup SDF Back Annotation dialog box is displayed. Type the name of your <design_name>.sdf in the SDF File box or use the Browse button.

9. **Add Scope options.** In the Scope window, fill in the name of the instance in the test bench you want to back annotate (e.g. "/uut"). Select the Delay Mode you want to use (Minimum, Typical, or Maximum). Click the Add button and verify that Scope, File, and Timing settings are correct in the main window. Use the Change and Remove buttons to make any corrections.

10. **Back annotate your design.** Click OK.

11. **Simulate your design.** Choose the Run command from the Simulate menu. The Run dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

To simulate a design using SpeedWave 7.4 and 7.5:

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design from Designer.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog is displayed. Create a <design_name>.sdf file by choosing the SDF option from the CAE pull-down menu. Click OK.
3. **Select your Actel project in Project Manager.** If you have not created a project, go to "Project Setup for Viewlogic SpeedWave (PC Only)" on page 10 for the procedure.
4. **Invoke SpeedWave.**
5. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click the Cancel button in the Welcome dialog box and go to "Creating a Project Library in SpeedWave" on page 13 for the procedure.
6. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select a .hws file and click the Open button in the Open dialog box.
7. **(Optional) Analyze your VHDL design files and test bench.** Skip this step if you are using the same structural VHDL netlist and test bench you analyzed for structural simulation. Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Assign Source Files command from the File menu (Add Source Files command from the Library menu in 7.5). The Assign Source Files dialog box is displayed. Select the structural VHDL netlist and test bench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output

window for successful completion. Save the HDL workspace and close the HDL Manager window.

Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.

8. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.

9. **Import the timing information for your design.** Click the VITAL Timing index tab. Click the Perform SDF Back Annotation check box and click OK. The Setup SDF Back Annotation dialog box is displayed. Type the name of your <design_name>.sdf in the SDF File box or use the Browse button.

10. **Add Scope options.** In the Scope window, fill in the name of the instance in the test bench you want to back annotate (e.g. "/uut"). Select the Delay Mode you want use (Minimum, Typical, or Maximum). Click the Add button and verify that Scope, File, and Timing settings are correct in the main window. Use the Change and Remove buttons to make any corrections.

11. **Back annotate your design.** Click OK.

12. **Simulate your design**. Choose the Run command (Run Simulation command in 7.5) from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

Behavioral Simulation (UNIX)

Use the following procedure to perform a behavioral simulation of an Actel design on UNIX.

1. **Create a working directory.** For more information refer to the Viewlogic manuals. Type:

   ```
   vanlibcreate ./user.lib user
   ```

2. **Create a soft link to the synopsys library.** Type:

   ```
   ln -s $VANTAGE_VSS/pgm/libs/synopsys.lib synopsys
   ```

   Note: When installing the Viewlogic SpeedWave simulator, you have the option of installing a pristine IEEE library or the Synopsys version. The Synopsys library is needed for compatibility with the Actel VITAL libraries. If you have installed the Synopsys version you will need to include the Synopsys library in your invocations. The commands in this manual are shown for the Synopsys version of IEEE libraries.

3. **Analyze your vhdl design files and test bench.**

   ```
   analyze -src <behavioral>.vhd -lib user.lib -libieee -lib
   synopsys
   analyze -src <test_bench>.vhd -lib user.lib -libieee -lib
   synopsys
   ```

4. **Map to the compiled Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, you must add the following switches when analyzing your VHDL design files:

   ```
   analyze -src <behavioral>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
   ```

   Add the following lines to your VHDL design files to reference the Actel Family library in your VHDL design files:

   ```
   library <vhd_fam>;
   use <vhd_fam>.components.all;
   ```

   Note: If you are using ACTmap Asyl Packages for synthesis you must compile the Asyl packages first. For more information

on Asyl packages refer to *ACTmap VHDL Synthesis Methodology Guide*.

5. **Simulate your design.** Type:

```
vbsim -cfg <configuration_name> -until complete -lib
user.lib -libieee -lib synopsys
```

6. **Map to the compiled Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, you must add the following switches when simulating your VHDL design files:

```
vbsim -cfg <configuration_name> -until complete -lib
user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/
swave/<vhd_fam>
```

where <configuration_name> is the name of the configuration that binds the test bench entity and architecture.

For example:

```
vbsim -cfg test_add_behave -until complete -lib user.lib
-libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
```

Here the configuration named test_add_behave will be simulated.

Structural Simulation (UNIX)

Use the following procedure to perform a structural simulation of an Actel design on UNIX.

1. **Generate a structural VHDL netlist.**

   If you are using Synopsys Design Compiler or ACTmap, generate the structural VHDL netlist from these tools.

   If you are using other synthesis tools, generate a gate level VHDL from your EDIF netlist by either exporting it from Designer or by using the edn2vhdl program.

To generate a netlist using edn2vhdl:

Type:

```
edn2vhdl fam:<act_fam> <design_name>
```

To generate a netlist using Designer Series software:

Select the Import Netlist command from the File menu of the Designer window. Specify EDIF as the Netlist Type, GENERIC as the Edif Flavor, and VHDL as the Naming Style. Use the Browse utility to search for the EDIF netlist of your design.

Select the Export command from the Designer File menu and select Netlist VHDL.

Note: The VHDL generated by both Designer and the edn2vhdl program will use std_logic for all ports. The bus ports will be in the same bit order as they appear in the EDIF netlist.

2. **Analyze the structural VHDL and the Test bench.** Type:

```
analyze -src <structural>.vhd -lib user.lib -lib $ALSDIR/
lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys

analyze -src <test_bench>.vhd -lib user.lib -lib $ALSDIR/
lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
```

3. **Perform a structural simulation of your design.** To perform a structural simulation using your SpeedWave simulator, type:

```
vbsim -cfg <configuration_name> -until complete
-lib user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/
95/swave/<vhd_fam>
```

For example:

```
vbsim -cfg test_add_structure -until complete -lib user.lib
-libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
```

Here the configuration specified by test_add_structure will be simulated.

Timing Simulation (UNIX)

Use the following procedure to perform a timing simulation of an Actel design on UNIX.

1. **Compile the structural netlist.** To perform a timing simulation using your SpeedWave simulator, compile your VHDL design and testbench files, if not already done for structural simulation, and run simulation.

   The following commands demonstrate how to compile VHDL design and testbench files:

   ```
   analyze -src <structural>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys


   analyze -src <test_bench>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
   ```

2. **Run the back annotation simulation using the timing information from the SDF file.** Type:

   ```
   vbsim -cfg <configuration_name> -until complete -lib
   user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/
   swave/<vhd_fam> -sdf <design_name>.sdf <UUT> -sdfmode
   [min|typ|max]
   ```

   Where <configuration_name> is the name of your configuration that binds the test bench entity and architecture, <design_name> is name of top level entity, <UUT> is the instance of the top level entity in the test bench.

8

Simulation with Synopsys VSS

This chapter describes steps to perform Functional (Behavioral and Structural) and Timing simulation for Actel devices using the Synopsys VSS simulator.

Behavioral Simulation

After the VHDL descriptions of the logic blocks have been coded, test and debug the design using the VSS simulator. Use the following procedure to perform behavioral simulation.

1. **Create a working directory.** Use the UNIX *mkdir* command to create a directory for VSS to use as your working directory.

   ```
   mkdir work
   ```

2. **Using a text editor, create a ".synopsys_vss.setup" file in your current directory containing the following lines:**

   ```
   work > default
   default: ./work
   ```

3. **Map to the compiled Actel VITAL library.** If any Actel macros are instantiated in your VHDL source, you must add the following line to your ".synopsys_vss.setup" file:

   ```
   <vhd_fam>: $ALSDIR/lib/vtl/95/vss/<vhd_fam>
   ```

4. **Analyze your VHDL design files and test bench.** Use the *vhdlan* command to compile your VHDL source files:

   ```
   vhdlan <behavioral>.vhd
   vhdlan <test_bench>.vhd
   ```

5. **Create a vss.dofile to run simulation in batch mode.** Enter the following lines:

   ```
   run
   quit
   ```

6. **Simulate your design.** Use the vhdlsim command to simulate your testbench configuration:

   ```
   vhdlsim -t ps -i vss.dofile <configuration_name>
   ```

Structural Simulation

Use the following procedure to perform structural simulation.

1. **Generate a structural VHDL netlist.**

   If you are using Synopsys Design Compiler or ACTmap, generate the structural VHDL netlist from these tools.

   If you are using other synthesis tools, generate a gate level VHDL from your EDIF netlist by either exporting it from Designer or by using the edn2vhdl program.

To generate a netlist using edn2vhdl:

Type:

```
edn2vhdl fam:<act_fam> <design_name>
```

To generate a netlist using Designer Series software:

Select the Import Netlist command from the File menu of the Designer window. Specify EDIF as the Netlist Type, GENERIC as the Edif Flavor, and VHDL as the Naming Style. Use the Browse utility to search for the EDIF netlist of your design.

Select the Export command from the Designer File menu and select Netlist VHDL.

Note: The VHDL generated by both Designer and the edn2vhdl program will use std_logic for all ports. The bus ports will be in the same bit order as they appear in the EDIF netlist.

2. **Analyze your structural VHDL netlist and test bench.** Use the *vhdlan* command to compile your VHDL source files:

```
vhdlan <structural>.vhd
vhdlan <test_bench>.vhd
```

3. **Simulate your design.** Use the vhdlsim command to simulate your testbench configuration:

```
vhdlsim -t ps -i vss.dofile <configuration_name>
```

Timing Simulation

Use the following procedure to perform timing simulation.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a (design_name>.sdf file by specifying SDF as the CAE type. Click OK.
3. **Analyze your structural VHDL netlist and test bench.** Use the *vhdlan* command to compile your VHDL source files:

   ```
   vhdlan <structural>.vhd
   vhdlan <test_bench>.vhd
   ```

4. **Simulate your design using SDF back annotation.** Use the vhdlsim command with the SDF back annotation options to simulate your test bench configuration:

   ```
   vhdlsim -t ps -i vss.dofile -sdf_max -sdf_top
   <top_entity_name>/<instance_name> -sdf <design_name>.sdf
   <configuration_name>
   ```

   Substitute “-sdf_min” or “-sdf_typ” for “-sdf_max” to use the minimum or typical delays, respectively. Subsitute the name of your configuration that binds the test bench entity and architecture for <configuration_name>, the top-level entity in your test bench for <top_entity_name>, and the instance of the design for <instance_name>.

A

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Actel backs its products with various technical support services including a Web site, monthly Fax Broadcast, a fax back service, a bulletin board system, electronic mail, Customer Service, and a Customer Applications Center.

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All calls are answered by our Technical Message Center. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 a.m. to 5 p.m., Pacific Standard Time, Monday through Friday.

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