Viewlogic® Workview® Office

Interface Guide

Windows® Environments

Actel Corporation, Sunnyvale, CA 94086

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Introduction

The *Viewlogic Workview Office Interface Guide* contains information about using the Viewlogic Workview Office CAE software tools with the Actel Designer Series FPGA development software tools to create designs for Actel devices. Refer to the *Designing with Actel* manual for additional information about using the Designer series software and the Viewlogic documentation for information about using the Workview Office software.

Document Organization

The *Viewlogic Workview Office Interface Guide* is divided into the following chapters:

Chapter 1 - Setup contains information and procedures about setting up the Workview Office software for use in creating Actel designs.

Chapter 2 - Design Flow illustrates and describes the design flow for creating Actel designs using Workview Office software and Designer Series software.

Chapter 3 - Actel-Viewlogic Design Considerations contains information and procedures to assist you in creating Actel designs with Workview Office and Designer Series software.

Chapter 4 - Simulation Using ViewSim® contains information and procedures about simulating Actel designs with ViewSim.

Chapter 5 - Simulation Using SpeedWave™ contains information and procedures about simulating Actel designs with SpeedWave.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

The information in this guide is based on the following assumptions:

1. You have installed the Designer Series software in the “C:\Actel” directory.

2. You have installed the Workview Office software in the "C:\Wvoffice" directory.
3. You are familiar with PCs and Windows operating environments.
4. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

The following conventions are used throughout this manual.

Information that is meant to be input by the user is formatted as follows:

```
keyboard input
```

The content of a file is formatted as follows:

```
file contents
```

Messages that are displayed on the screen appear as follows:

```
Screen Message
```

The <act_fam> variable represents an Actel device family. To reference an actual family, substitute the name of the Actel device when you see this variable. Available families are act1, act2 (for ACT 2 and 1200XL devices), act3, 3200dx, 40mx, 42mx, and 54sx.

The <vhd_fam> variable represents Compiled VHDL libraries. To reference an actual compiled library, substitute the name of the library (act1, act2 (for ACT 2 and 1200XL devices), act3, a3200dx, a40mx, a42mx, and a54sx) when you see this variable. Compiled VHDL libraries must begin with an alpha character.

Designer Series Manuals

The Designer Series software includes printed and on-line manuals. The on-line manuals are in PDF format on the CD-ROM in the "/doc" directory. These manuals are also installed onto your system when you

install the Designer software. To view the on-line manuals, you must have Adobe® Acrobat Reader® installed. Actel provides Reader on the Designer Series CD-ROM.

The Designer Series includes the following manuals, which provide additional information about designing Actel FPGAs:

Designing with Actel. This manual describes the design flow and user interface for the Actel Designer Series software, including information about using the ACTgen Macro Builder and ACTmap VHDL Synthesis software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

ACTmap VHDL Synthesis Methodology Guide. This guide contains information, optimization techniques, and procedures to assist designers in the design of Actel devices using ACTmap VHDL.

Silicon Expert User's Guide. This guide contains information and procedures to assist designers in the use of Actel's Silicon Expert tool.

Cadence® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

MOTIVE™ Static Timing Analysis Interface Guide. This guide contains information and procedures to assist designers in the use of the MOTIVE software to perform static timing analysis on Actel designs.

Synopsys® Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information and procedures to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Viewlogic Powerview® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Powerview CAE software and the Designer Series software.

Viewlogic Workview Office Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Workview Office CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

*Verilog® Simulation Guid*e. This guide contains information and procedures to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Silicon Explorer Quick Start. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Designer Series Development System Conversion Guide UNIX® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for UNIX to be compatible with later versions of Designer Series.

Designer Series Development System Conversion Guide Windows Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for Windows to be compatible with later versions of Designer Series.

FPGA Data Book and Design Guide. This guide contains detailed specifications on Actel device families. Information such as propagation delays, device package pinout, derating factors, and power calculations are found in this guide.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

On-Line Help

The Designer Series software comes with on-line help. On-line help specific to each software tool is available in Designer, ACTgen, ACTmap, Silicon Expert, and APSW.

1

Setup

This chapter contains information about setting up Workview Office to create Actel designs. This includes information about accessing the Actel and migration libraries, setting up Workview Office to interface with the Designer Series software, and setting up Actel projects in Workview Office. Refer to the Viewlogic documentation for additional information about setting up Workview Office.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R3-1998 or later and Viewlogic Workview Office. For specific information about which versions are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

Actel Libraries

The Actel libraries contain models for each Actel macro in all Actel families for use in Viewlogic. The Actel libraries are sufficient for most cases. Refer to “Migration Libraries” below for exceptions to using the Actel libraries.

Migration Libraries

In addition to the Actel libraries, Actel provides a set of migration libraries. These libraries contain macros that were supported in earlier versions of the Designer Series software and macros that may be needed to retarget designs from a different Actel family. If you are upgrading from a previous version of Designer and you have existing Actel designs, you must use the migration libraries. Actel does not recommend using the migration libraries on new designs.

The Workview Office software uses a “libs.lst” file to access the Actel libraries. A “migrate.lst” file is installed in the “c:\actel\lib\wv” directory when the Designer Series software is installed. You must use this “migrate.lst” file as your “libs.lst” file to properly access the migration libraries.

To access the migration libraries:

1. **(Optional) Create a backup copy of the “libs.lst” in the “c:\wvoffice\standard” directory.**
2. **Delete the “libs.lst” file in the “c:\wvoffice\standard” directory.**
3. **Copy the “migrate.lst” file in the “c:\actel\lib\wv” directory to the “c:\wvoffice\standard” directory.**
4. **Rename the “migrate.lst” file as the “libs.lst” file in the “c:\wvoffice\standard” directory.**

User Setup

Before creating designs, there are some one-time procedures to perform so that the Workview Office and Designer Series software can interface properly. This section describes those procedures.

Actel EDIF Command

To automatically generate an Actel compatible EDIF netlist, add a custom command to the Tools menu in ViewDraw. Once added, this command appears as the Actel EDIF command. The following steps describe the procedure.

1. **Invoke ViewDraw.** If you have not already set up a project, the Project Manager Wizard dialog box is displayed. You must set up an Actel project for ViewDraw to open. Go to “Project Setup” on page 5 for the procedure.
2. **Open the Customize Tools Menu dialog box.** Choose the Customize command from the Tools menu.

3. **Add the Actel EDIF command.** Click the User Menu radio button. In the Menu Text box type “Actel EDIF.” In the Command box type or use the Browse button to select: “c:\wvoffice\edifneto.exe.” In the Arguments box type “-L hard $BLOCKNAME.” Click OK. Figure 1-1 shows the configured Customize Tools Menu dialog box.

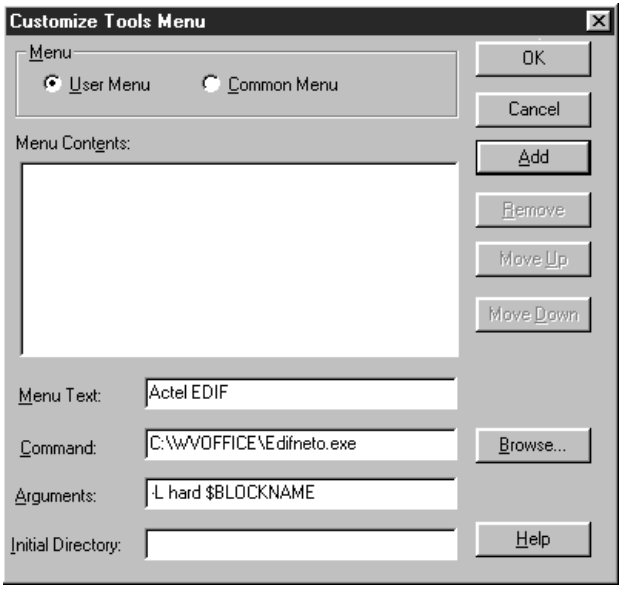

Figure 1-1. Customize Tools Menu Dialog Box

Compiling Actel VITAL Libraries

Before simulating VHDL netlists that reference Actel macros in Speedwave, you must compile Actel VITAL libraries. The following procedures describe the process.

1. **Create a directory called “swave” in the “c:\actel\lib\vtl\95” directory.**

2. **Set your project directory.** Invoke Project Manager and click the New button. Enter “swave” in the Project Name box and “c:\actel\lib\vtl\95\swave” in the Project Directory box. Click the Next button three times, then click the Finish button to complete the process. Do not set your library search order.

3. **Save your project and exit Project Manager.**
4. **Invoke SpeedWave.**
5. **Open the HDL Library Manager window.** Choose the Analyze VHDL Design command from the File menu. Click Cancel in the Welcome dialog box. The HDL Manager window is displayed.
6. **Create a <vhd_fam> library.** Choose the Create command from the File menu. Specify "c:\actel\lib\vtl\95\swave" in the Library Path box and <vhd_fam> in the Symbolic Name box. Click OK.
7. **Add system libraries to search order.** Make sure that the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under the VHDL System Libraries section in the VHDL View window.
8. **Add the Actel VITAL library to the <vhd_fam> library.** Choose the Add Source Files command from the Library menu. Select the <act_fam>.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.
9. **Compile the Actel VITAL library.** Select the <act_fam>.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.
10. **(Optional) Add the Actel VITAL Migration library to the <vhd_fam> library.** Select the <act_fam>_mig.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.
11. **(Optional) Compile the Actel VITAL Migration library.** Select the <act_fam>_mig.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.

Project Setup

You must set up an Actel project in the Viewlogic Project Manager for each Actel design before creating your design in Viewlogic. The following procedures describe the process.

1. **Invoke Project Manager.**
2. **Set up a new project.** Choose the New command from the File menu. The Creating a New Project wizard is displayed.
3. **Set the Project Directory.** Type the full path name of your design directory in the Project Directory box or use the Browse button. Type the name of your project in the Project Name box. Click the Next button.
4. **Locate your project file.** Type the full path name of your project file in the Location of Project File box or use the Browse button. Click the Next button.
5. **Select an Actel FPGA library.** Choose a library in the Configured FPGA Libraries box. Click the icon of the Actel library you want to select, then click Next.
6. **(Optional) Add additional libraries.** Click the Add button and type the full path name of the library you want to add or use the Browse button.
7. **Save the project.** Choose the Save command from the File menu.

Creating a Project Library in SpeedWave

If you use SpeedWave to simulate your designs, you must create a project library in SpeedWave, in addition to creating an Actel project in Project Manager, for each VHDL synthesis-based Actel project. The following procedures describe the process.

1. **Invoke SpeedWave.**
2. **Open the HDL Manager window.** Choose the Analyze VHDL Design command from the File menu. Click Cancel in the Welcome dialog box. The HDL Manager window is displayed.

3. **Setup a project.** Choose the Create command from the Library menu. The Create Library dialog box is displayed. Make sure the path in the Library Path box is correct and already exists. Type "user" in the Symbolic Name box and click OK. Make sure no errors are reported in the Output window.

4. **Verify that the "user" library icon appears under the VHDL User Libraries section in the VHDL View window.**

5. **Add the compiled Actel VITAL library to the Project Libraries.** Choose the Add to Workspace command from the Library menu. The Add Existing Library to Workspace dialog box is displayed. Click the ellipsis box to open the Select Directory dialog box. Browse to the "c:\actel\lib\vtl\95\swave\<vhd_fam>.lib" directory and click OK. Click OK again in the Add Existing Library to Workspace dialog box. If you have not compiled the Actel VITAL library, go to "Compiling Actel VITAL Libraries" on page 3 for the procedure.

   Note: Only add the <vhd_fam>.lib if you have referenced Actel macros in your VHDL netlist.

6. **Add system libraries to the Project Libraries.** Make sure the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under VHDL System Libraries in the VHDL View window. If they are not present you must reinstall SpeedWave making sure to choose the Synopsys IEEE libraries when prompted.

7. **Save the project workspace.** Choose the Save command from the File menu.

2

Actel-Viewlogic Design Flow

This chapter illustrates and describes the design flow for creating Actel designs using the Workview Office and Designer Series software.

Schematic-Based Design Flow Illustrated

Figure 2-1 shows the schematic-based design flow for creating an Actel device using the Workview Office and Designer Series software[1].

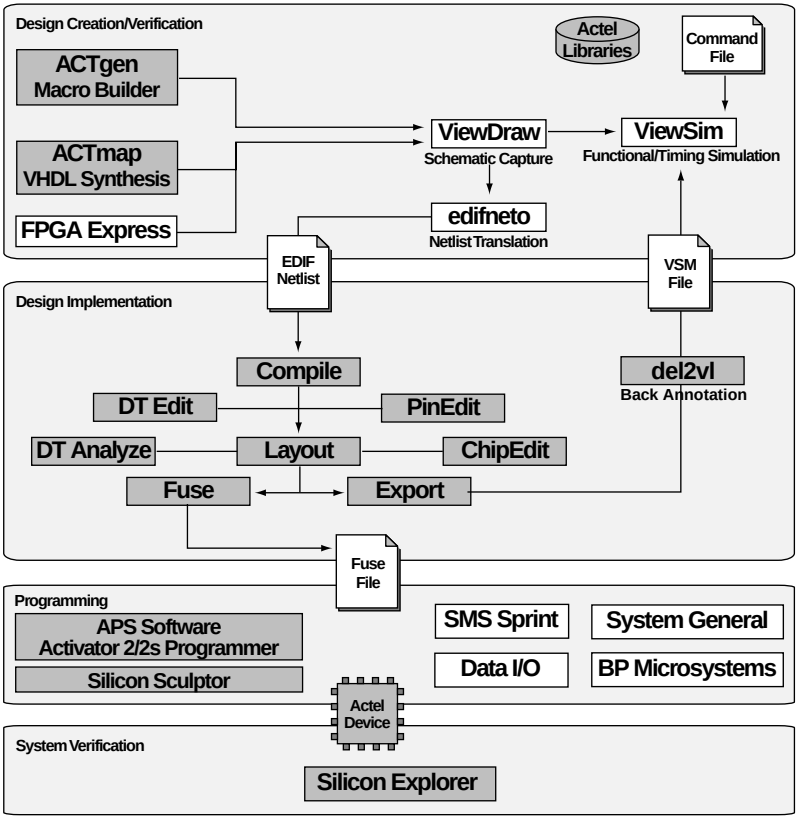

Figure 2-1. Actel-Viewlogic Schematic-Based Design Flow

1. Actel-specific utilities/tools are denoted by the grey boxes in Figure 2-1.

Schematic-Based Design Flow Overview

The Actel-Viewlogic schematic-based design flow has four main steps; design creation/verification, design implementation, programming, and system verification. These steps are described in the following sections.

Design Creation/ Verification

During design creation/verification, a schematic representation of a design is captured using the Viewlogic ViewDraw software. After design capture, a pre-layout (functional) simulation can be performed with the Viewlogic ViewSim software. Finally, an EDIF netlist is generated for use in Designer.

Schematic Capture

Enter your schematic in ViewDraw. Refer to chapter 3, "Actel-Viewlogic Design Considerations" on page 15 and the Viewlogic documentation for information about using ViewDraw.

Functional Simulation

Perform a functional simulation of your design using ViewSim before generating an EDIF netlist for place and route. Functional simulation verifies that the logic of the design is correct. Unit delays are used for all gates during functional simulation. Refer to "Functional Simulation" on page 23 and the Viewlogic documentation for information about performing functional simulation.

EDIF Netlist Generation

After you have captured and verified your design, you must generate an EDIF netlist for place and route in Designer. Refer to "Generating an EDIF Netlist" on page 19 for information about generating an EDIF netlist.

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, static timing analysis can be performed on a design in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with the Viewlogic ViewSim software.

Place and Route

Use Designer to place and route your design. Make sure you specify VIEWLOGIC as the Edif Flavor and Generic as the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designing with Actel* manual for information about using Designer.

Static Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis on your design. Refer to the *Designing with Actel* manual for information about using DT Analyze.

Timing Simulation

Perform a timing simulation of your design using ViewSim after placing and routing it in Designer. Timing simulation requires information extracted and back annotated from Designer. Refer to "Timing Simulation" on page 24 and the Viewlogic documentation for information about performing timing simulation.

Programming

Program a device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designing with Actel* manual and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information about using the Silicon Explorer.

VHDL Synthesis-Based Design Flow Illustrated

Figure 2-2 shows the VHDL synthesis-based design flow for an Actel device using the Workview Office and Designer Series software[1].

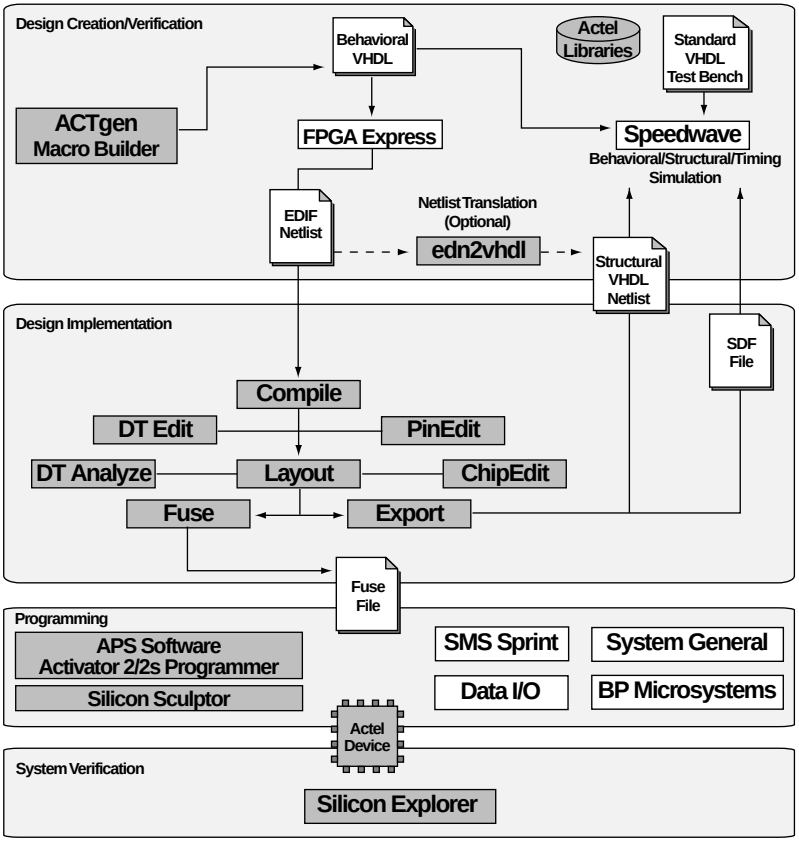

Figure 2-2. Actel-Viewlogic VHDL Synthesis-Based Design Flow

1. *Actel-specific utilities/tools are denoted by the grey boxes in Figure 2-2.*

VHDL Synthesis-Based Design Flow Overview

The Actel-Viewlogic VHDL synthesis-based design flow has four main steps; design creation/verification, design implementation, programming, and system verification. Two verification tools are described, SpeedWave and ViewSim. SpeedWave should be used if it is available. It is a VHDL simulator that allows you to perform behavioral, structural, and timing simulation. It also allows stimulus to be written in VHDL. If SpeedWave is not available, structural and timing simulation may be done with ViewSim. These steps are described in the following sections.

Design Creation/ Verification

During design creation/verification, a design is captured in an RTL-level (behavioral) VHDL source file. After capturing the design, a behavioral simulation of the VHDL file may be performed with SpeedWave to verify that the VHDL code is correct. The code is then synthesized into a structural EDIF netlist using FPGA Express. After synthesis, a structural simulation of the design can be performed with SpeedWave or ViewSim. The EDIF netlist is imported into Designer and a timing simulation is performed using SpeedWave or ViewSim.

VHDL Design Source Entry

Enter your design source using a text editor or a context-sensitive VHDL editor. Your VHDL design source can contain RTL-level constructs as well as instantiations of structural elements, such as ACTgen macros.

Behavioral Simulation

If SpeedWave is available, perform a behavioral simulation of your design before synthesis. Behavioral simulation verifies the functionality of your VHDL code. Typically, unit delays are used and a standard VHDL test bench can be used to drive simulation. Refer to “Behavioral Simulation” on page 27 and the Viewlogic documentation for information about performing behavioral simulation.

Synthesis

Synthesize your design using FPGA Express. This transforms the behavioral VHDL file into a gate-level EDIF netlist, optimizing the design for a target technology.

Structural VHDL Netlist Generation

If SpeedWave is used for structural and timing simulation, generate a structural VHDL netlist from your EDIF netlist by either exporting it from Designer or by using the Actel "edn2vhdl" program. Refer to "Generating a Structural VHDL Netlist" on page 20 for information about generating a structural netlist.

Structural Simulation

Perform a structural simulation of your design before placing and routing it. Structural simulation verifies the functionality of your post-synthesis structural netlist. Unit delays are used for each gate. Refer to "Functional Simulation" on page 23 if using ViewSim or "Structural Simulation" on page 28 if using Speedwave. Also refer to the Viewlogic documentation for information about performing structural simulation.

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, static timing analysis can be performed on a design in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with the Viewlogic SpeedWave software.

Place and Route

Use Designer to place and route your design. Make sure to use GENERIC for the Edif flavor and VHDL for the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designing with Actel* manual for information about using Designer.

Static Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis of your design. Refer to the *Designing with Actel* manual for information about using DT Analyze.

Timing Simulation

Perform a timing simulation of your design after placing and routing it. Timing simulation uses information extracted from Designer, which overrides unit delays in the Actel VHDL. Refer to "Timing Simulation" on page 24 if using Viewsim or "Timing Simulation" on page 29 if using SpeedWave. Also refer to the Viewlogic documentation for information about performing timing simulation.

Programming

Program a device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designing with Actel* manual and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information about using the Silicon Explorer.

3

Actel-Viewlogic Design Considerations

This chapter contains information and procedures to assist you in creating Actel designs with the Viewlogic Workview Office software. This includes naming conventions, information about adding pins to a schematic, and about generating top-level symbols. Also included is information about using buried I/Os, adding power and ground, and how sheets and symbols are treated. Other sections include how to assign pins in a schematic and how to add ACTgen, ACTmap and FPGA Express blocks to a design. Finally, procedures for generating EDIF and structural VHDL netlists are given.

Naming Conventions

Top level blocks in ViewDraw and FPGA Express must have a design name that follows the DOS file naming convention (i.e. 8.3 naming convention). The Actel back annotation program can only accept file names that follow this convention.

Use only alphanumeric and underscore "_" characters for schematic net and instance names. Do not use asterisks, forward and backward slashes, spaces, or periods.

Adding Pins to the Schematic

Add pins to the top-level schematic of the design by using the I/O buffer macros with a dangling net attached to the pad, as shown in Figure 3-1. The label on the dangling net becomes the I/O pin name.

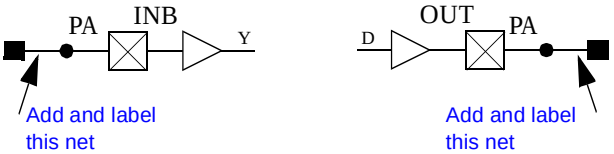

Figure 3-1. Adding Pins to a design

Generating a Top-Level Symbol

When generating a top-level symbol, ViewGen looks for an In or Out port. The convention is illustrated in Figure 3-2. ViewGen does not generate symbols for schematics without IN/OUT ports. The IN/OUT ports are found in the “c:\actel \lib\wv\asicbin” directory.

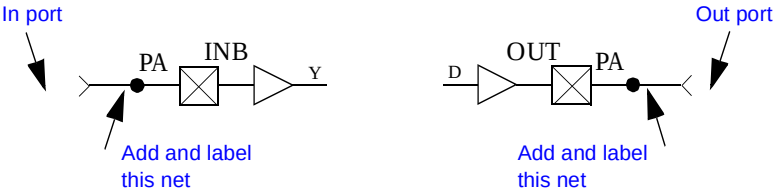

Figure 3-2. Input/Output Ports

Buried I/O

I/O macros can be buried in the design hierarchy.

Adding Power and Ground

To add power or ground signals in the schematic, use the Actel VCC or GND symbols. You can also label the nets as VDD or GND.

Sheets and Symbols

A multiple-page design is composed of more than one schematic file or <design.n> file in the schematic directory. For a multiple-page design, each sheet is treated as a part of a top-level schematic and is not considered a hierarchy level.

Assigning Pins in a Schematic

Nets in your schematic that have the "PIN" attribute assigned to them in ViewDraw are automatically assigned to that pin during design implementation in Designer.

To assign the "PIN" attribute to a net:

1. **Double-click the net to assign pin information.** The Net Properties dialog box is displayed.
2. **Select the Attributes Tab.**
3. **Assign the "PIN" attribute to the net.** Type "PIN" in the Name box and the pin number to be assigned in the Value box. Click OK.

Note: This procedure assigns the pin name to the signal net in the netlist. If you use this method to fix pins, and you change your pin assignments in PinEdit, you will not be able to back annotate. PinEdit does not change netlist information.

Adding ACTgen Macros

The ACTgen Macro Builder can automatically generate symbols that can be added to your schematic. The following steps describe the procedure.

1. **Invoke ACTgen.**
2. **Select the family, macro type, and macro options.**
3. **Generate your macro as a Viewlogic symbol.** Make sure that you specify Viewlogic as the Netlist/CAE Formats in the Generate Macro dialog box.
4. **Add the macro as a component in the schematic.** Refer to the Viewlogic documentation for information about adding components to a schematic.

Refer to the *Designing With Actel* manual or the ACTgen on-line help for additional information about using ACTgen.

Adding ACTmap Blocks

The ACTmap VHDL Synthesis tool can generate symbols from VHDL blocks that can be added to your schematic. The following steps describe the procedure.

1. **Invoke ACTmap.**
2. **Open the ACTmap VHDL Compiler window.** Select the VHDL Compiler command from the File menu.
3. **Compile your VHDL block and generate an EDIF netlist.** Type the name of your design in the Source Design box or use the Browse button. Specify Block as the Mode, select options, and click the Run button. The Main window displays a report of the compilation process.
4. **Translate the EDIF netlist to a Viewlogic symbol.** Click the Translate button in the ACTmap VHDL Compile window. Type the name of your VHDL block in the Source Design box or use the Browse button. Specify Viewlogic as the Output Format, select options, and click the Run button.
5. **Set VL options.** In the Set VL dialog box, make sure the symbol check box is marked. The other check boxes are optional. Click OK.
6. **Add the block as a component in the schematic.** Refer to the Viewlogic documentation for information about adding components to a schematic.

   Note: ACTmap supports hierarchical EDIF output, but the symbol generator only creates the top level symbol.

Refer to the *Designing with Actel* manual, the *ACTmap VHDL Synthesis Methodology Guide*, or the ACTmap on-line help for additional information about using ACTmap.

Adding FPGA Express Blocks

FPGA Express can generate blocks that can be added to your ViewDraw schematic. The following steps describe the procedure.

1. **Invoke FPGA Express.**
2. **Create a new project or open an existing one.** Add your VHDL source file(s) to the project.
3. **Create an implementation.** In the Create Implementation form, select “Do not insert I/O pads.”
4. **Export the Netlist.** In the Export form, select “%s<%d:%d>” for Bus Style and NONE for the Simulation Output Format.
5. **Save the Project and exit FPGA Express.**
6. **Translate the EDIF file into ViewDraw’s wir format.** Invoke the EDIF Interfaces program and select the EDIF Netlist Reader tab. Specify the EDIF file created by FPGA Express as the Input and your Viewlogic project directory as your Output Dir.
7. **Invoke ViewGen to generate a symbol.** Specify the wir file generated by the EDIF Netlist Reader as the input. Select “Generate the top level symbol” and optionally, “Generate schematic.”
8. **Add the symbol to your ViewDraw schematic.** Refer to the Viewlogic documentation for information about adding symbols to a schematic.

Refer to the FPGA Express and other WorkView Office on-line help for additional information.

Generating an EDIF Netlist

The EDIF netlist is used for place and route in Designer. This section describes the procedures for generating an EDIF netlist for your design.

To generate an EDIF netlist from a schematic-based design:

Select the Actel EDIF command from the Tools menu of ViewDraw. If you have not added the Actel EDIF command to the tools menu in ViewDraw, go to “Actel EDIF Command” on page 2 for the procedure.

To generate an EDIF netlist from a synthesis-based design:

FPGA Express creates an EDIF file that can be imported directly into Designer. No special procedure is required.

Generating a Structural VHDL Netlist

You can generate a structural VHDL netlist for SpeedWave simulation from your EDIF netlist by either exporting it from Designer or by using the “edn2vhdl” program. The structural VHDL netlist generated by Designer and the “edn2vhdl” use std_logic for all ports. The bus ports are in the same bit order as they appear in the EDIF netlist.

To generate a structural VHDL netlist using Designer:

1. **Invoke Designer.**
2. **Import the EDIF netlist.** Select the Import Netlist File command from the File menu. The Import Netlist dialog box is displayed. Specify EDIF as the Netlist Type, GENERIC (or VIEWLOGIC if you are using a Viewlogic synthesis tool) as the Edif Flavor, and VHDL in the Naming Style. Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK.
3. **Export the structural VHDL netlist.** Select the Export command from the File menu. The Export dialog box is displayed. Specify Netlist File as the File Type and VHDL as the Format. Click OK.

To generate a structural VHDL netlist using edn2vhdl:

1. **Open a DOS window.**
2. **Change to the directory that contains the EDIF netlist.**
3. **Translate the EDIF netlist to a structural VHDL Netlist.** Type the following command at the prompt:

```
edn2vhdl fam:<act_fam> <design_name>
```

Using FPGA Express with SpeedWave

When using FPGA Express with SpeedWave, you do not need to use ViewDraw, ViewSim, ViewGen, or Viewlogic EDIF interfaces. You use three point tools: SpeedWave, FPGA Express, and Designer.

1. **Perform a behavior simulation in SpeedWave.** After writing your VHDL, simulate and debug it in SpeedWave as described in “Behavioral Simulation” on page 27.
2. **Synthesize your design in FPGA Express.** Create or open an existing FPGA Express project. Add your VHDL source file(s) to the project.

   In the Create Implementation form, be sure that the “Do not insert I/O pads” checkbox is not selected.

   In the Export form, select "%s<%d:%d>" for Bus Style and NONE for the Simulation Output Format.

   An EDIF netlist is exported by FPGA Express.
3. **Perform a structural simulation in SpeedWave.** Translate the EDIF into VHDL as described in “Generating a Structural VHDL Netlist” on page 20. Then perform a structural simulation as described in “Structural Simulation” on page 28.
4. **Place and route your design in Designer.** Export an SDF timing file.
5. **Perform a timing simulation in SpeedWave.** Perform a timing simulation as described in “Timing Simulation” on page 29.

Using FPGA Express with Viewsim

When using FPGA Express with ViewSim, you will not be able to do a behavioral simulation, and you need to import the synthesized design into the ViewDraw/ViewSim environment.

1. **Synthesize your design in FPGA Express.** Create or open an existing FPGA Express project. Add your VHDL source file(s) to the project.

In the Create Implementation form, make sure that the “Do not insert I/O pads” checkbox is not selected.

In the Export form, select “%s<%d:%d>” for Bus Style and NONE for the Simulation Output Format.

An EDIF netlist is exported by FPGA Express.

2. **Import the synthesized EDIF into the ViewDraw/ViewSim environment.** Invoke the EDIF Interfaces program and select the EDIF Netlist Reader tab. Specify the EDIF file created by FPGA Express as the Input and your Viewlogic project directory as your Output Dir.
3. **Perform a functional simulation in ViewSim.** See “Functional Simulation” on page 23 for detailed information.
4. **Place and route your design in Designer.** Export an STF (also known as Generic) timing file.
5. **Perform timing simulation in ViewSim.** See “Timing Simulation” on page 24 for detailed information.

4

Simulation Using ViewSim

This chapter describes the procedures for performing functional and timing simulations of an Actel design using the Viewlogic ViewSim simulation tool.

Functional Simulation

Use the following procedure to perform a functional simulation of an Actel design:

1. **Select your Actel project in the Viewlogic Project Manager.** If you have not created or setup your project, go to “Project Setup” on page 5 for the procedure.
2. **Open the ViewSim Wirelister dialog box.** Invoke ViewVSM, or from ViewDraw choose the Create Digital Netlist command from the Tools menu.
3. **Generate a simulation (.vsm) wirelist.** Type in the design name or use the Browse button. Click OK. A simulation wirelist is generated and the Workview Office Simulation window is displayed.
4. **Simulate the design.** Invoke ViewSim. Type in the design name in the Design Name box and click OK.

Refer to the Viewlogic documentation for additional information about performing simulation with ViewSim.

Timing Simulation

Use the following procedure to perform a timing simulation of an Actel design:

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information on using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a <design_name>.stf file by choosing the GENERIC option from the CAE pull-down menu. Click OK.
3. **Back annotate your delays.** Select the Viewlogic Back annotate icon from the Designer Series group. The Open dialog box is displayed. Select the <design_name>.stf file and click OK to generate the <design_name>.dtb file and the <design_name>.vsm file for use with ViewSim.
4. **Select your Actel project in Project Manager.** If you have not created or setup your project see “Project Setup” on page 5.
5. **Simulate the design.** Invoke ViewSim. Choose the Load Design from the File menu. The Load compiled VSM file dialog box is displayed. Select the <design_name>.vsm file created in step 3 and click OK.

Refer to the Viewlogic documentation for additional information about performing simulation with ViewSim.

Multichip Simulation

System designs are typically divided into functional modules that are implemented by several Actel devices. To check the functionality of the system, all Actel devices must be simulated together. You can use ViewSim and Designer to perform multichip simulation. Use the following procedure to perform a multichip simulation of an Actel design:

Note: Because the viewdraw.ini file uses the same alias for all Actel families, you can only simulate multiple Actel devices of the same family.

1. **Create a top level schematic and instantiate the individual chip designs.** This example, assumes there are three designs with instance names “chip1,” “chip2,” and “chip3.” The name of the top level schematic is “top.” Figure 4-1 depicts the directory structure for this example. Names written in normal text represent file names and those in bold text represent directory names.

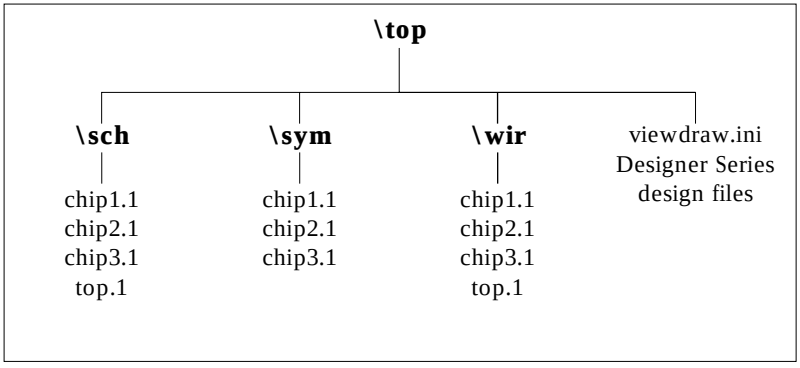

Figure 4-1. Directory Structure for Multichip Simulation

Note: This example only contains single-sheet schematics for each design. Similar procedures apply to multiple-sheet designs.

2. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.

3. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a “chip1.stf” file by choosing the GENERIC option from the CAE pull-down menu. Click OK. Repeat for “chip2.stf” and “chip3.stf.”

4. **Back annotate your delays.** Select the Viewlogic Back annotate icon from the Designer Series group. The Open dialog box is displayed. Select the “chip1.stf” file and click OK to generate the “chip1.dtb” file. Repeat for the “chip2.dtb” and “chip3.dtb” files.

5. **Generate a "top.dtb" file for the top level schematic.** The top level DTB file should include the following lines:

```
.ba
c chip1
a dtb=chip1.dtb
c chip2
a dtb=chip2.dtb
c chip3
a dtb=chip3.dtb
.ab
```

   The "c" line above specifies an instance name, "chip1." If you haven't labeled an instance, you can use the default handle name of an instance, "$1I38" as it appears in your top-level schematic. Also, the individual DTB files should reside in the top level design directory, "top."

6. **Run ViewVSM on "top.dtb."** Reference the "top.dtb" file in the VSM pop-up dialog box. The VSM program processes the DTB files for each chip and creates the "top.vsm" file with back annotated post-layout timing delays.

7. **Simulate "top.vsm."** Invoke ViewSim. Type "top.vsm" in the Design Name box and click OK.

Refer to the Viewlogic documentation for additional information about performing simulation with ViewSim.

5

Simulation Using SpeedWave

This chapter describes the procedures for performing behavioral, structural, and timing simulations of an Actel design using the Viewlogic SpeedWave simulation tool.

Behavioral Simulation

Use the following procedures to perform a behavioral simulation of an Actel design. Refer to the Viewlogic documentation for additional information about performing simulation with SpeedWave:

1. **Select your Actel project in Project Manager.** If you have not created your project, go to “Project Setup” on page 5 for the procedure.
2. **Invoke SpeedWave.**
3. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click the Cancel button in the Welcome dialog box and go to “Creating a Project Library in SpeedWave” on page 5 for the procedure.
4. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select an .hws file and click the Open button in the Open dialog box.
5. **Analyze your behavioral VHDL design files and test bench.** Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Add Source Files command from the Library menu. The Assign Source Files dialog box is displayed. Select the behavioral VHDL and test bench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.
6. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double click “user.lib” and select the

configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.

7. **Simulate your design.** Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

Structural Simulation

Use the following procedures to perform a structural simulation of an Actel design. Refer to the Viewlogic documentation for additional information about performing simulation with SpeedWave.

1. **Synthesize your design.** Refer to the documentation included with your synthesis tool for information about synthesis.
2. **Select your Actel project in Project Manager.** If you have not created your project, go to “Project Setup” on page 5 for the procedure.
3. **Invoke SpeedWave.**
4. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click the Cancel button in the Welcome dialog box and go to “Creating a Project Library in SpeedWave” on page 5 for the procedure.
5. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select an .hws file and click the Open button in the Open dialog box.
6. **Analyze your structural VHDL netlist and test bench.** If you have not already generated a structural VHDL netlist, go to “Generating a Structural VHDL Netlist” on page 20 for the procedure. Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Add Source Files command from the Library menu. The Assign Source Files dialog box is displayed. Select the structural VHDL netlist and test bench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the

Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.

7. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.
8. **Simulate your design.** Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

Timing Simulation

Use the following procedures to perform a timing simulation of an Actel design. Refer to the Viewlogic documentation for additional information about performing simulation with SpeedWave.

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design from Designer.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog is displayed. Create a <design_name>.sdf file by choosing the SDF option from the CAE pull-down menu. Click OK.
3. **Select your Actel project in Project Manager.** If you have not created a project, go to "Project Setup" on page 5 for the procedure.
4. **Invoke SpeedWave.**
5. **Open the HDL Manager dialog box.** Choose the Analyze VHDL Design command from the File menu. If the HDL Manager wizard appears, you must create a project library before continuing. Click the Cancel button in the Welcome dialog box and go to "Creating a Project Library in SpeedWave" on page 5 for the procedure.

6. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select an .hws file and click the Open button in the Open dialog box.

7. **(Optional) Analyze your VHDL design files and test bench.** Skip this step if you are using the same structural VHDL netlist and test bench you analyzed for structural simulation. Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Add Source Files command from the Library menu. The Assign Source Files dialog box is displayed. Select the structural VHDL netlist and test bench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your test bench.

8. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double click “user.lib” and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.

9. **Import the timing information for your design.** Click the VITAL Timing index tab. Click the Perform SDF Back Annotation check box and click OK. The Setup SDF Back Annotation dialog box is displayed. Type the name of your <design_name>.sdf in the SDF File box or use the Browse button.

10. **Add Scope options.** In the Scope window, fill in the name of the instance in the test bench you want to back annotate (e.g. “/uut”). Select the Delay Mode you want use (Minimum, Typical, or Maximum). Click the Add button and verify that Scope, File, and Timing settings are correct in the main window. Use the Change and Remove buttons to make any corrections.

11. **Back annotate your design.** Click OK.

12. **Simulate your design**. Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a fax back service, a Web and FTP site, electronic mail, and worldwide sales offices. This appendix contains information about using these services and contacting Actel for service and support.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel Toll-Free Line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4474.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4474 or +44 (0) 1256 305600.
From Japan, call (408) 522-4252.
From the rest of the world, call (408) 522-4252.
Fax, from anywhere in the world (408) 522-8044.

Customer Applications Center

The Customer Applications Center is staffed by applications engineers who can answer your hardware, software, and design questions.

All calls are answered by our Technical Message Center. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 a.m. to 5 p.m., Pacific Standard Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305600.

Guru Automated Technical Support

Guru is a Web based automated technical support system accessible through the Actel home page (http://www.actel.com). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations and links to other resources on the Actel Web site. Guru is available 24 hours a day, seven days a week.

Action Facts

Action Facts is a 24-hour fax-back service that allows you to have technical literature faxed directly to you. The literature includes current applications notes, device diagrams, radiation testing reports, CAE-related documents, training release schedules, and much more.

To receive your free copy of the catalog or any of our literature, contact us at (800) 262-1062 or (408) 739-1588.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is http://www.actel.com. You are welcome to share the resources we have provided on the net.

Be sure to visit the "Actel User Area" on our Web site, which contains information regarding: products, technical services, current manuals, and release notes.

FTP Site

Actel has an anonymous FTP site located at ftp://ftp.actel.com. You can directly obtain library updates, software patches, design files, and data sheets.

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. The e-mail account is monitored several times per day.

The technical support e-mail address is tech@actel.com.

Worldwide Sales Offices

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
USA
Toll Free: 888.99.ACTEL
Tel: 408.739.1010
Fax: 408.739.1540

California (North)
Tel: 408.328.2200
Fax: 408.328.2358

California (South)
Tel: 714.727.0470
Fax: 714.727.0476

Georgia
Tel: 770.844.4495
Fax: 770.844.1395

Illinois
Tel: 847.259.1501
Fax: 847.259.1572

Massachusetts
Tel: 508.635.0010
Fax: 508.635.9510

Texas
Tel: 972.235.8944
Fax: 972.235.9659

Actel Europe, Ltd.
Daneshill House, Lutyens Close
Basingstoke,
Hampshire RG24 8AG
United Kingdom
Tel: +44 (0)1256.305600
Fax: +44 (0)1256.355420

France
Tel: +33 (0)1.40.83.11.00
Fax: +33 (0)1.40.94.11.04

Germany
Tel: +49 (0)8165.9584.0
Fax: +49 (0)8165.9584.10

Italy
Tel: +39 (0)2.38.09.32.59
Fax: +39 (0)2.38.09.32.60

Actel Asia-Pacific
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Tel: +81 (0)3.3445.7671
Fax: +81 (0)3.3445.7668

Korea
Tel: +82 (0)2.555.7425
Fax: +82 (0)2.555.5779

Taipei, Taiwan R.O.C.
Tel: +886 (0)2.698.2448
ext. 104
Fax: +886 (0)2.698.2548

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