

54SX Family FPGAs

Leading Edge Performance

- 320 MHz Internal Performance
- 3.7 ns Clock-to-Out (Pin-to-Pin)
- 0.1 ns Input Set-Up
- 0.25 ns Clock Skew

Specifications

- 8,000 to 32,000 Available Logic Gates
- Up to 246 User-Programmable I/O
- 1,980 Flip-Flops
- 0.35 μ CMOS

Features

- 66 MHz PCI
- CPLD and FPGA Integration
- Single Chip Solution

- 100% Resource Utilization with 100% Pin Locking
- 3.3V Operation with 5.0V Input Tolerance
- Very Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique, In-System Diagnostic and Debug capability with Silicon Explorer
- JTAG Boundary Scan Testing in Compliance with IEEE Standard 1149.1
- Actel Designer Series Design Tools, Supported by Cadence, Exemplar, IST, Mentor Graphics, Model Tech, Synopsys, Synplicity, and Viewlogic Design Entry and Simulation Tools
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

SX Product Profile

	A54SX08	A54SX16	A54SX16P	A54SX32
Gate Capacity	8,000	16,000	16,000	32,000
Logic Modules	768	1,452	1,452	2,880
Combinatorial Cells	512	924	924	1,800
Register Cells (Dedicated Flip-Flops)	256	528	528	1,080
Maximum Flip-Flops	512	990	990	1,980
User I/Os (Maximum)	129	177	177	246
Clocks	3	3	3	3
JTAG	Yes	Yes	Yes	Yes
PCI	—	—	Yes	—
Clock-to-Out	3.7 ns	3.9 ns	4.4 ns	4.6 ns
Input Set-Up (External)	0.8 ns	0.5 ns	0.5 ns	0.1 ns
Speed Grades	Std, -1, -2, -3	Std, -1, -2, -3	Std, -1, -2, -3	Std, -1, -2, -3
Temperature Grades	C, I, M	C, I, M	C, I, M	C, I, M
Packages (by pin count)				
PQFP	208	208	208	208
VQFP	100	100	100	—
TQFP	144, 176	176	144, 176	144, 176
PBGA	—	—	—	313, 329

General Description

The New SX Family of FPGAs

Actel's SX Family of FPGAs features a revolutionary new sea-of-modules architecture that delivers next-generation device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further speed time-to-market for performance-intensive applications.

Fast and Flexible New Architecture

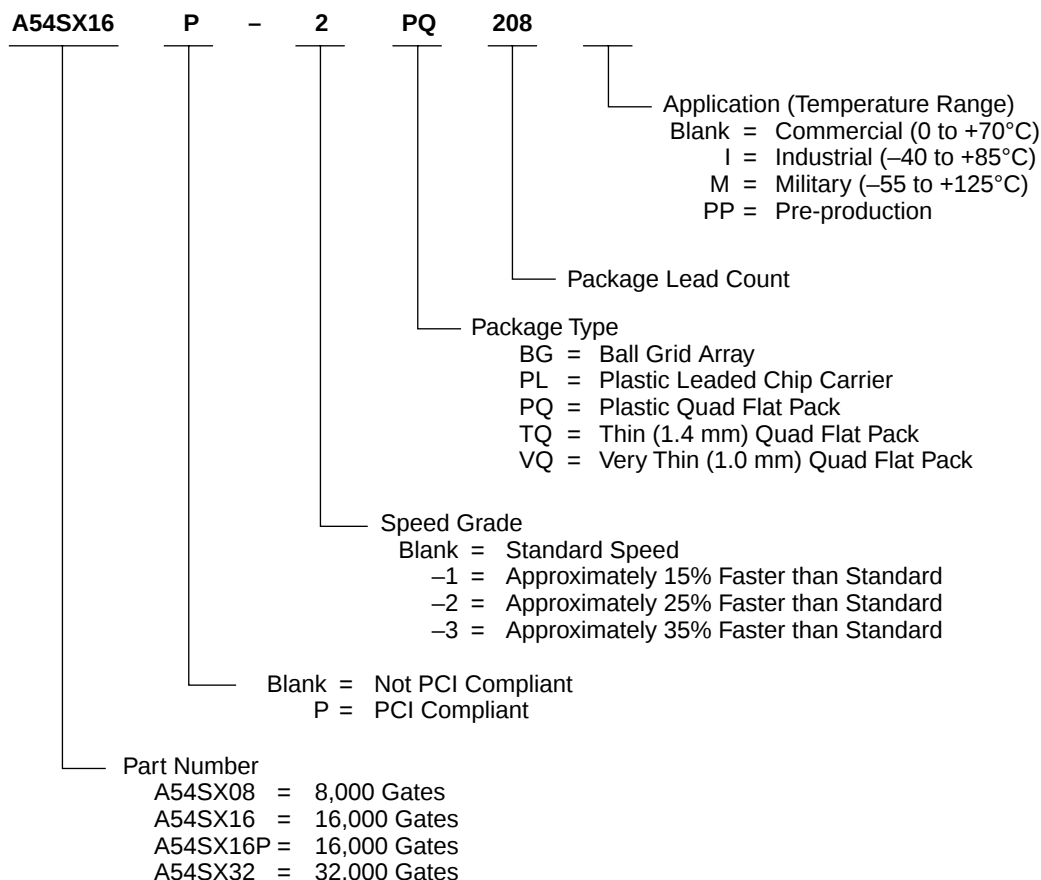
Actel's SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. Optimal use of the silicon is made by locating the routing and interconnect resources in the metal layers above the logic modules, enabling the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules") which reduces the distance signals have to travel between logic modules.

To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local

routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (typically 90% of connections use only three antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100% pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with a minimum of effort.

Further complementing the SX's flexible routing structure, a hard-wired, constantly-loaded clock network has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SX devices have easy-to-use I/O cells which do not require HDL instantiation, facilitating design re-use and reducing design and debugging time.

Ordering Information



Product Plan

	Speed Grade*				Application		
	Std	-1	-2	-3	C	I†	M*
A54SX08 Device							
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✓	✓	P	P	✓	✓	P
144-Pin Thin Quad Flat Pack (TQFP)	✓	✓	P	P	✓	✓	P
176-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	P	P
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	P	P	✓	✓	P
A54SX16 Device							
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✓	✓	P	P	✓	✓	P
176-Pin Thin Quad Flat Pack (TQFP)	✓	✓	P	P	✓	✓	P
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	P	P	✓	✓	P
A54SX16P Device							
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✓	✓	P	P	✓	✓	P
144-Pin Thin Quad Flat Pack (TQFP)	✓	✓	P	P	✓	✓	P
176-Pin Thin Quad Flat Pack (TQFP)	✓	✓	P	P	✓	✓	P
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	P	P	✓	✓	P
A54SX32 Device							
144-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	P	P
176-Pin Thin Quad Flat Pack (TQFP)	✓	✓	P	P	✓	✓	P
208-Pin Plastic Quad Flat Pack (PQFP)	✓	✓	P	P	✓	✓	P
313-Pin Plastic Ball Grid Array (PBGA)	✓	✓	P	P	✓	✓	P
329-Pin Plastic Ball Grid Array (PBGA)	✓	✓	P	P	P	P	P

Consult your local Actel sales representative for product availability.

Applications: C = Commercial Availability: ✓ = Available
 I = Industrial P = Planned
 M = Military — = Not Planned

*Speed Grade: -1 = Approx. 15% Faster than Standard
 -2 = Approx. 25% Faster than Standard
 -3 = Approx. 35% Faster than Standard

† Only Std, -1, -2 Speed Grade

• Only Std, -1 Speed Grade

Plastic Device Resources

Device	User I/Os					
	VQFP 100-Pin	PQFP 208-Pin	TQFP 144-Pin	TQFP 176-Pin	PBGA 313-Pin	PBGA 329-Pin
A54SX08	78	129	112	129	—	—
A54SX16	78	172	—	144	—	—
A54SX16P	78	172	112	144	—	—
A54SX32	—	171	112	144	246	246

Package Definitions (Consult your local Actel sales representative for product availability.)

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack,
 PBGA = Plastic Ball Grid Array

Pin Description

CLKA Clock A (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

CLKB Clock B (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

TCK Test Clock (Input)

Test clock input for diagnostic probe and device programming. In flexible mode (refer to the JTAG pins functionality table), TCK becomes active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the “logic reset” state.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tri-stated by the Designer Series software.

TMS Test Mode Select (Input)

The TMS pin controls the use of JTAG pins (TCK, TDI, TDO). In flexible mode (refer to the JTAG pins functionality table), when the TMS pin is set LOW, the TCK, TDI, and TDO pins are JTAG pins. Once the JTAG pins are in JTAG mode they will remain in JTAG mode until the internal JTAG state machine reaches the “logic reset” state. At this point the JTAG pins will be released and will function as regular I/O pins. The “logic reset” state is reached 5 TCK cycles after the TMS pin is

set HIGH. In dedicated JTAG mode, TMS functions as specified in the IEEE 499.1 JTAG Specifications. JTAG operation is further described on page 10.

NC No Connection

This pin is not connected to circuitry within the device.

PRA ActionProbe A (Output)

The ActionProbe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the ActionProbe B pin to allow real-time diagnostic output of any signal path within the device. The ActionProbe A pin can be used as a user-defined I/O when debugging has been completed.

PRB ActionProbe B (Output)

The ActionProbe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the ActionProbe A pin to allow real-time diagnostic output of any signal path within the device. The ActionProbe B pin can be used as a user-defined I/O when debugging has been completed.

TDI Test Data Input (Input)

Serial input for JTAG and diagnostic probe. In flexible mode, (refer to the JTAG pins functionality table), TDI is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the “logic reset” state.

TDO Test Data Output (output)

Serial output for JTAG. In flexible mode (Refer to the JTAG pins functionality table), TDO is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the “logic reset” state.

V_{CCI} Supply Voltage

Supply voltage for I/Os.

V_{CCA} Supply Voltage

Supply voltage for Array.

V_{CCR} Supply Voltage

Supply voltage for input tolerance (required for internal biasing).

Table 1 • Supply Voltages

	V _{CCA}	V _{CCI}	V _{CCR}	Input Tolerance	Output Drive
A54SX08	3.3V	3.3V	5.0V	3.3V	3.3V
A54SX16	3.3V	3.3V	5.0V	5.0V	3.3V
A54SX32	3.3V	3.3V	5.0V	5.0V	3.3V
A54SX16P	3.3V	3.3V	3.3V	3.3V	3.3V
	3.3V	3.3V	5.0V	5.0V	3.3V
	3.3V	5.0V	5.0V	5.0V	5.0V

SX Family Architecture

The SX Family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

Actel's new SX Family provides much more efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (see Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse

interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX Family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible as it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

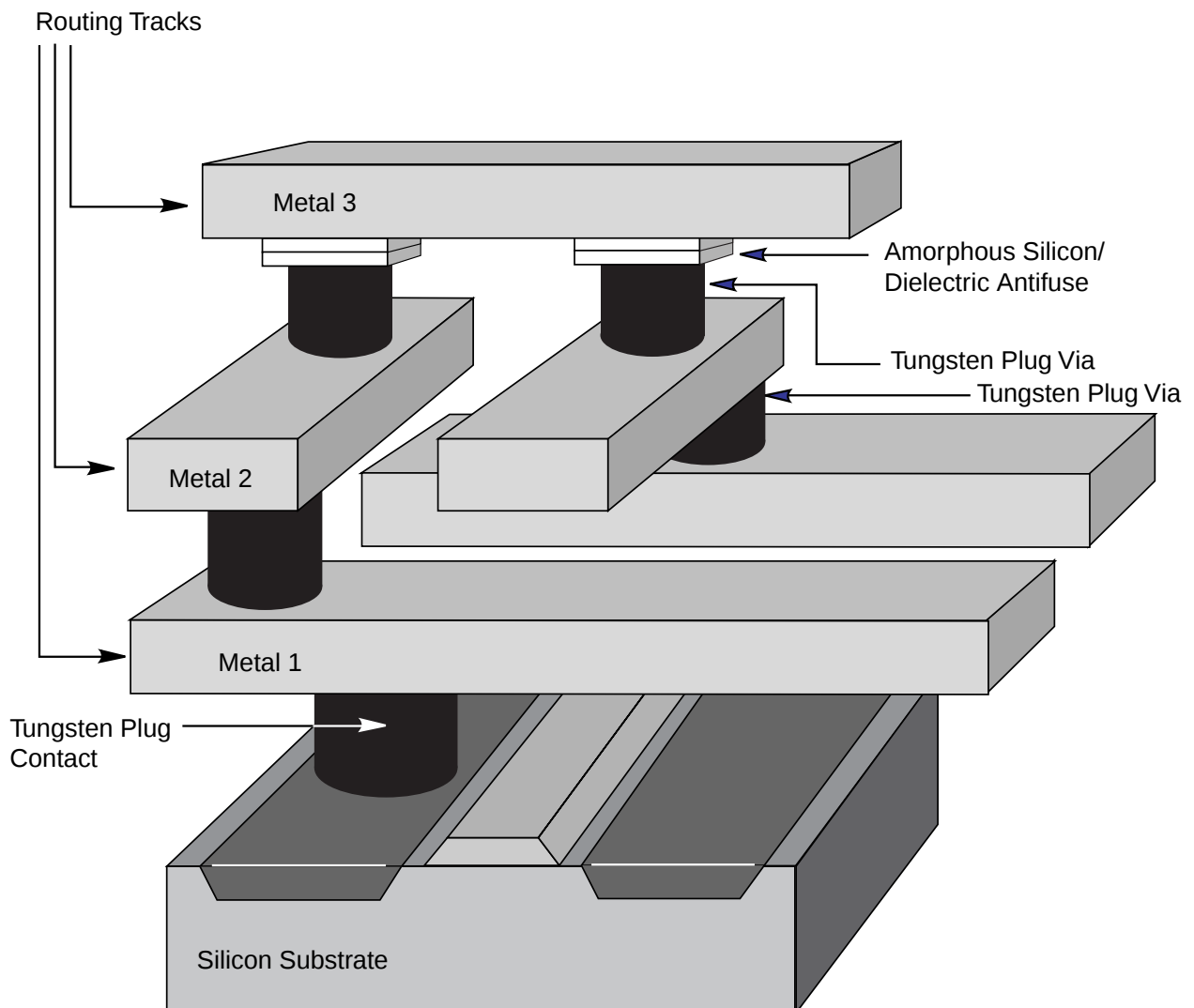


Figure 1 • SX Family Interconnect Elements

Logic Module Design

The SX Family architecture has been called a “sea-of-modules” architecture because the entire floor of the device is covered with a grid of logic modules with virtually no

chip area lost to interconnect elements or routing (see Figure 2). Actel provides two types of logic modules, the R-cell and the C-cell.

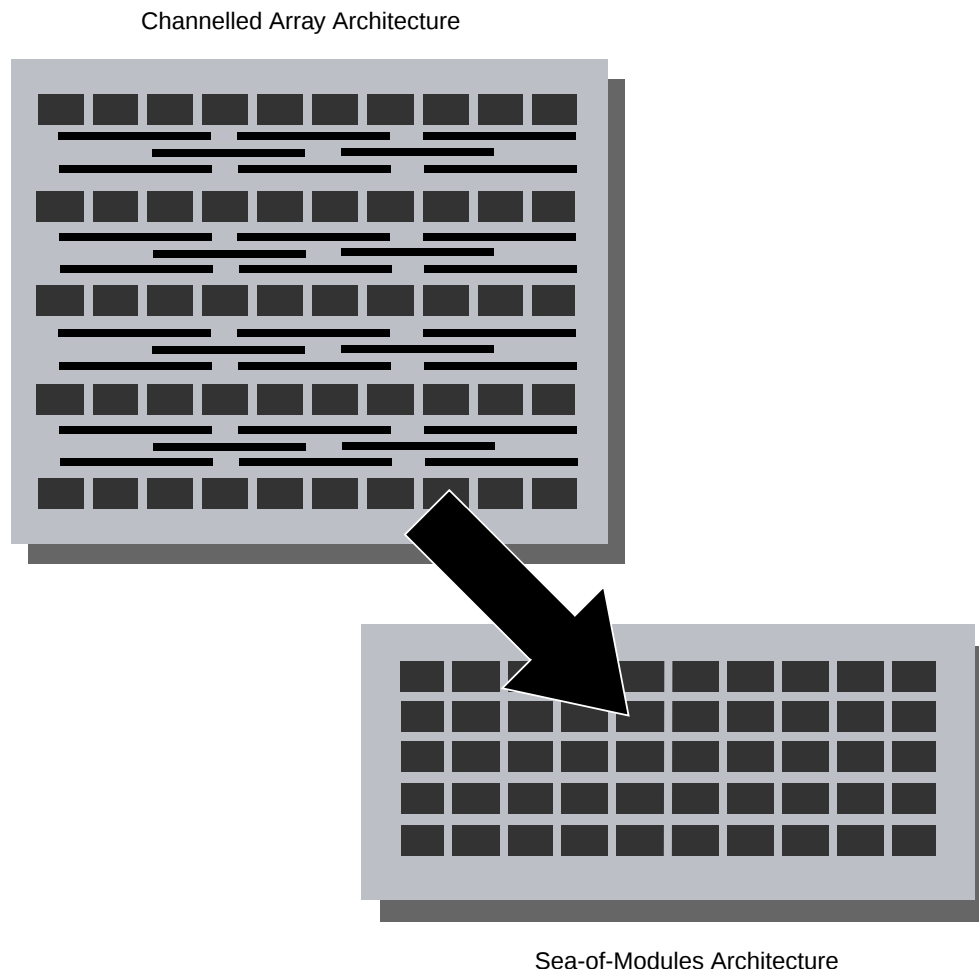


Figure 2 • Channelled Array and Sea-of-Modules Architectures

The R-cell (or register cell) contains a flip-flop featuring more control signals than in previous Actel architectures, including asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines). The R-cell (Figure 3) registers feature programmable clock polarity, selectable on a register-by-register basis. This provides the designer with additional flexibility while allowing mapping of synthesized functions into the SX FPGA. The clock source for the R-cell can be chosen from the hard-wired clock or the routed clock.

The C-cell (or combinatorial cell, Figure 4) implements a range of combinatorial functions up to 5-inputs. Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions which can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX

architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

Chip Architecture

The SX Family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

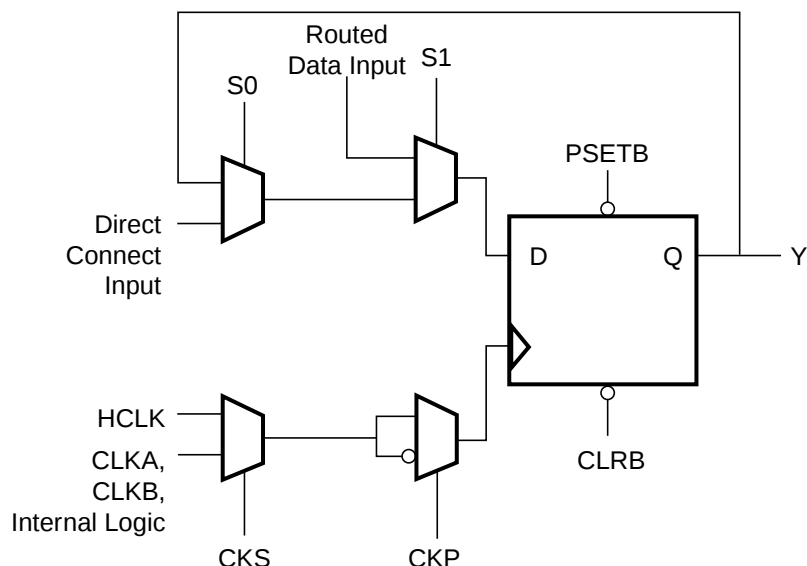


Figure 3 • R-Cell

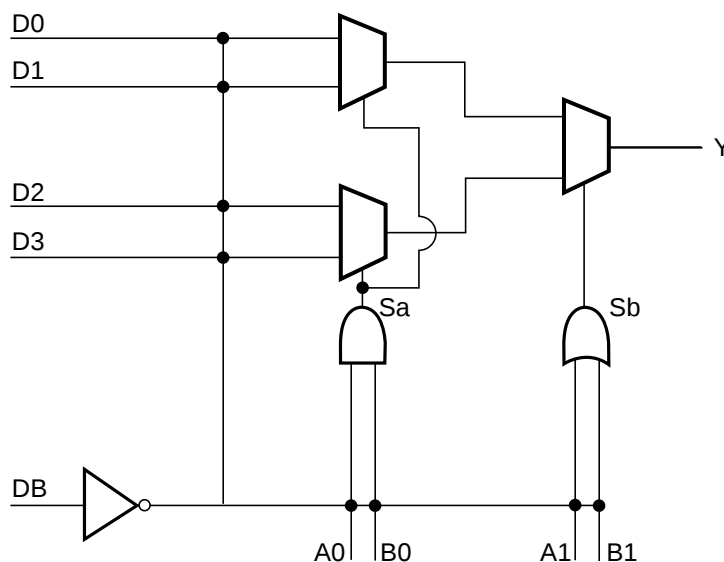


Figure 4 • C-Cell

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (see Figure 5). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature significantly more SuperCluster 1 modules than SuperCluster

2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative new local routing resources called *FastConnect* and *DirectConnect* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (see Figure 6 and Figure 7). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

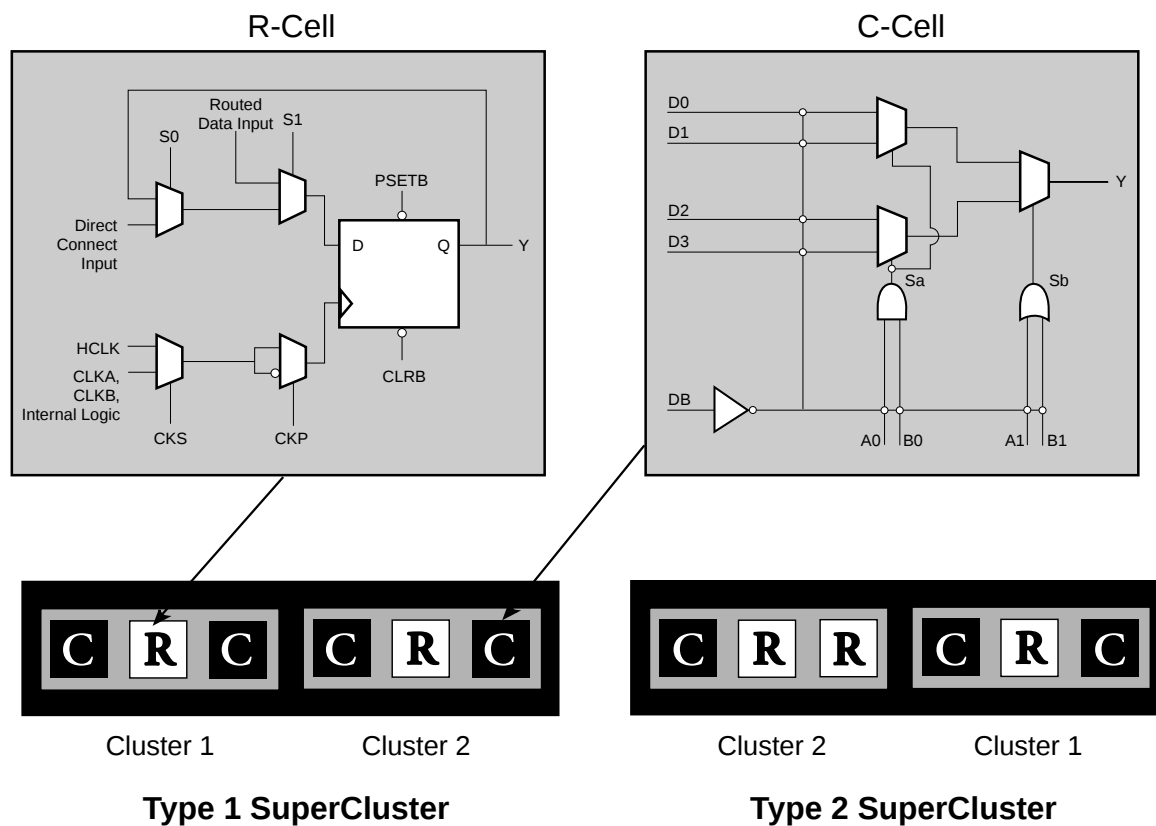


Figure 5 • Cluster Organization

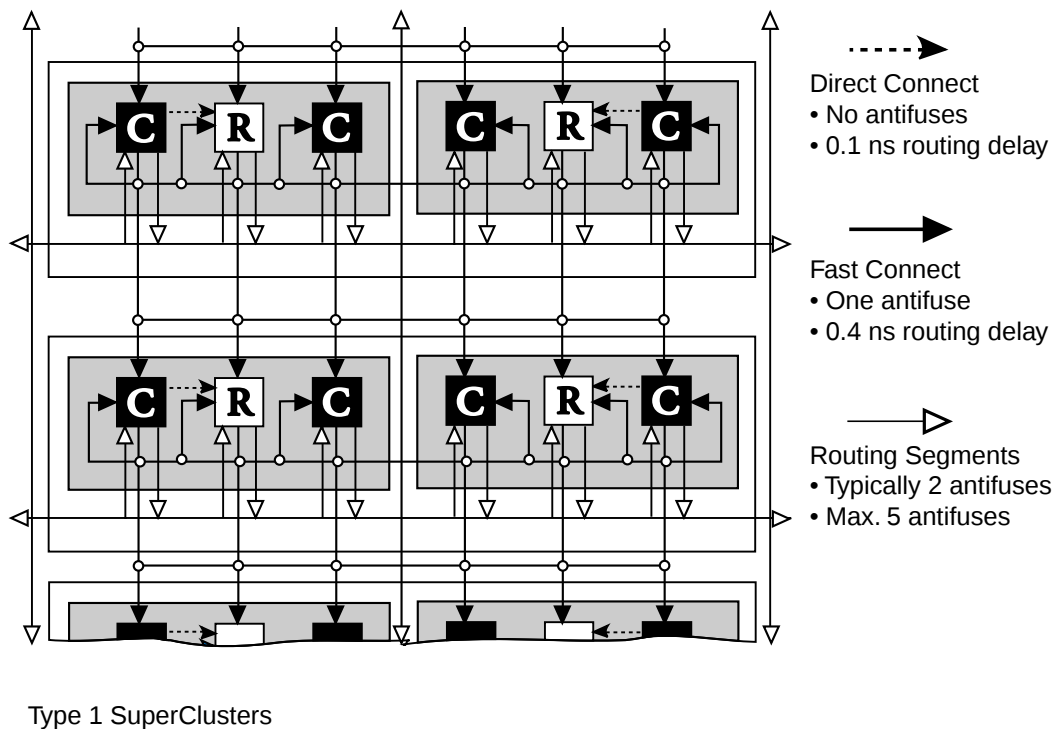


Figure 6 • DirectConnect and FastConnect for Type 1 SuperClusters

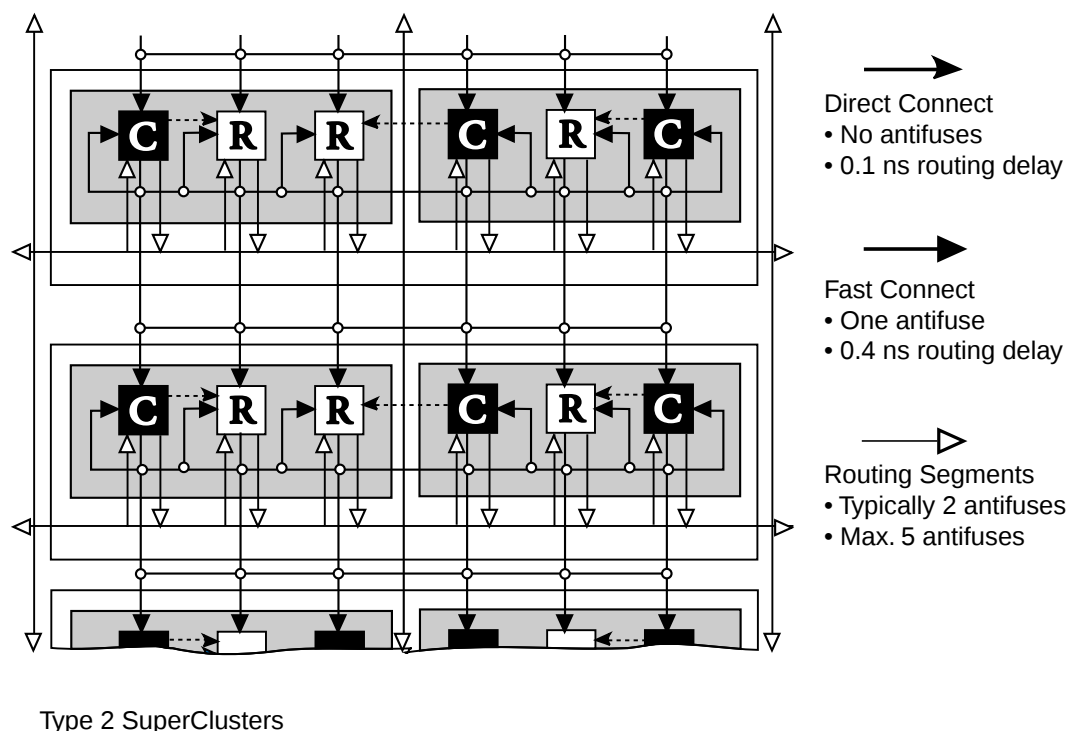


Figure 7 • DirectConnect and FastConnect for Type 2 SuperClusters

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place and route software to minimize signal propagation delays.

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hard-wired from the HCLK buffer to the clock select MUX in each R-cell. This provides a fast propagation path for the clock signal, enabling the 4.0 ns clock-to-out (pin-to-pin) performance of the SX devices. The hard-wired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB)

are global clocks that can be sourced from external pins or from internal signal logic within the SX device.

Other Architecture Features

Technology

Actel's SX Family of FPGAs is implemented in high-voltage twin-well CMOS using three layers of metal and 0.35 micron design rules (moving quickly to 0.25 micron). The M2/M3 antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals, and has a programmed ("on" state) resistance of 25 ohms with capacitance of 1.6 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the Actel SX Family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs which previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time-to-market. Using timing-driven place and route tools, designers can achieve highly deterministic device performance.

With SX devices, designers can achieve a higher level of performance without recourse to complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tri-state output, or a bi-directional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 4.0 ns, and external set-up time as low as 0.6 ns. I/O cells including embedded latches and flip-flops require instantiation in HDL code, a complication not required by SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reducing overall design time.

Power Requirements

The SX Family supports 3.3-volt operation and is designed to tolerate 5-volt inputs. Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path, and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as an SRAM or EPROM does), thereby making it the lowest-power architecture on the market.

JTAG

All SX devices are IEEE 1149.1 (JTAG) compliant. SX devices offer superior diagnostic and testing capabilities by providing JTAG and probing capabilities. These functions are controlled through the special JTAG pins in conjunction with the program fuse. The functionality of each pin is described in Table 2.

Table 2 • JTAG

Program Fuse Blown (Dedicated JTAG Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated JTAG pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10K ohm on TMS

In the dedicated JTAG mode, TCK, TDI and TDO are dedicated JTAG pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10K ohm. TMS can be pulled LOW to initiate the JTAG sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

Design Tool Support

As with all Actel FPGAs, the new SX Family is fully supported by Actel's Designer Series development tools, which include:

- DirectTime for automated, timing-driven place and route;
- ACTgen for fast development using a wide range of macro functions; and
- ACTmap for logic synthesis.

Designer Series supports industry-leading VHDL and Verilog-based design tools, including synthesis tools from industry leaders such as Exemplar Logic, Synplicity, and Synopsys.

Silicon Explorer and SX FPGA

Actel SX FPGAs include internal Probe circuitry to dynamically observe and analyze any signal inside the FPGA during normal device operation. The Probe circuitry is accessed and controlled by the Silicon Explorer--an integrated debugging and logic analysis tool that attaches to a PC. The Silicon Explorer is also an 18-channel logic analyzer that samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Two channels of the logic analyzer have a direct connection to PRA and PRB pins, which can automatically display any two signals inside the FPGA. The remaining 16 channels of the logic analyzer can be used to examine other signals on the board. In addition, Silicon Explorer can read back the design's checksum, allowing designers to verify that the correct design was programmed in the FPGA.

SX Probe Circuit Control Pins

The Silicon Explorer tool uses the JTAG ports (TDI, TCK, TMS and TDO) to select the desired nets for debugging. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 8 illustrates the interconnection between the Silicon Explorer and the FPGA to perform in-circuit debugging.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA and PRB pins as input or bi-directional ports. Because these pins are active during probing, critical signal input through these pins is not available while probing. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuitry.

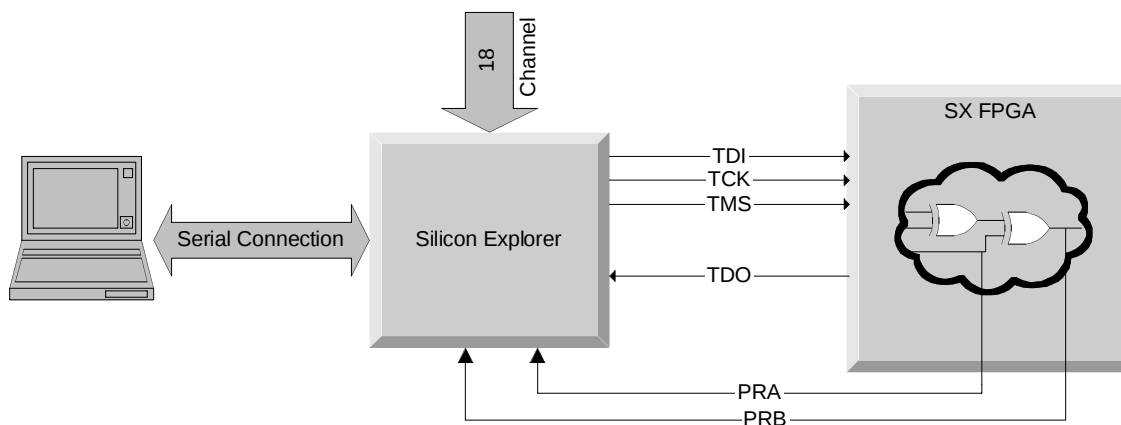


Figure 8 • Probe Setup

3.3V/5V Operating Conditions

Absolute Maximum Ratings¹

Symbol	Parameter	Limits	Units
V_{CCR}^2	DC Supply Voltage ³	–0.3 to +6.0	V
V_{CCA}^2	DC Supply Voltage	–0.3 to +4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX08, A54SX16, A54SX32)	–0.3 to +4.0	V
V_{CCI}^2	DC Supply Voltage (A54SX16P)	–0.3 to +6.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +3.6	V
I_{IO}	I/O Source Sink Current ³	–30 to +5.0	mA
T_{STG}	Storage Temperature	–40 to +125	°C

Notes:

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
- V_{CCR} in the A54SX16P must be greater than or equal to V_{CCI} during power-up and power-down sequences and during normal operation.
- Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC} + 0.5V$ or less than $GND - 0.5V$, the internal protection diodes will forward-bias and can draw excessive current.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range ¹	0 to +70	–40 to +85	–55 to +125	°C
3.3V Power Supply Tolerance	±10	±10	±10	% V_{CC}
5V Power Supply Tolerance	±5	±10	±10	% V_{CC}

Note:

- Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}	($I_{OH} = -20\mu A$) (CMOS) ($I_{OH} = -8mA$) (TTL) ($I_{OH} = -6mA$) (TTL)	($V_{CCI} - 0.1$) 2.4	V_{CCI} V_{CCI}	($V_{CCI} - 0.1$) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	($I_{OL} = 20\mu A$) (CMOS) ($I_{OL} = 12mA$) (TTL) ($I_{OL} = 8mA$) (TTL)		0.10 0.50		0.50	V
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current	See "Evaluating Power in 54SX Devices" on page 14.				

Note: See IEEE PCI specification for A54SX16P 3.3V and 5.0V PCI operation.

PCI Compliance for 54SX Family

The 54SX family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1. Figure 9 and

Figure 10 show the V/I curves and the minimum and maximum PCI drive characteristics of the 54SX family.

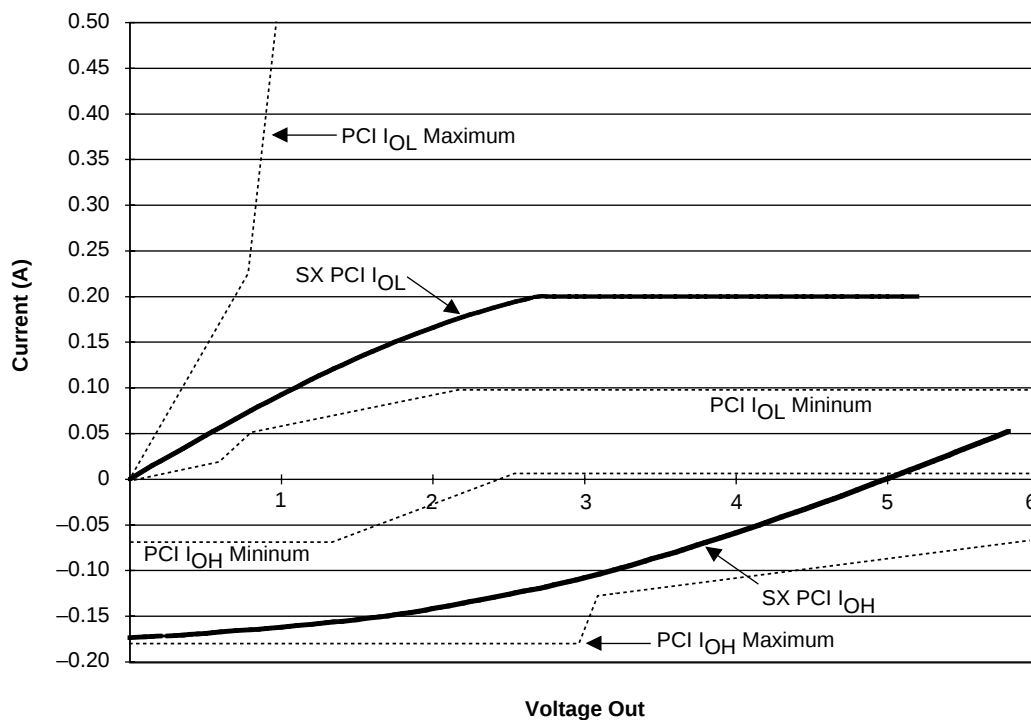


Figure 9 • 5.0V PCI Curve for 54SX Family

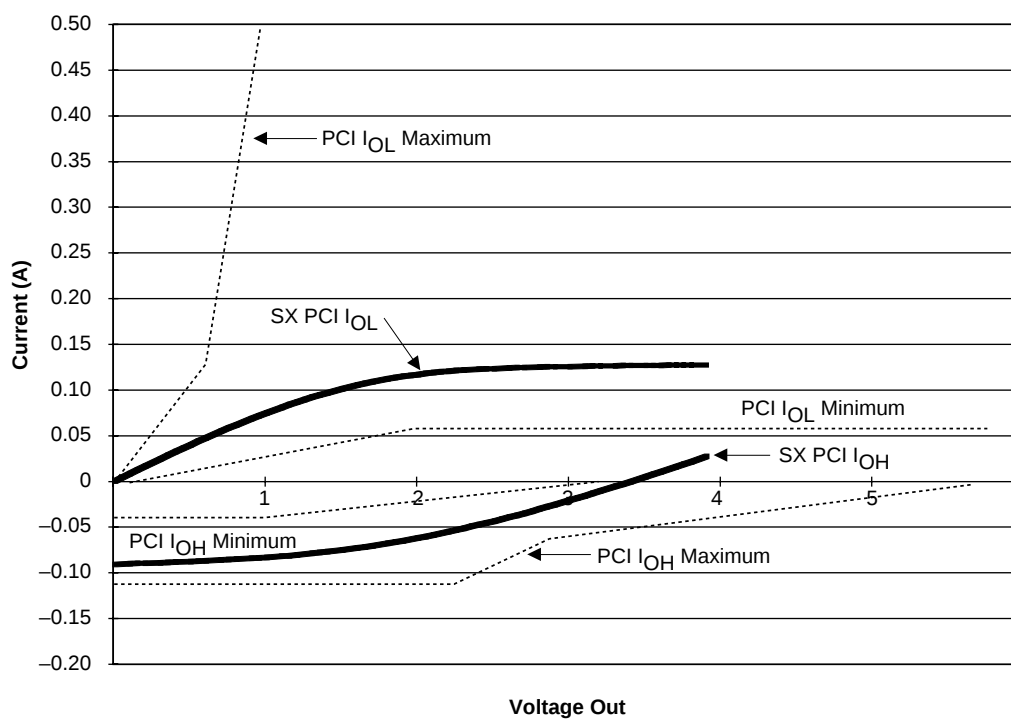


Figure 10 • 3.3V PCI Curve for 54SX Family

Power-Up Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Up Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.
A54SX16P				
3.3V	3.3V	3.3V	3.3V Only	No possible damage to device.
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	Possible damage to device.
3.3V	5.0V	5.0V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Power-Down Sequencing

V _{CCA}	V _{CCR}	V _{CCI}	Power-Down Sequence	Comments
A54SX08, A54SX16, A54SX32				
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.
A54SX16P				
3.3V	3.3V	3.3V	3.3V Only	No possible damage to device.
3.3V	5.0V	3.3V	5.0V First 3.3V Second	Possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.
3.3V	5.0V	5.0V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Evaluating Power in 54SX Devices

A critical element of system reliability is the ability of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

- Estimate the power consumption of the application.
- Calculate the maximum power allowed for the device and package.
- Compare the estimated power and maximum power values.

Estimating Power Consumption

The total power dissipation for the 54SX family is the sum of the DC power dissipation and the AC power dissipation. Use Equation 1 to calculate the estimated power consumption of your application.

$$P_{\text{Total}} = P_{\text{DC}} + P_{\text{AC}} \quad (1)$$

DC Power Dissipation

The power due to standby current is typically a small component of the overall power. The Standby power is shown below for commercial, worst case conditions (70°C).

I _{CC}	V _{CC}	Power
4mA	3.6V	14.4mW

The DC power dissipation is defined in Equation 2 as follows:

$$P_{\text{DC}} = (I_{\text{standby}}) * V_{\text{CCA}} + (I_{\text{standby}}) * V_{\text{CCR}} + (I_{\text{standby}}) * V_{\text{CCI}} + x * V_{\text{OL}} * I_{\text{OL}} + y * (V_{\text{CCI}} - V_{\text{OH}}) * V_{\text{OH}} \quad (2)$$

AC Power Dissipation

The power dissipation of the 54SX Family is usually dominated by the dynamic power dissipation. Dynamic power dissipation is a function of frequency, equivalent capacitance and power supply voltage. The AC power dissipation is defined as follows:

$$P_{\text{AC}} = P_{\text{Module}} + P_{\text{RCLKA Net}} + P_{\text{RCLKB Net}} + P_{\text{HCLK Net}} + P_{\text{Output Buffer}} + P_{\text{Input Buffer}} \quad (3)$$

$$P_{\text{AC}} = V_{\text{CCA}}^2 * [(m * C_{\text{EQM}} * f_m)_{\text{Module}} + (n * C_{\text{EQI}} * f_n)_{\text{Input Buffer}} + (p * (C_{\text{EQO}} + C_L) * f_p)_{\text{Output Buffer}} + (0.5 * (q_1 * C_{\text{EQCR}} * f_{q1}) + (r_1 * f_{q1}))_{\text{RCLKA}} + (0.5 * (q_2 * C_{\text{EQCR}} * f_{q2}) + (r_2 * f_{q2}))_{\text{RCLKB}} + (0.5 * (s_1 * C_{\text{EQHV}} * f_{s1}) + (C_{\text{EQHF}} * f_{s1}))_{\text{HCLK}}] \quad (4)$$

Definition of Terms Used in Formula

m	=	Number of logic modules switching at f_m
n	=	Number of input buffers switching at f_n
p	=	Number of output buffers switching at f_p
q_1	=	Number of clock loads on the first routed array clock
q_2	=	Number of clock loads on the second routed array clock
x	=	Number of I/Os at logic low
y	=	Number of I/Os at logic high
r_1	=	Fixed capacitance due to first routed array clock
r_2	=	Fixed capacitance due to second routed array clock
s_1	=	Number of clock loads on the dedicated array clock
C_{EQM}	=	Equivalent capacitance of logic modules in pF
C_{EQI}	=	Equivalent capacitance of input buffers in pF
C_{EQO}	=	Equivalent capacitance of output buffers in pF
C_{EQCR}	=	Equivalent capacitance of routed array clock in pF
C_{EQHV}	=	Variable capacitance of dedicated array clock
C_{EQHF}	=	Fixed capacitance of dedicated array clock
C_L	=	Output lead capacitance in pF
f_m	=	Average logic module switching rate in MHz
f_n	=	Average input buffer switching rate in MHz
f_p	=	Average output buffer switching rate in MHz
f_{q1}	=	Average first routed array clock rate in MHz
f_{q2}	=	Average second routed array clock rate in MHz
f_{s1}	=	Average dedicated array clock rate in MHz

 C_{EQ} Values

	A54SX08	A54SX16	A54SX16P	A54SX32
C_{EQM} (pF)	3.9	3.9	3.9	3.9
C_{EQI} (pF)	8.8	8.8	8.8	8.8
C_{EQO} (pF)	4.7	4.7	4.7	4.7
C_{EQCR} (pF)	1.6	1.6	1.6	1.6
C_{EQHV}	0.623	0.623	0.623	0.623
C_{EQHF}	96	96	96	96
r_1 (pF)	119	119	119	119
r_2 (pF)	119	119	119	119

Guidelines for Calculating Power Consumption

The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Logic Modules (m)	=	20% of modules
Inputs Switching (n)	=	# inputs/4
Outputs Switching (p)	=	# output/4
First Routed Array Clock Loads (q_1)	=	20% of register cells
Second Routed Array Clock Loads (q_2)	=	20% of register cells
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	$f/10$
Average Input Switching Rate (f_n)	=	$f/5$
Average Output Switching Rate (f_p)	=	$f/10$
Average First Routed Array Clock Rate (f_{q1})	=	$f/2$
Average Second Routed Array Clock Rate (f_{q2})	=	$f/2$
Average Dedicated Array Clock Rate (f_{s1})	=	f
Dedicated Clock Array clock loads (s_1)	=	20% of regular modules

Sample Power Calculation

One of the designs used to characterize the A54SX family was a 528 bit serial in serial out shift register. The design utilized 100% of the dedicated flip-flops of a A54SX16P device. A pattern of 0101... was clocked into the device at frequencies ranging from 1 MHz to 200 MHz. Shifting in a series of 0101... caused 50% of the flip-flops to toggle from low to high at every clock cycle.

Follow the steps below to estimate power consumption. The values provided for the sample calculation below are for the shift register design above. This method for estimating power consumption is conservative and the actual power consumption of your design may be less than the estimated power consumption.

The total power dissipation for the 54SX family is the sum of the AC power dissipation and the DC power dissipation.

$$P_{\text{Total}} = P_{\text{AC}} (\text{dynamic power}) + P_{\text{DC}} (\text{static power}) \quad (5)$$

AC Power Dissipation

$$P_{AC} = P_{Module} + P_{RCLKA\ Net} + P_{RCLKB\ Net} + P_{HCLK\ Net} + P_{Output\ Buffer} + P_{Input\ Buffer} \quad (6)$$

$$P_{AC} = V_{CCA}^2 * [(m * C_{EQM} * f_m)_{Module} + (n * C_{EQI} * f_n)_{Input\ Buffer} + (p * (C_{EQO} + C_L) * f_p)_{Output\ Buffer} + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{RCLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{RCLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1}))_{HCLK}] \quad (7)$$

Step #1: Define Terms Used in Formula

V_{CCA}		3.3
Module		
Number of logic modules switching at f_m (Used 50%)	m	264
Average logic modules switching rate f_m (MHz) (Guidelines: f/10)	f_m	20
Module capacitance C_{EQM} (pf)	C_{EQM}	3.9
Input Buffer		
Number of input buffers switching at f_n	n	1
Average input switching rate f_n (MHz) (Guidelines: f/5)	f_n	40
Input buffer capacitance C_{EQI} (pf)	C_{EQI}	8.8
Output Buffer		
Number of output buffers switching at f_p	p	1
Average output buffers switching rate f_p (MHz) (Guidelines: f/10)	f_p	20
Output buffers buffer Capacitance C_{EQO} (pf)	C_{EQO}	4.7
Output Load capacitance C_L (pf)	C_L	35
RCLKA		
Number of Clock loads q_1	q_1	528
Capacitance of routed array clock (pf)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q1}	200
Fixed capacitance (pf)	r_1	119.6
RCLKB		
Number of Clock loads q_2	q_2	0
Capacitance of routed array clock (pf)	C_{EQCR}	1.6
Average clock rate (MHz)	f_{q2}	0
Fixed capacitance (pf)	r_2	119.6
HCLK		
Number of Clock loads	s_1	0
Variable capacitance of dedicated array clock (pf)	C_{EQHV}	0.623
Fixed capacitance of dedicated array clock (pf)	C_{EQHF}	96
Average clock rate (MHz)	f_{s1}	0

Step #2: Calculate Dynamic Power Consumption

$V_{CCA} * V_{CCA}$	10.89
$m * f_m * C_{EQM}$	0.020592
$n * f_n * C_{EQI}$	0.000352
$p * f_p * (C_{EQO} + C_L)$	0.000794
$0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1})$	0.1084
$0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2})$	0
$0.5 * (s_1 * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1})$	0
$P_{AC} = 1.417W$	

Step #3: Calculate DC Power Dissipation

DC Power Dissipation

$$P_{DC} = (I_{standby}) * V_{CCA} + (I_{standby}) * V_{CCR} + (I_{standby}) * V_{CCI} + X * V_{OL} * I_{OL} + Y * (V_{CCI} - V_{OH}) * V_{OH} \quad (8)$$

For a rough estimate of DC Power Dissipation, only use $P_{DC} = (I_{standby}) * V_{CCA}$. The rest of the formula provides a very small number that can be considered negligible.

$$P_{DC} = (I_{standby}) * V_{CCA}$$

$$P_{DC} = .55mA * 3.3V$$

$$P_{DC} = 0.001815W$$

Step #4: Calculate Total Power Consumption

$$P_{Total} = P_{AC} + P_{DC}$$

$$P_{Total} = 1.417 + 0.001815$$

$$P_{Total} = 1.4188W$$

Step #5: Compare Estimated Power Consumption against Characterized Power Consumption

The estimated total power consumption for this design is 1.42W. The characterized power consumption for this design at 200MHz is 1.0164W. Figure 10 shows the characterized power dissipation numbers for the shift register design using frequencies ranging from 1MHz to 200MHz.

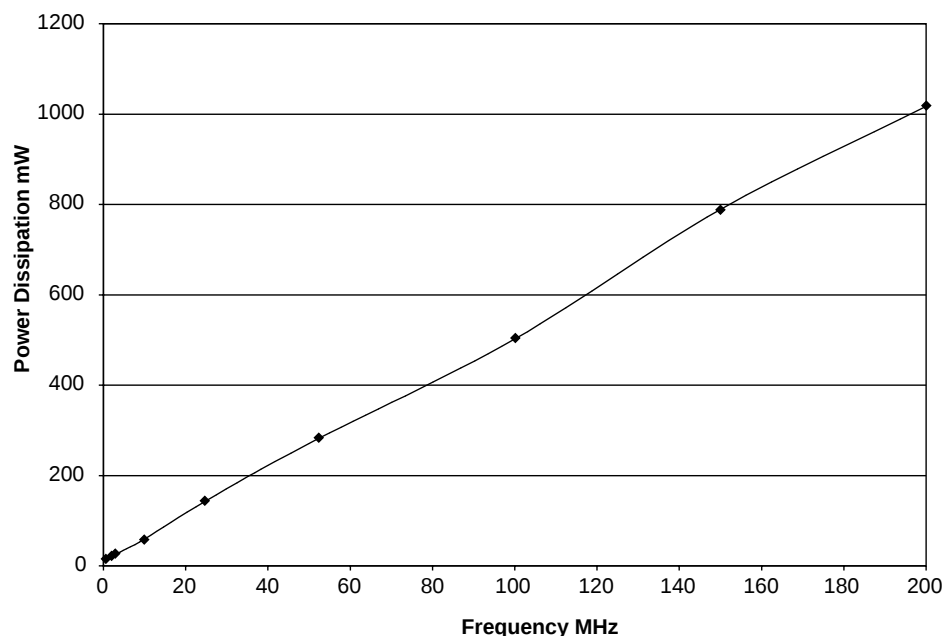


Figure 11 • Power Dissipation

Junction Temperature (T_j)

The temperature that you select in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Use the Equation 4 below to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (4)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P$$

P = Power calculated from Estimating Power Consumption section

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in Package Thermal Characteristics section.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc} , and the junction to ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates.

The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

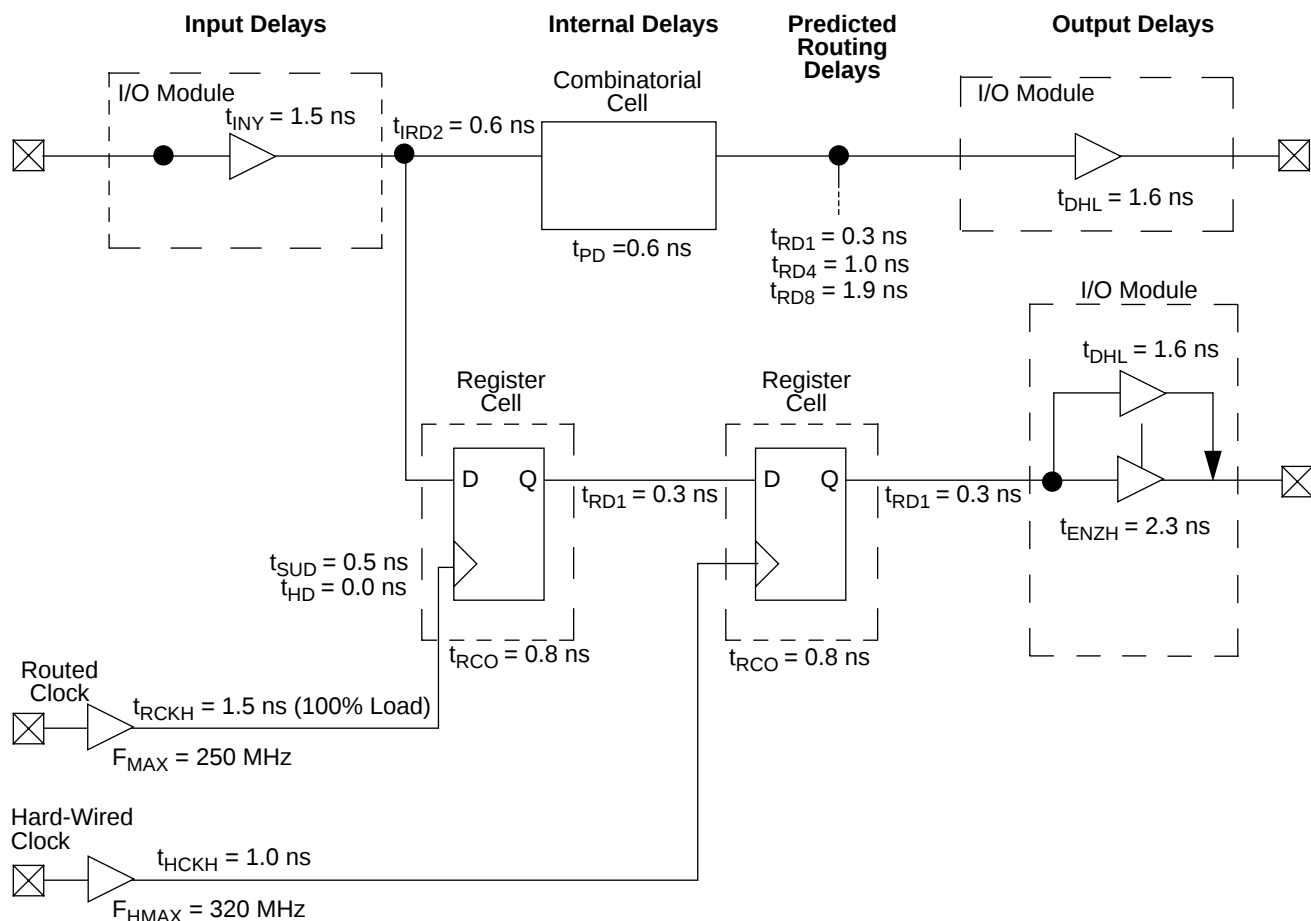
$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{28^\circ\text{C/W}} = 2.86\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Plastic Leaded Chip Carrier (PLCC)	84	12	32	22	°C/W
Thin Quad Flatpack (TQFP)	144	10	32	24	°C/W
Thin Quad Flatpack (TQFP)	176	11	28	21	°C/W
Very Thin Quad Flatpack (VQFP)	100	11	38	32	°C/W
Plastic Quad Flatpack (PQFP) with Heat Spreader	208	8	18	14	°C/W
Plastic Ball Grid Array (PBGA)	329	3	18	13.5	°C/W
Plastic Ball Grid Array (PBGA)	313	8	25	21	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	14.5	°C/W

Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, $T_J = 70^\circ\text{C}$, $V_{CCA} = 3.0\text{V}$)

V_{CCA}	Junction Temperature (T_J)						
	-55	-40	0	25	70	85	125
3.0	0.75	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.70	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.66	0.69	0.77	0.78	0.87	0.92	1.02

54SX Timing Model*



*Values shown for A54SX08-3, worst-case commercial conditions.

Hard-Wired Clock

$$\begin{aligned}\text{External Set-Up} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.0 = 1.3\text{ ns}\end{aligned}$$

Clock-to-Out (Pin-to-Pin)

$$\begin{aligned}&= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.0 + 0.8 + 0.3 + 1.6 = 3.7\text{ ns}\end{aligned}$$

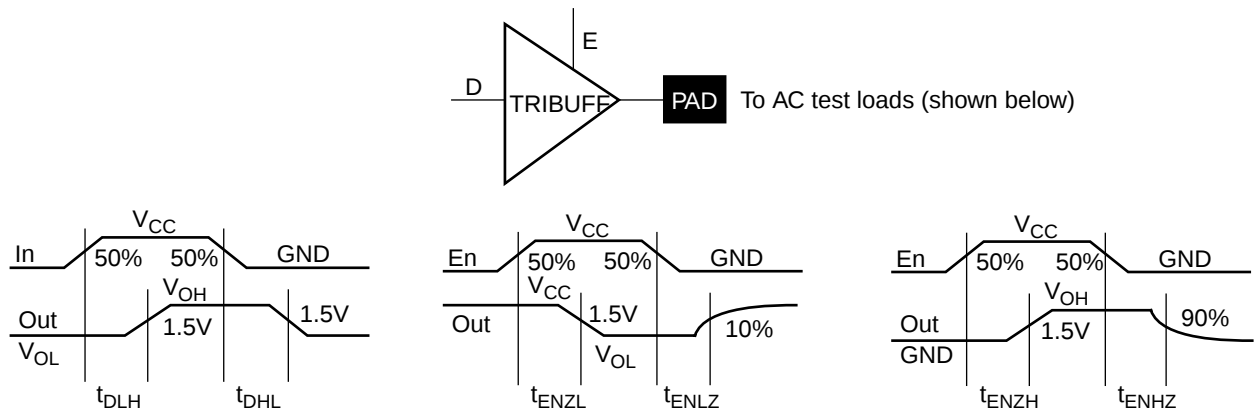
Routed Clock

$$\begin{aligned}\text{External Set-Up} &= t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH} \\ &= 1.5 + 0.3 + 0.5 - 1.5 = 0.8\text{ ns}\end{aligned}$$

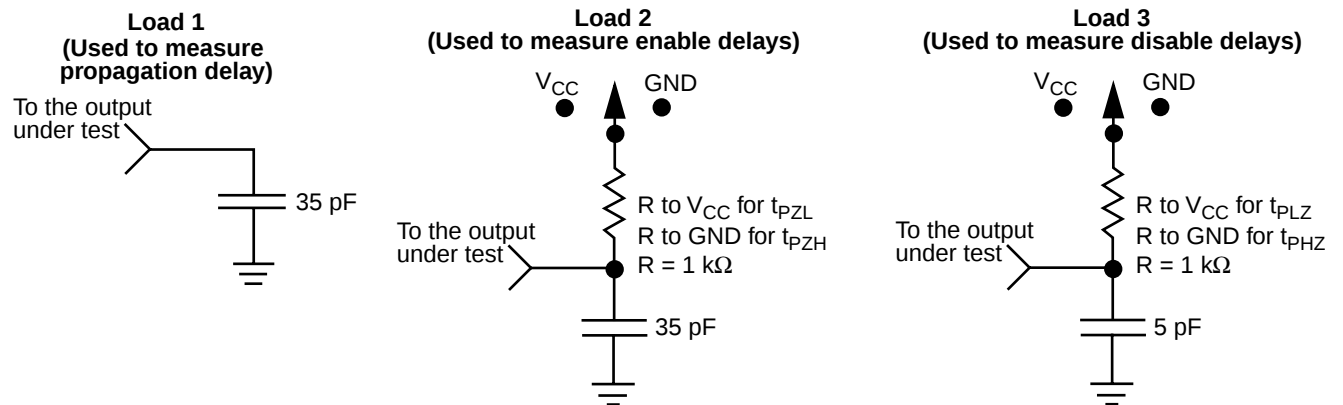
Clock-to-Out (Pin-to-Pin)

$$\begin{aligned}&= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL} \\ &= 1.52 + 0.8 + 0.3 + 1.6 = 4.2\text{ ns}\end{aligned}$$

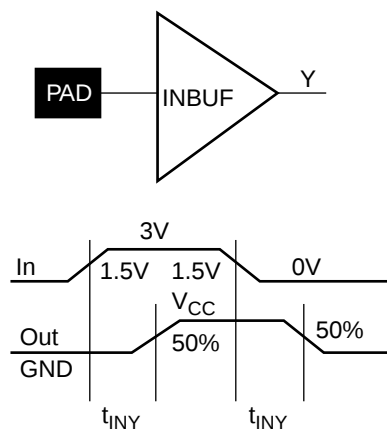
Output Buffer Delays



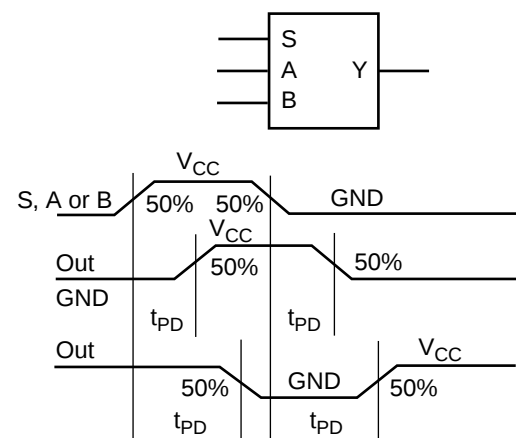
AC Test Loads



Input Buffer Delays

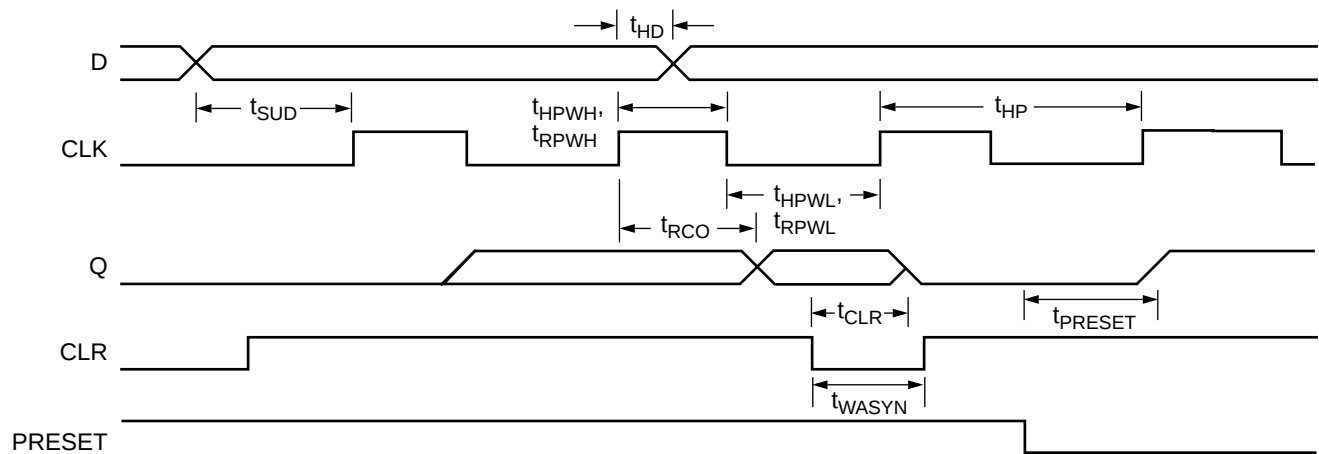
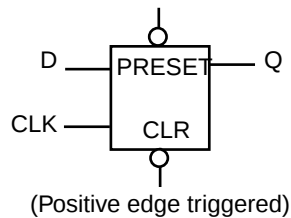


C-Cell Delays



Register Cell Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for 54SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all 54SX family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout (FO=24) routing delays in the data sheet specifications section.

Timing Derating

54SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX08 Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

C-Cell Propagation Delays ¹		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays ²										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
t_{RD18}	FO=18 Routing Delay		4.2		4.8		5.4		6.4	ns
t_{RD24}	FO=24 Routing Delay		5.5		6.3		7.1		8.4	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX08 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t _{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays¹										
t _{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{IRD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t _{IRD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t _{IRD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{IRD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t _{IRD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
t _{IRD18}	FO=18 Routing Delay		4.2		4.8		5.4		6.4	ns
t _{IRD24}	FO=24 Routing Delay		5.5		6.3		7.1		8.4	ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing ¹		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t _{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

A54SX08 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) Array Clock Network		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.0		1.1		1.3		1.5	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.0		1.2		1.4		1.6	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew		0.1		0.2		0.2		0.2	ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.3		1.5		1.7		2.0	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.4		1.6		1.8		2.1	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.4		1.7		1.9		2.2	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		1.5		1.7		2.0		2.3	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.5		1.7		1.9		2.2	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		1.5		1.8		2.0		2.3	ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.1		0.2		0.2		0.2	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.3		0.3		0.4		0.4	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.3		0.3		0.4		0.4	ns

A54SX16 Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

C-Cell Propagation Delays ¹		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays ²										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
t_{RD18}	FO=18 Routing Delay		4.2		4.8		5.4		6.4	ns
t_{RD24}	FO=24 Routing Delay		5.5		6.3		7.1		8.4	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.2		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX16 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t _{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays¹										
t _{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{IRD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t _{IRD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t _{IRD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{IRD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t _{IRD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
t _{IRD18}	FO=18 Routing Delay		4.2		4.8		5.4		6.4	ns
t _{IRD24}	FO=24 Routing Delay		5.5		6.3		7.1		8.4	ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing ¹		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t _{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

A54SX16 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) Array Clock Network		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.4		1.5		1.8	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.2		1.4		1.6		1.9	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew		0.2		0.2		0.3		0.3	ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.5	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.8		2.1		2.5		2.8	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.8		2.1		2.4		2.8	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.5		0.5		0.5		0.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8	ns

A54SX16P Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

C-Cell Propagation Delays ¹		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays ²										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t_{RD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t_{RD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t_{RD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
t_{RD18}	FO=18 Routing Delay		4.2		4.8		5.4		6.4	ns
t_{RD24}	FO=24 Routing Delay		5.5		6.3		7.1		8.4	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.9		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.5		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX16P Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t _{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays¹										
t _{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{IRD2}	FO=2 Routing Delay		0.6		0.7		0.8		0.9	ns
t _{IRD3}	FO=3 Routing Delay		0.8		0.9		1.0		1.2	ns
t _{IRD4}	FO=4 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{IRD8}	FO=8 Routing Delay		1.9		2.2		2.5		2.9	ns
t _{IRD12}	FO=12 Routing Delay		2.8		3.2		3.7		4.3	ns
t _{IRD18}	FO=18 Routing Delay		4.2		4.8		5.4		6.4	ns
t _{IRD24}	FO=24 Routing Delay		5.5		6.3		7.1		8.4	ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX16P Timing Characteristics (continued)(Worst-Case Commercial Conditions $V_{CCR} = 3.0\text{ V}$, V_{CCA} , $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

I/O Module – PCI Output Timing ¹		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DLH}	Data-to-Pad LOW to HIGH		1.8		2.0		2.3		2.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.7		2.0		2.2		2.6	ns
t_{ENZL}	Enable-to-Pad, Z to L		0.8		1.0		1.1		1.3	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.2		1.2		1.5		1.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		1.0		1.1		1.3		1.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.1		1.3		1.5		1.7	ns

Note:

1. Delays based on 10pF loading.

(Worst-Case Commercial Conditions $V_{CCR} = 3.0\text{ V}$, V_{CCA} , $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

I/O Module – TTL Output Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.5		2.8		3.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.0		2.3		2.6		3.1	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.5		2.9		3.2		3.8	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.0		3.5		3.9		4.6	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.1		3.6	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns

A54SX16P Timing Characteristics (continued)

(Worst-Case Commercial Conditions $V_{CCR} = 4.75\text{ V}$, V_{CCA} , $V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

I/O Module – TTL Output Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DLH}	Data-to-Pad LOW to HIGH		2.4		2.8		3.1		3.7	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.3		2.9		3.2		3.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		3.0		3.4		3.9		4.6	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.3		3.8		4.3		5.0	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.3		2.7		3.0		3.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.8		3.2		3.7		4.3	ns

(Worst-Case Commercial Conditions $V_{CCR} = 4.75\text{ V}$, V_{CCA} , $V_{CCI} = 4.75\text{ V}$, $T_J = 70^\circ\text{C}$)

I/O Module – TTL/PCI Output Timing		‘–3’ Speed		‘–2’ Speed		‘–1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DLH}	Data-to-Pad LOW to HIGH		1.5		1.7		2.0		2.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		1.9		2.2		2.4		2.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.3		2.6		3.0		3.5	ns
t_{ENZH}	Enable-to-Pad, Z to H		1.5		1.7		1.9		2.3	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.1		3.5		4.1	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.9		3.3		3.7		4.4	ns

A54SX16P Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) Array Clock Network		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.2		1.4		1.5		1.8	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.2		1.4		1.6		1.9	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew		0.2		0.2		0.3		0.3	ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.6		1.8		2.1		2.5	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		1.8		2.0		2.3		2.7	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		1.8		2.1		2.5		2.8	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		1.8		2.1		2.4		2.8	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.0		2.2		2.5		3.0	ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.5		0.5		0.5		0.7	ns
t _{RCKSW}	Maximum Skew (50% Load)		0.5		0.6		0.7		0.8	ns
t _{RCKSW}	Maximum Skew (100% Load)		0.5		0.6		0.7		0.8	ns

A54SX32 Timing Characteristics

(Worst-Case Commercial Conditions, $V_{CCR} = 4.75\text{ V}$, $V_{CCA}, V_{CCI} = 3.0\text{ V}$, $T_J = 70^\circ\text{C}$)

C-Cell Propagation Delays ¹		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{PD}	Internal Array Module		0.6		0.7		0.8		0.9	ns
Predicted Routing Delays ²										
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.3		0.4		0.4		0.5	ns
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.7		0.8		0.9		1.0	ns
t_{RD3}	FO=3 Routing Delay		1.0		1.2		1.4		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.4		1.6		1.8		2.1	ns
t_{RD8}	FO=8 Routing Delay		2.7		3.1		3.5		4.1	ns
t_{RD12}	FO=12 Routing Delay		4.0		4.7		5.3		6.2	ns
t_{RD18}	FO=18 Routing Delay		6.0		7.0		7.9		9.3	ns
t_{RD24}	FO=24 Routing Delay		8.1		9.3		10.5		12.4	ns
R-Cell Timing										
t_{RCO}	Sequential Clock-to-Q		0.8		1.1		1.3		1.4	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.6		0.7		0.8	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.7		0.8		0.9		1.0	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.5		0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.4		1.6		1.8		2.1		ns

Notes:

- For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX32 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{INYH}	Input Data Pad-to-Y HIGH		1.5		1.7		1.9		2.2	ns
t _{INYL}	Input Data Pad-to-Y LOW		1.5		1.7		1.9		2.2	ns
Predicted Input Routing Delays¹										
t _{IRD1}	FO=1 Routing Delay		0.3		0.4		0.4		0.5	ns
t _{IRD2}	FO=2 Routing Delay		0.7		0.8		0.9		1.0	ns
t _{IRD3}	FO=3 Routing Delay		1.0		1.2		1.4		1.6	ns
t _{IRD4}	FO=4 Routing Delay		1.4		1.6		1.8		2.1	ns
t _{IRD8}	FO=8 Routing Delay		2.7		3.1		3.5		4.1	ns
t _{IRD12}	FO=12 Routing Delay		4.0		4.7		5.3		6.2	ns
t _{IRD18}	FO=18 Routing Delay		6.0		7.0		7.9		9.3	ns
t _{IRD24}	FO=24 Routing Delay		8.1		9.3		10.5		12.4	ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

A54SX32 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing ¹		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{DLH}	Data-to-Pad LOW to HIGH		1.6		1.9		2.1		2.5	ns
t _{DHL}	Data-to-Pad HIGH to LOW		1.6		1.9		2.1		2.5	ns
t _{ENZL}	Enable-to-Pad, Z to L		2.1		2.4		2.8		3.2	ns
t _{ENZH}	Enable-to-Pad, Z to H		2.3		2.7		3.1		3.6	ns
t _{ENLZ}	Enable-to-Pad, L to Z		1.4		1.7		1.9		2.2	ns
t _{ENHZ}	Enable-to-Pad, H to Z		1.3		1.5		1.7		2.0	ns

Note:

1. Delays based on 35pF loading, except t_{ENZL} and t_{ENZH}. For t_{ENZL} and t_{ENZH} the loading is 5pF.

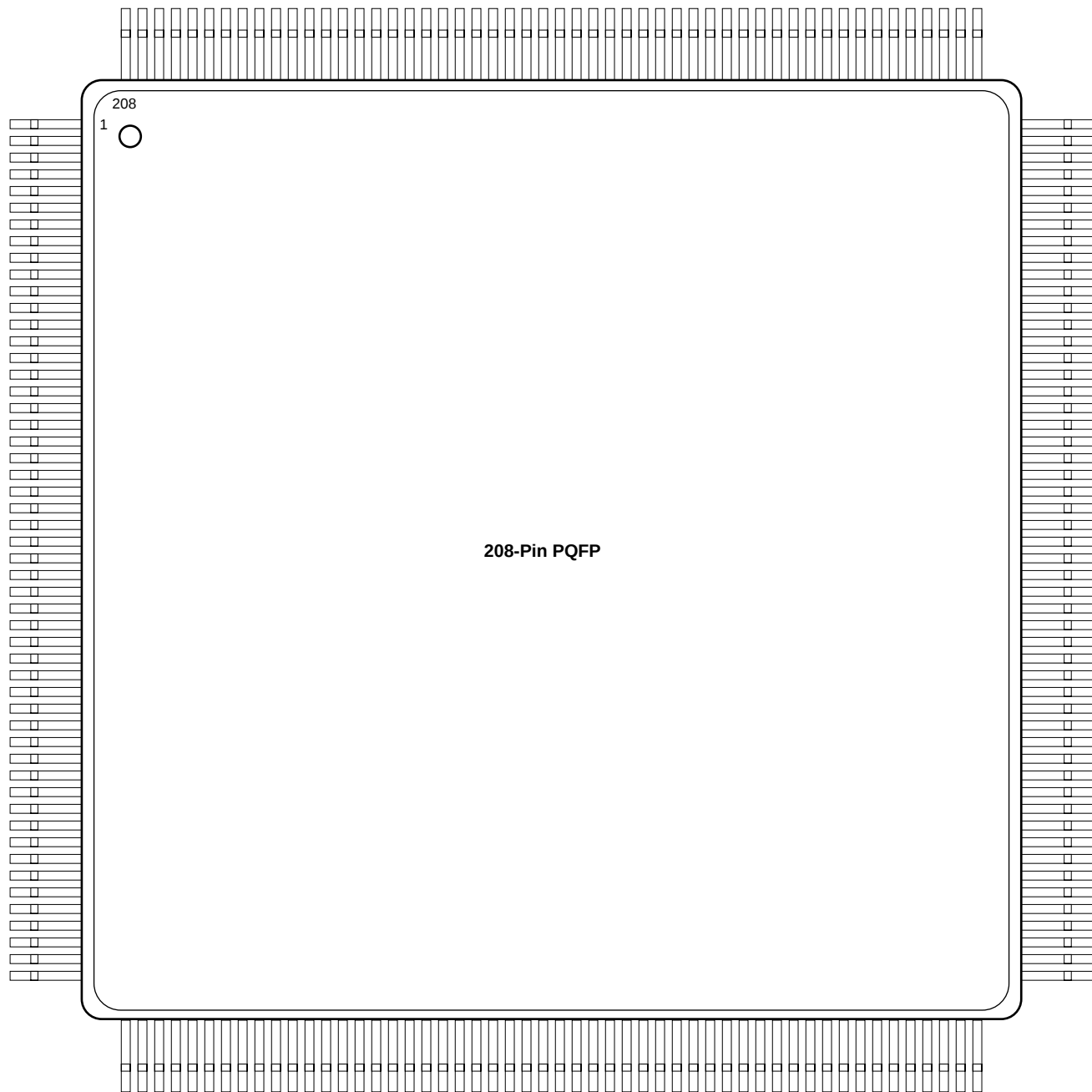
A54SX32 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) Array Clock Network		‘-3’ Speed		‘-2’ Speed		‘-1’ Speed		‘Std’ Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t _{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.9		2.1		2.4		2.8	ns
t _{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.9		2.1		2.4		2.8	ns
t _{HPWH}	Minimum Pulse Width HIGH	1.4		1.6		1.8		2.1		ns
t _{HPWL}	Minimum Pulse Width LOW	1.4		1.6		1.8		2.1		ns
t _{HCKSW}	Maximum Skew		0.3		0.4		0.4		0.5	ns
t _{HP}	Minimum Period	2.7		3.1		3.6		4.2		ns
f _{HMAX}	Maximum Frequency		350		320		280		240	MHz
Routed Array Clock Networks										
t _{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		2.4		2.7		3.0		3.5	ns
t _{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.4		2.7		3.1		3.6	ns
t _{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.7		3.0		3.5		4.1	ns
t _{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.7		3.1		3.6		4.2	ns
t _{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.7		3.1		3.5		4.1	ns
t _{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.8		3.2		3.6		4.3	ns
t _{RPWH}	Min. Pulse Width HIGH	2.1		2.4		2.7		3.2		ns
t _{RPWL}	Min. Pulse Width LOW	2.1		2.4		2.7		3.2		ns
t _{RCKSW}	Maximum Skew (Light Load)		0.85		0.98		1.1		1.3	ns
t _{RCKSW}	Maximum Skew (50% Load)		1.23		1.4		1.6		1.9	ns
t _{RCKSW}	Maximum Skew (100% Load)		1.30		1.5		1.7		2.0	ns

Package Pin Assignments

208-Pin PQFP (Top View)



208-Pin PQFP

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	NC	I/O	I/O
5	I/O	I/O	I/O
6	NC	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	I/O	I/O	I/O
11	TMS	TMS	TMS
12	V _{CCI}	V _{CCI}	V _{CCI}
13	I/O	I/O	I/O
14	NC	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	NC	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	NC	I/O	I/O
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	NC	I/O	I/O
24	I/O	I/O	I/O
25	V _{CCR}	V _{CCR}	V _{CCR}
26	GND	GND	GND
27	V _{CCA}	V _{CCA}	V _{CCA}
28	GND	GND	GND
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	NC	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	NC	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	NC	I/O	I/O
40	V _{CCI}	V _{CCI}	V _{CCI}
41	V _{CCA}	V _{CCA}	V _{CCA}
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	I/O	I/O	I/O
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	NC	I/O	I/O
49	I/O	I/O	I/O
50	NC	I/O	I/O
51	I/O	I/O	I/O
52	GND	GND	GND
53	I/O	I/O	I/O

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
54	I/O	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	I/O	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	V _{CCI}	V _{CCI}	V _{CCI}
61	NC	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	NC	I/O	I/O
65*	I/O	I/O	NC*
66	I/O	I/O	I/O
67	NC	I/O	I/O
68	I/O	I/O	I/O
69	I/O	I/O	I/O
70	NC	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	NC	I/O	I/O
74	I/O	I/O	I/O
75	NC	I/O	I/O
76	PRB, I/O	PRB, I/O	PRB, I/O
77	GND	GND	GND
78	V _{CCA}	V _{CCA}	V _{CCA}
79	GND	GND	GND
80	V _{CCR}	V _{CCR}	V _{CCR}
81	I/O	I/O	I/O
82	HCLK	HCLK	HCLK
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	NC	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	NC	I/O	I/O
89	I/O	I/O	I/O
90	I/O	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	NC	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	NC	I/O	I/O
98	V _{CCI}	V _{CCI}	V _{CCI}
99	I/O	I/O	I/O
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	TDO, I/O	TDO, I/O	TDO, I/O
104	I/O	I/O	I/O
105	GND	GND	GND
106	NC	I/O	I/O

* Please note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

208-Pin PQFP (Continued)

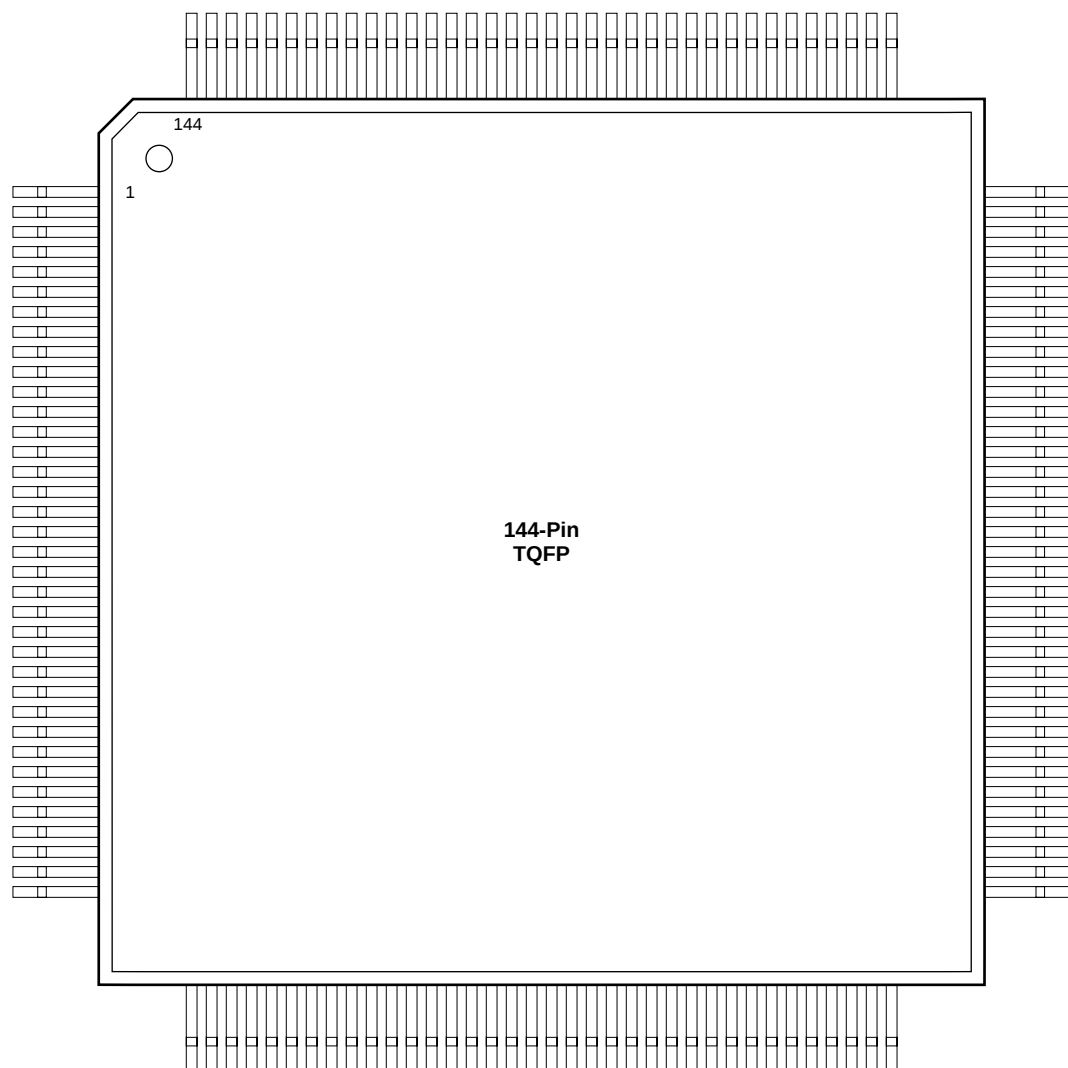
Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
107	I/O	I/O	I/O
108	NC	I/O	I/O
109	I/O	I/O	I/O
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	V _{CCA}	V _{CCA}	V _{CCA}
115	V _{CCI}	V _{CCI}	V _{CCI}
116	NC	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	NC	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	NC	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	NC	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	GND	GND	GND
130	V _{CCA}	V _{CCA}	V _{CCA}
131	GND	GND	GND
132	V _{CCR}	V _{CCR}	V _{CCR}
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	NC	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	NC	I/O	I/O
139	I/O	I/O	I/O
140	I/O	I/O	I/O
141	NC	I/O	I/O
142	I/O	I/O	I/O
143	NC	I/O	I/O
144	I/O	I/O	I/O
145	V _{CCA}	V _{CCA}	V _{CCA}
146	GND	GND	GND
147	I/O	I/O	I/O
148	V _{CCI}	V _{CCI}	V _{CCI}
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	I/O	I/O	I/O
153	I/O	I/O	I/O
154	I/O	I/O	I/O
155	NC	I/O	I/O
156	NC	I/O	I/O
157	GND	GND	GND

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	V _{CCI}	V _{CCI}	V _{CCI}
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	NC	I/O	I/O
168	I/O	I/O	I/O
169	I/O	I/O	I/O
170	NC	I/O	I/O
171	I/O	I/O	I/O
172	I/O	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	NC	I/O	I/O
177	I/O	I/O	I/O
178	I/O	I/O	I/O
179	I/O	I/O	I/O
180	CLKA	CLKA	CLKA
181	CLKB	CLKB	CLKB
182	V _{CCR}	V _{CCR}	V _{CCR}
183	GND	GND	GND
184	V _{CCA}	V _{CCA}	V _{CCA}
185	GND	GND	GND
186	PRA, I/O	PRA, I/O	PRA, I/O
187	I/O	I/O	I/O
188	I/O	I/O	I/O
189	NC	I/O	I/O
190	I/O	I/O	I/O
191	I/O	I/O	I/O
192	NC	I/O	I/O
193	I/O	I/O	I/O
194	I/O	I/O	I/O
195	NC	I/O	I/O
196	I/O	I/O	I/O
197	I/O	I/O	I/O
198	NC	I/O	I/O
199	I/O	I/O	I/O
200	I/O	I/O	I/O
201	V _{CCI}	V _{CCI}	V _{CCI}
202	NC	I/O	I/O
203	NC	I/O	I/O
204	I/O	I/O	I/O
205	NC	I/O	I/O
206	I/O	I/O	I/O
207	I/O	I/O	I/O
208	TCK, I/O	TCK, I/O	TCK, I/O

* Please note that Pin 65 in the A54SX32—PQ208 is a no connect (NC).

Package Pin Assignments (continued)

144-Pin TQFP (Top View)



144-Pin TQFP

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	I/O	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	TMS	TMS	TMS
10	V _{CCI}	V _{CCI}	V _{CCI}
11	GND	GND	GND
12	I/O	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	V _{CCR}	V _{CCR}	V _{CCR}
20	V _{CCA}	V _{CCA}	V _{CCA}
21	I/O	I/O	I/O
22	I/O	I/O	I/O
23	I/O	I/O	I/O
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	GND	GND	GND
29	V _{CCI}	V _{CCI}	V _{CCI}
30	V _{CCA}	V _{CCA}	V _{CCA}
31	I/O	I/O	I/O
32	I/O	I/O	I/O
33	I/O	I/O	I/O
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	GND	GND	GND
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	I/O	I/O	I/O

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
41	I/O	I/O	I/O
42	I/O	I/O	I/O
43	I/O	I/O	I/O
44	V _{CCI}	V _{CCI}	V _{CCI}
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	I/O	I/O	I/O
53	I/O	I/O	I/O
54	PRB, I/O	PRB, I/O	PRB, I/O
55	I/O	I/O	I/O
56	V _{CCA}	V _{CCA}	V _{CCA}
57	GND	GND	GND
58	V _{CCR}	V _{CCR}	V _{CCR}
59	I/O	I/O	I/O
60	HCLK	HCLK	HCLK
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	I/O	I/O	I/O
65	I/O	I/O	I/O
66	I/O	I/O	I/O
67	I/O	I/O	I/O
68	V _{CCI}	V _{CCI}	V _{CCI}
69	I/O	I/O	I/O
70	I/O	I/O	I/O
71	TDO, I/O	TDO, I/O	TDO, I/O
72	I/O	I/O	I/O
73	GND	GND	GND
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	V _{CCA}	V _{CCA}	V _{CCA}
80	V _{CCI}	V _{CCI}	V _{CCI}

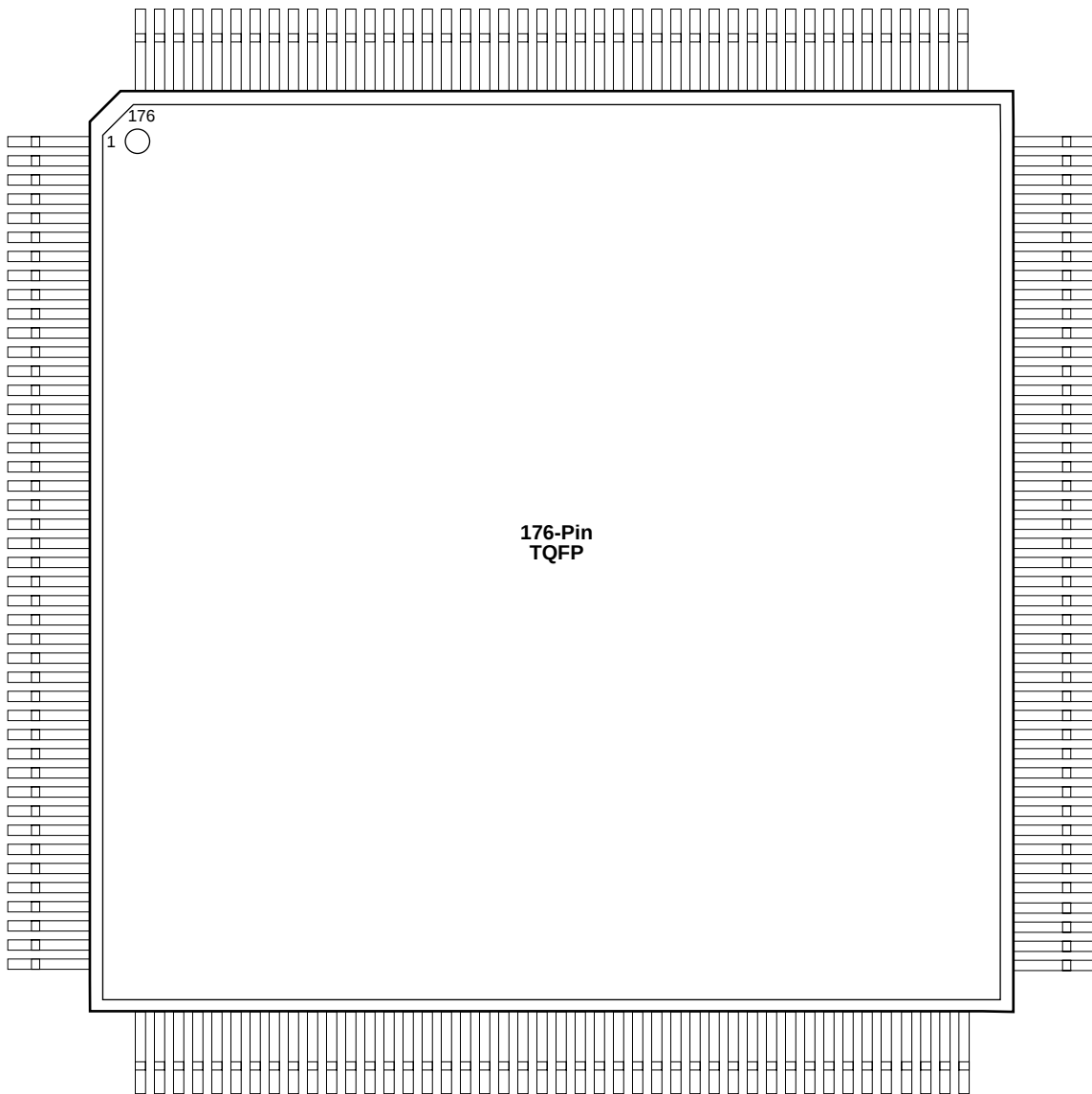
144-Pin TQFP (Continued)

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
81	GND	GND	GND
82	I/O	I/O	I/O
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	I/O	I/O	I/O
88	I/O	I/O	I/O
89	V _{CCA}	V _{CCA}	V _{CCA}
90	V _{CCR}	V _{CCR}	V _{CCR}
91	I/O	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	GND	GND	GND
100	I/O	I/O	I/O
101	GND	GND	GND
102	V _{CCI}	V _{CCI}	V _{CCI}
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	I/O	I/O	I/O
109	GND	GND	GND
110	I/O	I/O	I/O
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O

Pin Number	A54SX08 Function	A54SX16P Function	A54SX32 Function
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	V _{CCI}	V _{CCI}	V _{CCI}
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	I/O	I/O	I/O
119	I/O	I/O	I/O
120	I/O	I/O	I/O
121	I/O	I/O	I/O
122	I/O	I/O	I/O
123	I/O	I/O	I/O
124	I/O	I/O	I/O
125	CLKA	CLKA	CLKA
126	CLKB	CLKB	CLKB
127	V _{CCR}	V _{CCR}	V _{CCR}
128	GND	GND	GND
129	V _{CCA}	V _{CCA}	V _{CCA}
130	I/O	I/O	I/O
131	PRA, I/O	PRA, I/O	PRA, I/O
132	I/O	I/O	I/O
133	I/O	I/O	I/O
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

176-Pin TQFP (Top View)



176-Pin TQFP

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
1	GND	GND	GND
2	TDI, I/O	TDI, I/O	TDI, I/O
3	NC	I/O	I/O
4	I/O	I/O	I/O
5	I/O	I/O	I/O
6	I/O	I/O	I/O
7	I/O	I/O	I/O
8	I/O	I/O	I/O
9	I/O	I/O	I/O
10	TMS	TMS	TMS
11	V _{CCI}	V _{CCI}	V _{CCI}
12	NC	I/O	I/O
13	I/O	I/O	I/O
14	I/O	I/O	I/O
15	I/O	I/O	I/O
16	I/O	I/O	I/O
17	I/O	I/O	I/O
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	I/O	I/O	I/O
21	GND	GND	GND
22	V _{CCA}	V _{CCA}	V _{CCA}
23	GND	GND	GND
24	I/O	I/O	I/O
25	I/O	I/O	I/O
26	I/O	I/O	I/O
27	I/O	I/O	I/O
28	I/O	I/O	I/O
29	I/O	I/O	I/O
30	I/O	I/O	I/O
31	I/O	I/O	I/O
32	V _{CCI}	V _{CCI}	V _{CCI}
33	V _{CCA}	V _{CCA}	V _{CCA}
34	I/O	I/O	I/O
35	I/O	I/O	I/O
36	I/O	I/O	I/O
37	I/O	I/O	I/O
38	I/O	I/O	I/O
39	I/O	I/O	I/O
40	NC	I/O	I/O
41	I/O	I/O	I/O
42	NC	I/O	I/O
43	I/O	I/O	I/O
44	GND	GND	GND

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
45	I/O	I/O	I/O
46	I/O	I/O	I/O
47	I/O	I/O	I/O
48	I/O	I/O	I/O
49	I/O	I/O	I/O
50	I/O	I/O	I/O
51	I/O	I/O	I/O
52	V _{CCI}	V _{CCI}	V _{CCI}
53	I/O	I/O	I/O
54	NC	I/O	I/O
55	I/O	I/O	I/O
56	I/O	I/O	I/O
57	NC	I/O	I/O
58	I/O	I/O	I/O
59	I/O	I/O	I/O
60	I/O	I/O	I/O
61	I/O	I/O	I/O
62	I/O	I/O	I/O
63	I/O	I/O	I/O
64	PRB, I/O	PRB, I/O	PRB, I/O
65	GND	GND	GND
66	V _{CCA}	V _{CCA}	V _{CCA}
67	V _{CCR}	V _{CCR}	V _{CCR}
68	I/O	I/O	I/O
69	HCLK	HCLK	HCLK
70	I/O	I/O	I/O
71	I/O	I/O	I/O
72	I/O	I/O	I/O
73	I/O	I/O	I/O
74	I/O	I/O	I/O
75	I/O	I/O	I/O
76	I/O	I/O	I/O
77	I/O	I/O	I/O
78	I/O	I/O	I/O
79	NC	I/O	I/O
80	I/O	I/O	I/O
81	NC	I/O	I/O
82	V _{CCI}	V _{CCI}	V _{CCI}
83	I/O	I/O	I/O
84	I/O	I/O	I/O
85	I/O	I/O	I/O
86	I/O	I/O	I/O
87	TDO, I/O	TDO, I/O	TDO, I/O
88	I/O	I/O	I/O

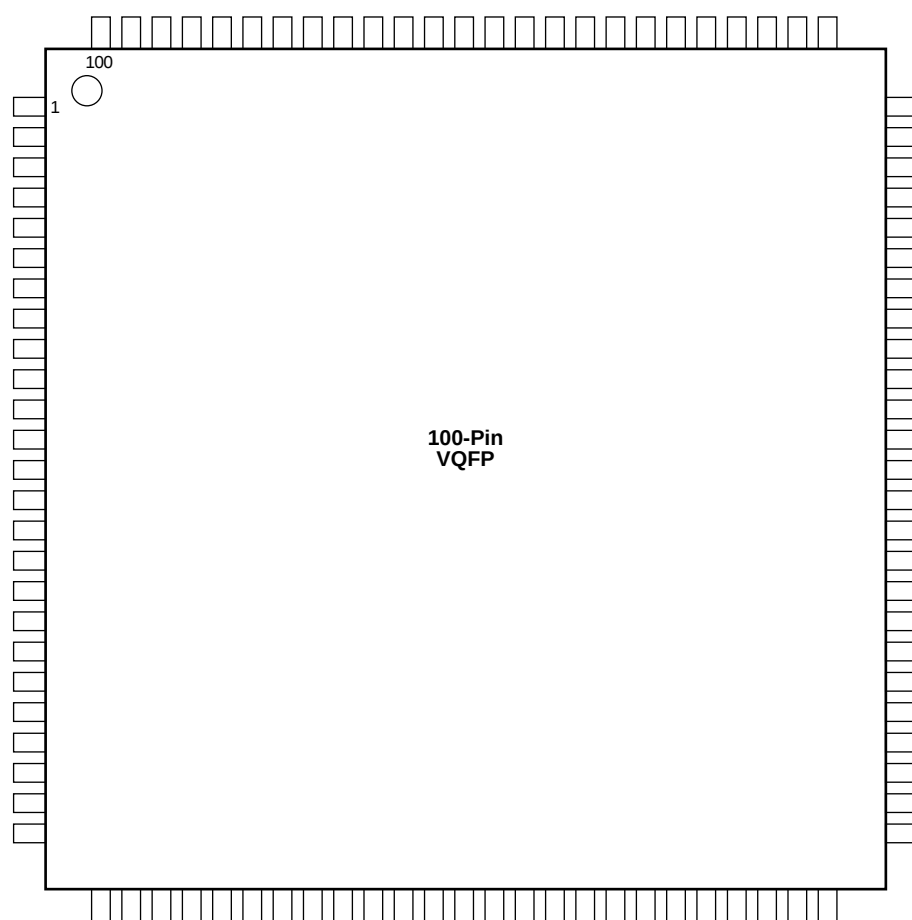
176-Pin TQFP (Continued)

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
89	GND	GND	GND
90	NC	I/O	I/O
91	NC	I/O	I/O
92	I/O	I/O	I/O
93	I/O	I/O	I/O
94	I/O	I/O	I/O
95	I/O	I/O	I/O
96	I/O	I/O	I/O
97	I/O	I/O	I/O
98	V _{CCA}	V _{CCA}	V _{CCA}
99	V _{CCI}	V _{CCI}	V _{CCI}
100	I/O	I/O	I/O
101	I/O	I/O	I/O
102	I/O	I/O	I/O
103	I/O	I/O	I/O
104	I/O	I/O	I/O
105	I/O	I/O	I/O
106	I/O	I/O	I/O
107	I/O	I/O	I/O
108	GND	GND	GND
109	V _{CCA}	V _{CCA}	V _{CCA}
110	GND	GND	GND
111	I/O	I/O	I/O
112	I/O	I/O	I/O
113	I/O	I/O	I/O
114	I/O	I/O	I/O
115	I/O	I/O	I/O
116	I/O	I/O	I/O
117	I/O	I/O	I/O
118	NC	I/O	I/O
119	I/O	I/O	I/O
120	NC	I/O	I/O
121	NC	I/O	I/O
122	V _{CCA}	V _{CCA}	V _{CCA}
123	GND	GND	GND
124	V _{CCI}	V _{CCI}	V _{CCI}
125	I/O	I/O	I/O
126	I/O	I/O	I/O
127	I/O	I/O	I/O
128	I/O	I/O	I/O
129	I/O	I/O	I/O
130	I/O	I/O	I/O
131	NC	I/O	I/O
132	NC	I/O	I/O

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function	A54SX32 Function
133	GND	GND	GND
134	I/O	I/O	I/O
135	I/O	I/O	I/O
136	I/O	I/O	I/O
137	I/O	I/O	I/O
138	I/O	I/O	I/O
139	I/O	I/O	I/O
140	V _{CCI}	V _{CCI}	V _{CCI}
141	I/O	I/O	I/O
142	I/O	I/O	I/O
143	I/O	I/O	I/O
144	I/O	I/O	I/O
145	I/O	I/O	I/O
146	I/O	I/O	I/O
147	I/O	I/O	I/O
148	I/O	I/O	I/O
149	I/O	I/O	I/O
150	I/O	I/O	I/O
151	I/O	I/O	I/O
152	CLKA	CLKA	CLKA
153	CLKB	CLKB	CLKB
154	V _{CCR}	V _{CCR}	V _{CCR}
155	GND	GND	GND
156	V _{CCA}	V _{CCA}	V _{CCA}
157	PRA, I/O	PRA, I/O	PRA, I/O
158	I/O	I/O	I/O
159	I/O	I/O	I/O
160	I/O	I/O	I/O
161	I/O	I/O	I/O
162	I/O	I/O	I/O
163	I/O	I/O	I/O
164	I/O	I/O	I/O
165	I/O	I/O	I/O
166	I/O	I/O	I/O
167	I/O	I/O	I/O
168	NC	I/O	I/O
169	V _{CCI}	V _{CCI}	V _{CCI}
170	I/O	I/O	I/O
171	NC	I/O	I/O
172	NC	I/O	I/O
173	NC	I/O	I/O
174	I/O	I/O	I/O
175	I/O	I/O	I/O
176	TCK, I/O	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

100-Pin VQFP (Top View)



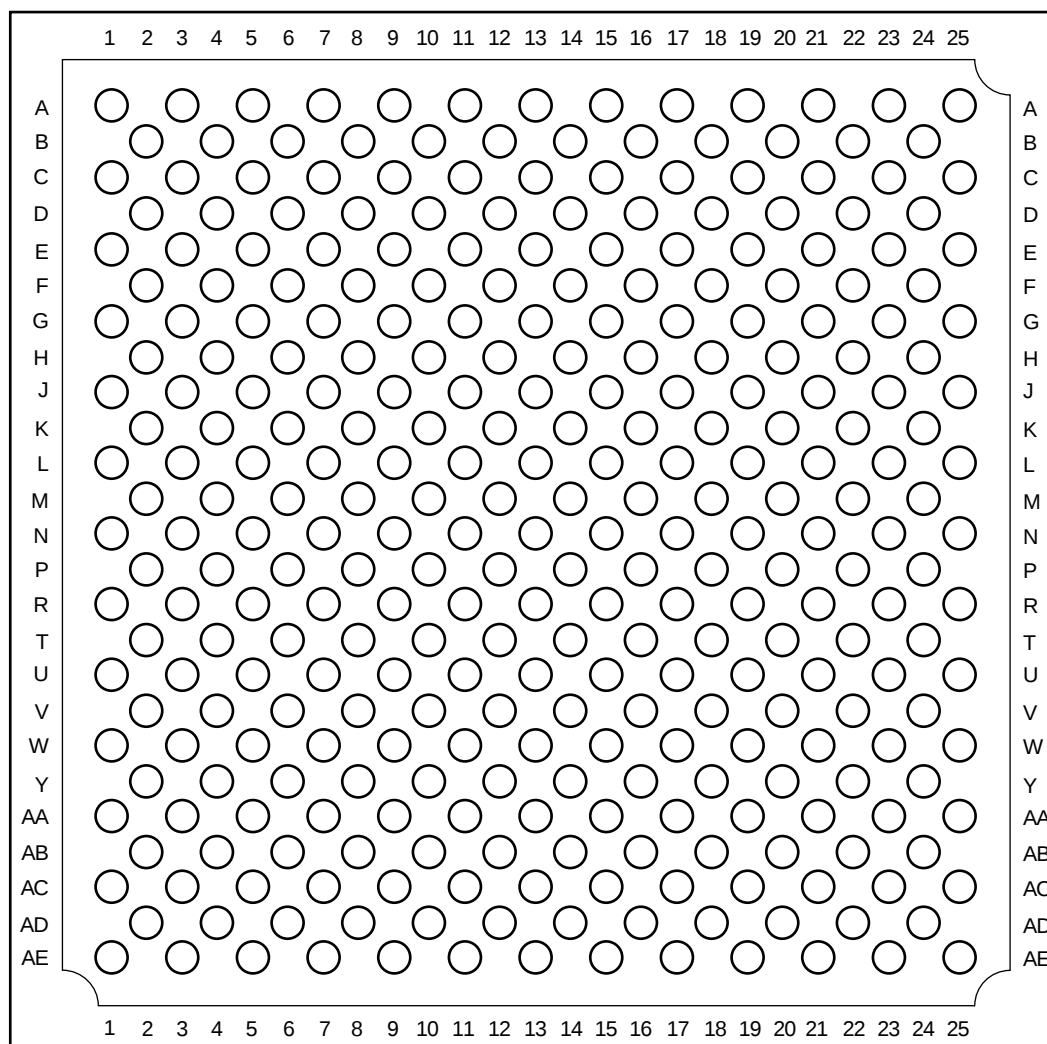
100-VQFP

Pin Number	A54SX08 Function	A54SX16, A54SX16P Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	TMS	TMS
8	V _{CCI}	V _{CCI}
9	GND	GND
10	I/O	I/O
11	I/O	I/O
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	V _{CCI}	V _{CCI}
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	I/O	I/O
29	I/O	I/O
30	I/O	I/O
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	PRB, I/O	PRB, I/O
35	V _{CCA}	V _{CCA}
36	GND	GND
37	V _{CCR}	V _{CCR}
38	I/O	I/O
39	HCLK	HCLK
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	V _{CCI}	V _{CCI}
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	TDO, I/O	TDO, I/O
50	I/O	I/O

Pin Number	A54SX08 Function	A54SX16 A54SX16P Function
51	GND	GND
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	V _{CCA}	V _{CCA}
58	V _{CCI}	V _{CCI}
59	I/O	I/O
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	V _{CCA}	V _{CCA}
68	GND	GND
69	GND	GND
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	V _{CCI}	V _{CCI}
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	CLKA	CLKA
88	CLKB	CLKB
89	V _{CCR}	V _{CCR}
90	V _{CCA}	V _{CCA}
91	GND	GND
92	PRA, I/O	PRA, I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	I/O	I/O
99	I/O	I/O
100	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

313-Pin PBGA (Top View)



313-Pin PBGA

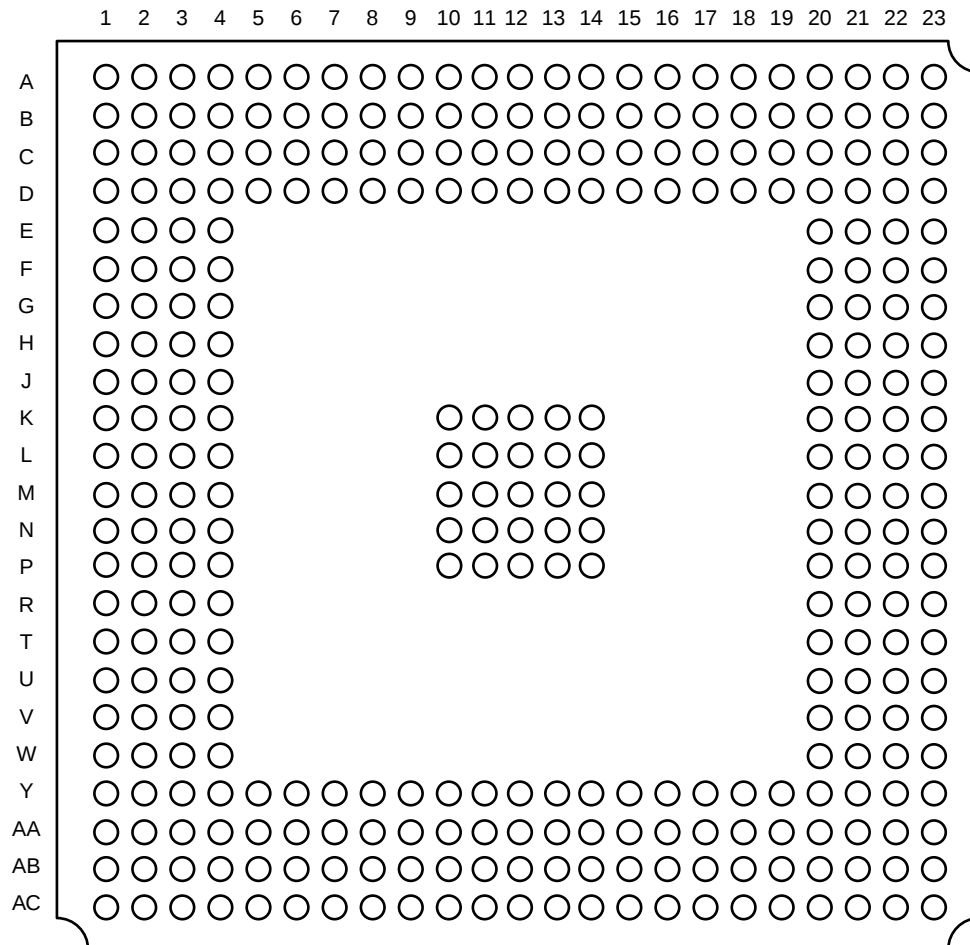
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
C1	TDI, I/O	T8	I/O	AB12	I/O	W25	I/O
D2	I/O	U3	I/O	U13	I/O	U21	I/O
H8	I/O	T6	I/O	AA13	I/O	T20	I/O
K10	I/O	U9	I/O	V14	I/O	U23	I/O
E1	I/O	V4	I/O	R15	I/O	R17	I/O
F4	I/O	W1	I/O	AD14	I/O	U25	I/O
G5	I/O	U7	I/O	AB14	I/O	T22	I/O
F2	I/O	W3	I/O	Y14	I/O	R19	I/O
H6	I/O	V6	I/O	AE15	I/O	T24	I/O
G3	TMS	W5	I/O	U15	I/O	R21	I/O
G1	I/O	Y2	I/O	AC15	I/O	P16	I/O
H4	I/O	AA1	I/O	W15	I/O	R23	I/O
H2	I/O	Y4	I/O	AA15	I/O	P18	I/O
J5	I/O	AA3	I/O	AD16	I/O	R25	I/O
K6	I/O	AC3	I/O	AB16	I/O	P22	I/O
J3	I/O	AC1	I/O	AE17	I/O	P24	I/O
L9	I/O	AE3	I/O	AC17	I/O	N17	I/O
J1	I/O	AD4	I/O	Y16	I/O	N19	I/O
K4	I/O	Y6	I/O	AA17	I/O	N21	I/O
L7	I/O	V8	I/O	AD18	I/O	M18	I/O
K2	I/O	AC5	I/O	U17	I/O	L15	I/O
L5	I/O	T10	I/O	AE19	I/O	M24	I/O
M10	I/O	AE5	I/O	W17	I/O	M22	I/O
L3	I/O	AB6	I/O	AC19	I/O	M20	I/O
M8	I/O	AA7	I/O	Y18	I/O	L25	I/O
L1	I/O	Y8	I/O	AA19	I/O	L17	I/O
M6	I/O	W9	I/O	AD20	I/O	L23	I/O
M4	I/O	AC7	I/O	W19	I/O	L19	I/O
M2	I/O	V10	I/O	AE21	I/O	L21	I/O
N7	I/O	AE7	I/O	AA21	I/O	K24	I/O
N1	I/O	AB8	I/O	AC21	I/O	K22	I/O
P10	I/O	AD8	I/O	AC23	I/O	J25	I/O
P8	I/O	Y10	I/O	AE23	TDO, I/O	K18	I/O
R11	I/O	AC9	I/O	AD24	I/O	J23	I/O
P2	I/O	U11	I/O	AB22	I/O	H24	I/O
P4	I/O	AE9	I/O	AB24	I/O	J17	I/O
P6	I/O	AB10	I/O	V18	I/O	G25	I/O
R1	I/O	W11	I/O	T16	I/O	J19	I/O
R9	I/O	AD10	I/O	AA25	I/O	G23	I/O
R3	I/O	AA11	I/O	Y22	I/O	H20	I/O
R7	I/O	T12	I/O	W21	I/O	G21	I/O
R5	I/O	AC11	I/O	V20	I/O	F24	I/O
T2	I/O	V12	I/O	U19	I/O	G19	I/O
T4	I/O	AE11	I/O	W23	I/O	E25	I/O
U1	I/O	Y12	I/O	T18	I/O	F22	I/O

313-Pin PBGA (Continued)

Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
E21	I/O	C11	I/O	F10	NC
E23	I/O	G11	I/O	C5	NC
C23	I/O	E11	I/O	J7	NC
B24	I/O	B10	I/O	F6	NC
D22	I/O	D10	I/O	Y24	NC
B22	I/O	A9	I/O	A3	NC
F20	I/O	H10	I/O	A1	GND
C21	I/O	C9	I/O	AD2	GND
K16	I/O	E9	I/O	AE25	GND
A21	I/O	B8	I/O	J21	GND
D20	I/O	J9	I/O	A25	GND
E19	I/O	D8	I/O	N11	GND
B20	I/O	A7	I/O	N13	GND
F18	I/O	C7	I/O	R13	GND
G17	I/O	F8	I/O	M14	GND
H16	I/O	E7	I/O	P14	GND
A19	I/O	B6	I/O	M12	GND
D18	I/O	G7	I/O	P12	GND
B18	I/O	A5	I/O	L13	GND
E17	I/O	D6	I/O	N15	GND
C17	I/O	E5	I/O	N3	V _{CCA}
J15	I/O	B4	I/O	V2	V _{CCA}
A17	I/O	C3	I/O	AE13	V _{CCA}
D16	I/O	B2	TCK, I/O	V22	V _{CCA}
G15	I/O	AD12	PRB, I/O	N25	V _{CCA}
B16	I/O	D4	NC	K20	V _{CCA}
E15	I/O	E3	NC	E13	V _{CCA}
K14	I/O	W7	NC	N5	V _{CCR}
C15	I/O	AA5	NC	AC13	V _{CCR}
H14	I/O	AB2	NC	N23	V _{CCR}
A15	I/O	AE1	NC	A13	V _{CCR}
F14	I/O	AB4	NC	AD6	V _{CCI}
D14	I/O	AA9	NC	C13	V _{CCI}
B14	I/O	V16	NC	G9	V _{CCI}
J13	CLKA	AB20	NC	U5	V _{CCI}
G13	CLKB	AD22	NC	M16	V _{CCI}
T14	HCLK	AC25	NC	K8	V _{CCI}
K12	I/O	Y20	NC	C19	V _{CCI}
H12	PRA, I/O	AA23	NC	H22	V _{CCI}
L11	I/O	P20	NC	N9	V _{CCI}
B12	I/O	D24	NC	V24	V _{CCI}
D12	I/O	C25	NC	W13	V _{CCI}
F12	I/O	A23	NC	AB18	V _{CCI}
A11	I/O	H18	NC		
J11	I/O	F16	NC		

Package Pin Assignments (continued)

329-Pin PBGA (Top View)



329-Pin PBGA

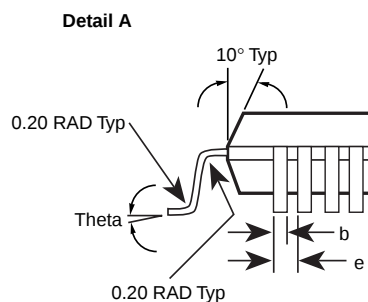
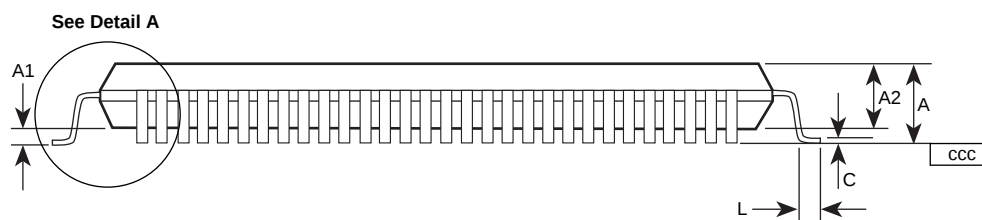
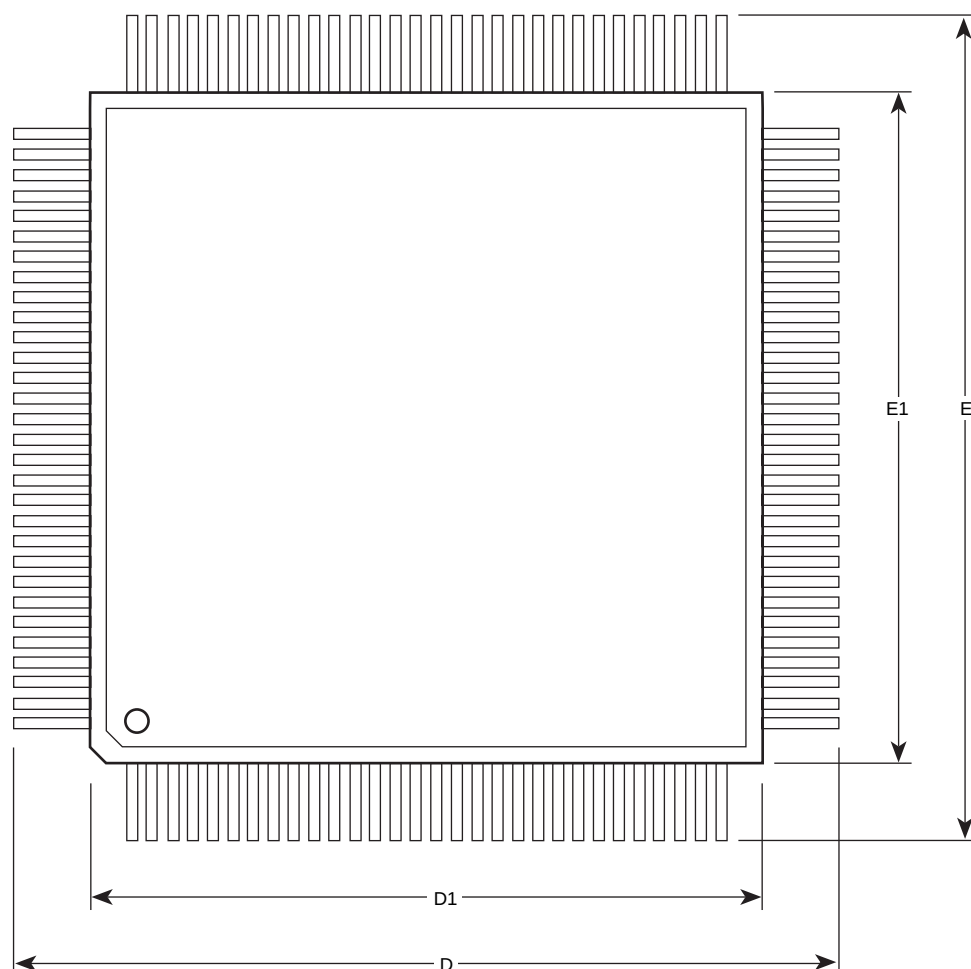
Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
A2	GND	R2	I/O	Y9	I/O	AB20	I/O
C2	TDI	R3	I/O	AA9	I/O	AB21	I/O
D2	I/O	R4	I/O	AB9	I/O	AA20	TDO
D1	I/O	T1	I/O	Y10	I/O	AB23	I/O
E4	I/O	T2	I/O	AA10	I/O	Y20	GND
E3	I/O	T3	I/O	AB10	I/O	Y21	I/O
E2	I/O	T4	I/O	AC10	I/O	AA22	I/O
F4	I/O	U1	I/O	Y11	I/O	Y22	I/O
F3	I/O	U2	I/O	AA11	I/O	Y23	I/O
F1	I/O	U3	V _{CC}	AC11	I/O	W20	I/O
F2	TMS	U4	I/O	AB11	PRB	W21	I/O
G4	I/O	V2	I/O	AB12	I/O	W22	I/O
G3	I/O	V3	I/O	Y12	V _{CCA}	V20	I/O
G2	I/O	V4	I/O	Y13	V _{CCR}	V21	I/O
G1	I/O	W1	I/O	AA12	I/O	V22	I/O
H4	I/O	W2	I/O	AB13	HCLK	V23	I/O
H3	I/O	W3	I/O	AA13	I/O	U20	I/O
H2	I/O	W4	I/O	AC13	I/O	U21	V _{CC}
H1	I/O	Y2	I/O	AC12	I/O	U22	I/O
J4	I/O	AB1	I/O	AC14	I/O	U23	I/O
J3	I/O	AA2	I/O	AB14	I/O	T20	I/O
J2	I/O	Y3	I/O	AA14	I/O	T21	I/O
K4	I/O	Y4	GND	Y14	I/O	T22	I/O
K3	I/O	AA4	I/O	AB15	I/O	T23	I/O
K2	I/O	AB3	I/O	AA15	I/O	R20	I/O
K1	I/O	AB4	I/O	Y15	I/O	R21	I/O
L3	I/O	AC4	I/O	AC16	I/O	R22	I/O
L2	I/O	Y5	I/O	AB16	I/O	R23	I/O
L1	I/O	AA5	I/O	AA16	I/O	P20	I/O
M2	I/O	AB5	I/O	Y16	I/O	P21	I/O
M3	I/O	AC5	I/O	AC17	I/O	P22	I/O
M1	I/O	Y6	I/O	AB17	I/O	P23	I/O
N1	I/O	AA6	I/O	AA17	I/O	N21	I/O
L4	V _{CCR}	AB6	I/O	Y17	I/O	N22	I/O
M4	V _{CCA}	AC6	I/O	AC18	I/O	N23	I/O
N3	I/O	Y7	I/O	AB18	I/O	M20	V _{CCA}
N2	I/O	AA7	I/O	AA18	I/O	L20	V _{CCR}
N4	I/O	AB7	I/O	Y18	I/O	M22	I/O
P1	I/O	AC7	I/O	AC19	I/O	M21	I/O
P2	I/O	Y8	I/O	AB19	I/O	L22	I/O
P3	I/O	AA8	I/O	AA19	I/O	L21	I/O
P4	I/O	AB8	I/O	Y19	I/O	K23	I/O
R1	I/O	AC8	I/O	AC20	I/O	K22	I/O

329-Pin PBGA (Continued)

Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function	Pin Number	A54SX32 Function
K21	I/O	A17	I/O	A5	I/O	A23	GND
K20	I/O	D16	I/O	B5	I/O	AA21	V _{CCI}
J23	I/O	C16	I/O	C5	I/O	C21	V _{CCI}
J22	I/O	B16	I/O	D5	I/O	A22	V _{CCI}
J21	I/O	A16	I/O	B4	I/O	A7	V _{CCI}
J20	I/O	D15	I/O	D3	I/O	A3	V _{CCI}
H23	I/O	C15	I/O	B3	I/O	B1	V _{CCI}
H22	I/O	B15	I/O	C4	I/O	E1	V _{CCI}
H21	I/O	A15	I/O	D4	TCK	V1	V _{CCI}
G22	I/O	D14	I/O	P14	GND	AA1	V _{CCI}
G21	I/O	C14	I/O	M11	GND	AC2	V _{CCI}
H20	V _{CC}	B14	I/O	M12	GND	AC9	V _{CCI}
G23	GND	A14	I/O	M13	GND	AC22	V _{CCI}
G20	I/O	D13	I/O	M14	GND	AA23	V _{CCI}
VCC	V _{CCI}	C13	I/O	N10	GND	M23	V _{CCI}
F23	I/O	A12	I/O	P13	GND	B23	V _{CCI}
F22	I/O	B13	CLKA	P12	GND	N20	NC
F21	I/O	A13	CLKB	P11	GND	L23	NC
F20	I/O	D12	V _{CCR}	P10	GND	Y1	NC
E23	I/O	D11	V _{CCA}	N14	GND	AC21	NC
E22	I/O	C12	I/O	N12	GND	AC15	NC
E21	I/O	B12	PRA	N11	GND	W23	NC
E20	I/O	A11	I/O	N13	GND	A4	NC
D23	I/O	B11	I/O	M10	GND	C1	NC
D22	I/O	C11	I/O	L14	GND	A8	NC
A20	I/O	A10	I/O	L13	GND	A21	NC
D21	I/O	B10	I/O	L12	GND	J1	NC
D20	I/O	C10	I/O	L11	GND	AC3	NC
C22	GND	D10	I/O	L10	GND	C23	NC
C20	I/O	A9	I/O	K14	GND		
B21	I/O	B9	I/O	K13	GND		
B20	I/O	C9	I/O	K12	GND		
D19	I/O	D9	I/O	K11	GND		
C19	I/O	B8	I/O	K10	GND		
B19	I/O	C8	I/O	C3	GND		
A19	I/O	D8	I/O	B2	GND		
D18	I/O	B7	I/O	A1	GND		
C18	I/O	C7	I/O	AA3	GND		
B18	I/O	D7	I/O	AB2	GND		
A18	I/O	A6	I/O	AC1	GND		
D17	I/O	B6	I/O	AB22	GND		
C17	I/O	C6	I/O	AC23	GND		
B17	I/O	D6	I/O	B22	GND		

Package Mechanical Drawings

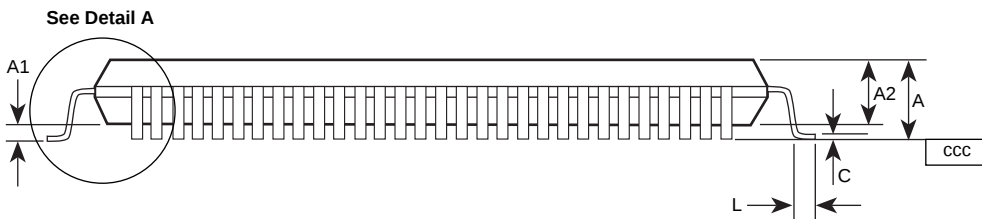
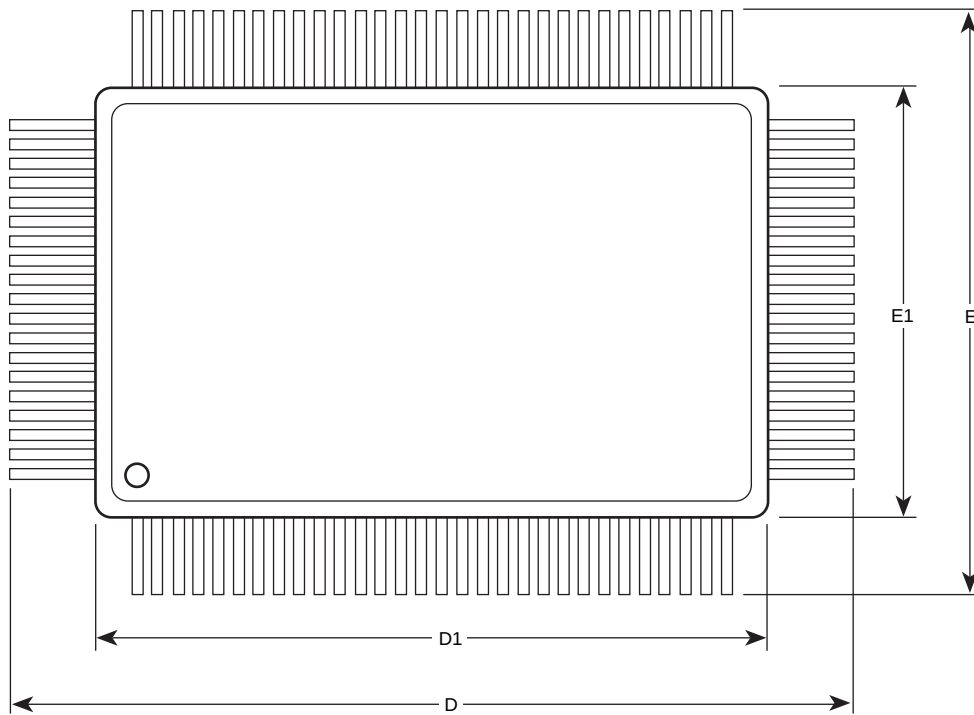
Plastic Quad Flatpack (PQFP, TQFP, VQFP)



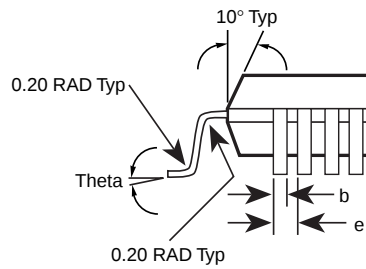
Package Mechanical Drawings (continued)

Plastic Quad Flatpack

Rectangular Package (PQFP)



Detail A



Plastic Quad Flat Packages (PQFP)

Jedec Equiv	PQFP 208 MO-143		
Dimension	Min	Nom	Max
A		3.70	4.10
A1	0.25	0.38	
A2	3.20	3.40	3.60
b	0.17		0.27
c	0.09		0.20
D/E	30.25	30.60	30.85
D1/E1	27.90	28.00	28.10
e	0.50 BSC		
L	0.50	0.60	0.75
ccc			0.10
Theta	0		7 deg
Diameter	19.82	20.32	20.82

Thin Quad Flatpacks (VQFP)

Jedec Equiv	VQFP 100 MO-136		
Dimension	Min	Nom	Max
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17		0.27
c	0.09		0.20
D/E	15.75	16.00	16.25
D1/E1	13.90	14.00	14.10
e	0.50 BSC		
L	0.45	0.60	0.75
ccc			0.10
Theta	0		7 deg

Notes:

1. All dimensions are in millimeters.
2. BSC—Basic Spacing between Centers.

Thin Quad Flatpacks (TQFP)

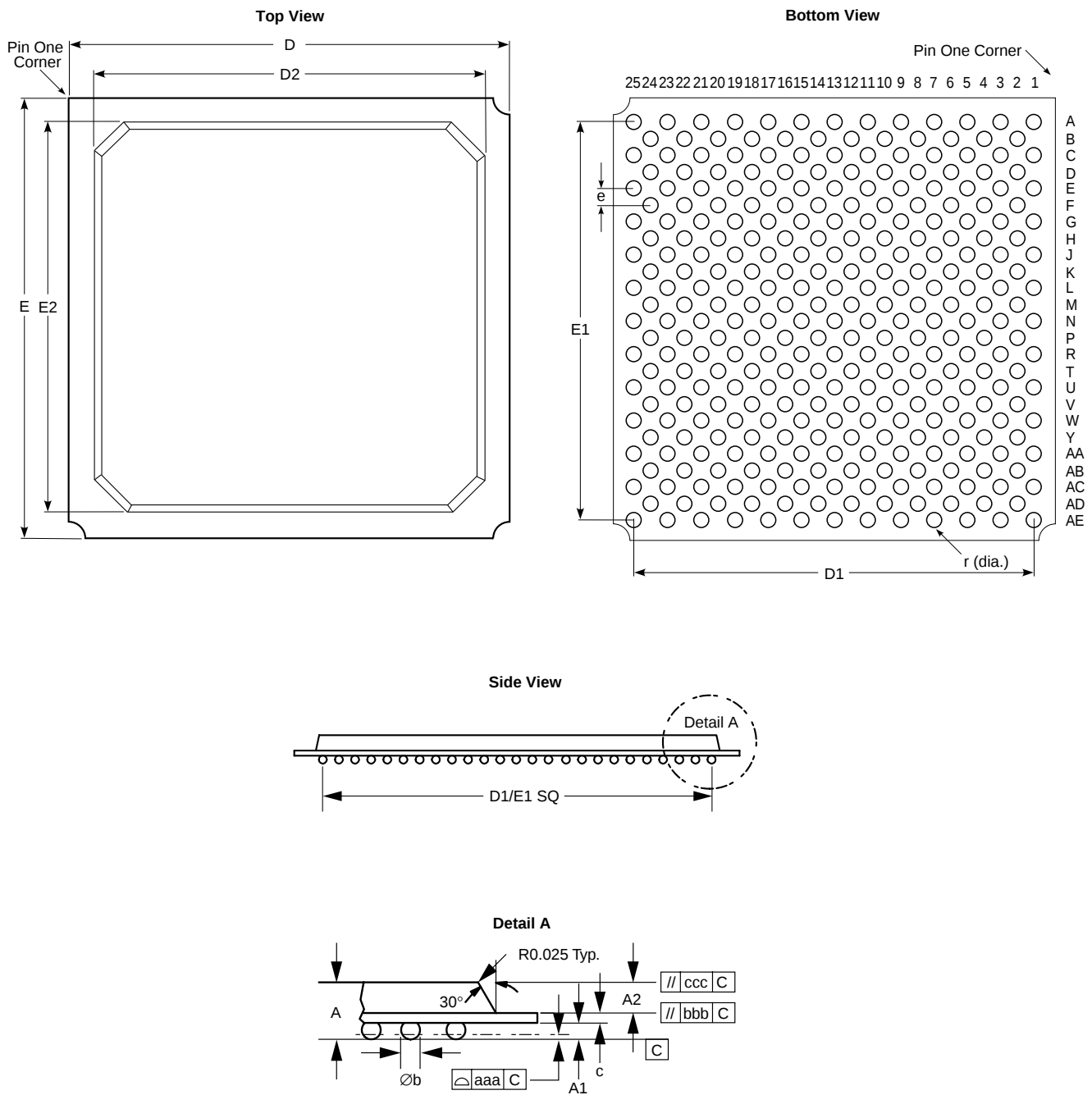
Jedec Equiv	TQFP 144 MO-136			TQFP 176 MO-136		
Dimension	Min	Nom	Max	Min	Nom	Max
A			1.60			1.60
A1	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45
b	0.17		0.27	0.17		0.27
c	0.09		0.20	0.09		0.20
D/E	21.75	22.00	22.25	25.75	26.00	26.25
D1/E1	19.90	20.00	20.10	23.90	24.00	24.10
e	0.50 BSC			0.50 BSC		
L	0.45	0.60	0.75	0.45	0.60	0.75
ccc			0.10			0.10
Theta	0		7 deg	0		7 deg

Notes:

1. All dimensions are in millimeters.
2. BSC—Basic Spacing between Centers.

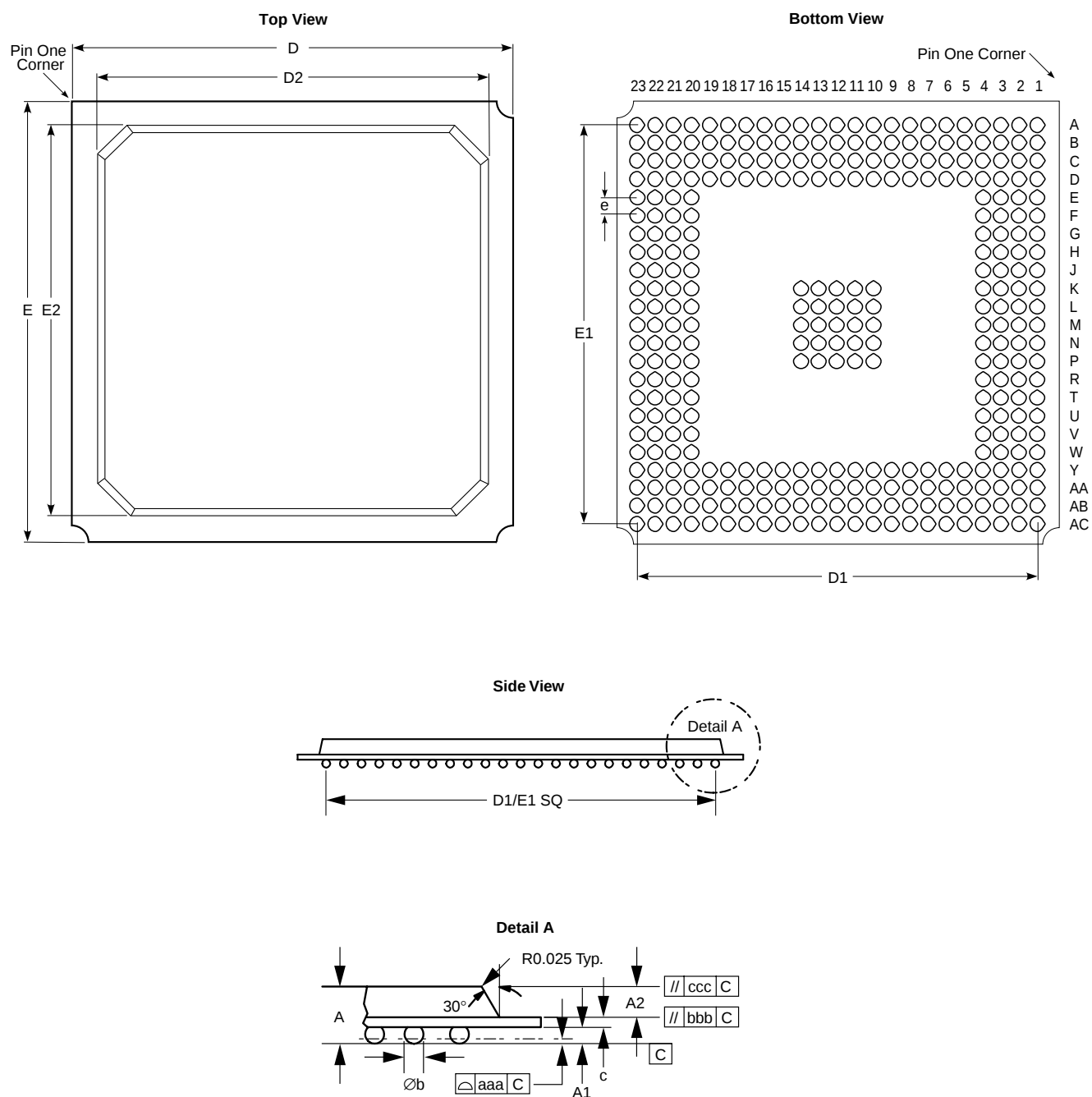
Package Mechanical Drawings (continued)

Plastic Ball Grid Array (BGA313)



Package Mechanical Drawings (continued)

Plastic Ball Grid Array (BGA329)



Plastic Ball Grid Array (PBGA)

JEDEC Equivalent	PBGA313			PBGA329		
Dimension	Min.	Nom.	Max.	Min.	Nom.	Max.
A	2.12	2.33	2.52	2.17	2.33	2.70
A1	0.50	0.60	0.70	0.50	0.60	0.70
A2	1.12	1.17	1.22	1.10	1.20	1.30
D	34.80	35.00	35.20	30.80	31.00	31.20
D1	30.48 BSC			27.94 BSC		
D2	29.50	30.00	30.70	27.90	28.00	28.10
E	34.80	35.00	35.20	30.80	31.00	31.20
E1	30.48 BSC			27.94 BSC		
E2	29.50	30.00	30.70	27.90	28.00	28.10
b	0.60	0.76	0.90	0.60	0.76	0.90
c	0.53	0.56	0.61	0.53	0.60	0.70
aaa			0.15			0.20
bbb			N/A			0.20
ccc			0.35			0.25
e	1.27 typ.			1.27 typ.		

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