

---

# **The ACEX Initiative**

**Low-Cost, High-Performance Solutions  
for the Communications Marketplace**

# Agenda

---

- ACEX Overview
- ACEX Applications
- The ACEX 1K Family
- The ACEX 2K Family
- The ACEX Advantage

# ACEX Overview

---

## ■ Communications Marketplace

- Provide Low-Cost, High-Performance Applications With a Programmable Solution for High-Volume Use

## ■ ACEX Fulfills This Need

- ACEX is a Broad-Based Initiative That Delivers Necessary Programmable Solutions
  - Architectures
  - Voltages
  - Feature Sets

# ACEX Applications

---

## ■ Communications Marketplace

- Volume Use in Price Sensitive Applications
  - Cable & xDSL Modems
  - Low-Cost Switches & Routers
  - Remote Access Concentrators
- High CAGR Applications Opportunities in this Marketplace

# ACEX Applications

---

- Cable Modems
- xDSL Modems
- Remote Access Systems
  - Remote Access Concentrators
- Private & Branch Access Routers
- Low-Cost Switches
- Low-Cost Line Cards
- Laser Printers
- PC Peripherals

# ACEX Applications

---

- xDSL Modems



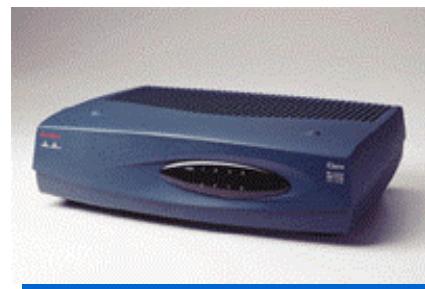
- Cable Modems



- Access Routers



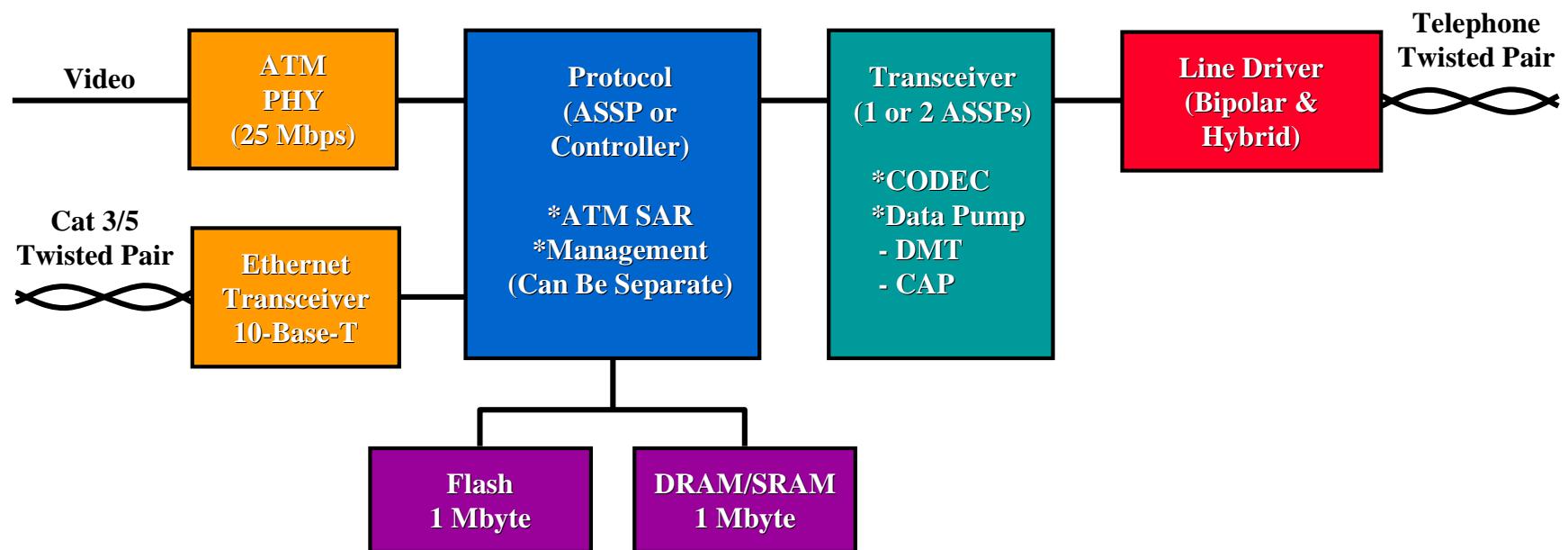
- Low Cost Ethernet LAN Switches



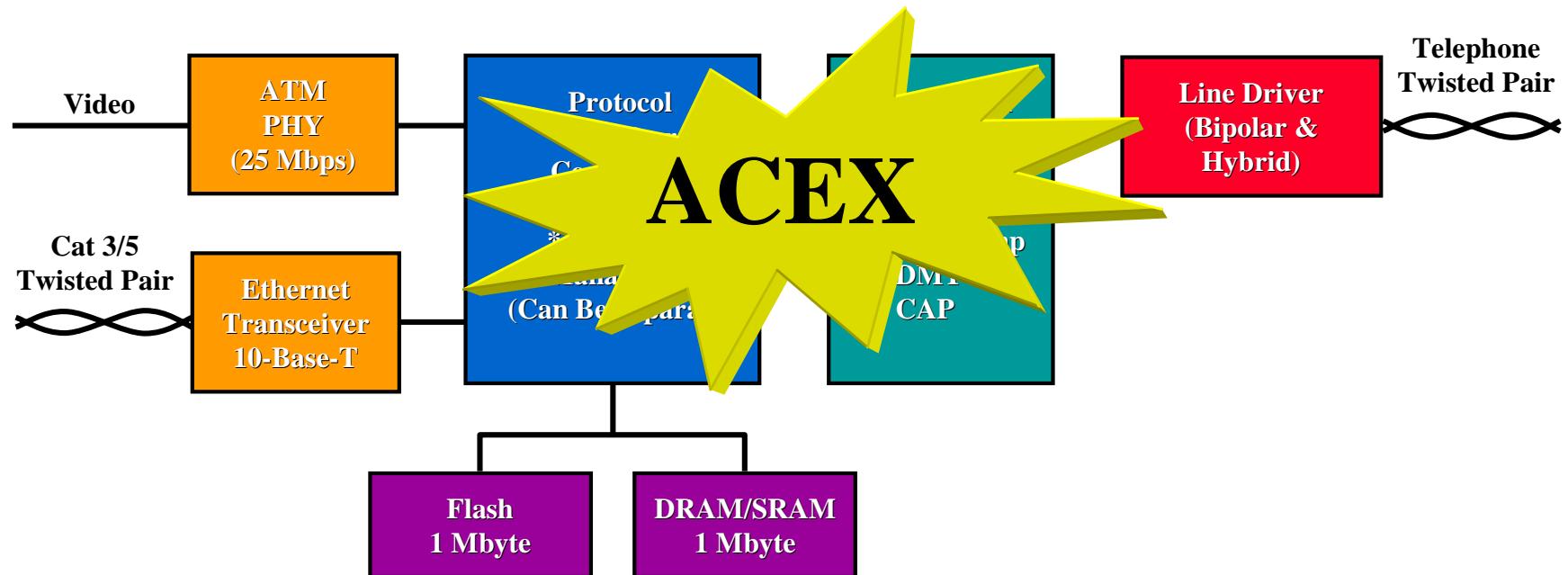
- Remote Access Concentrators



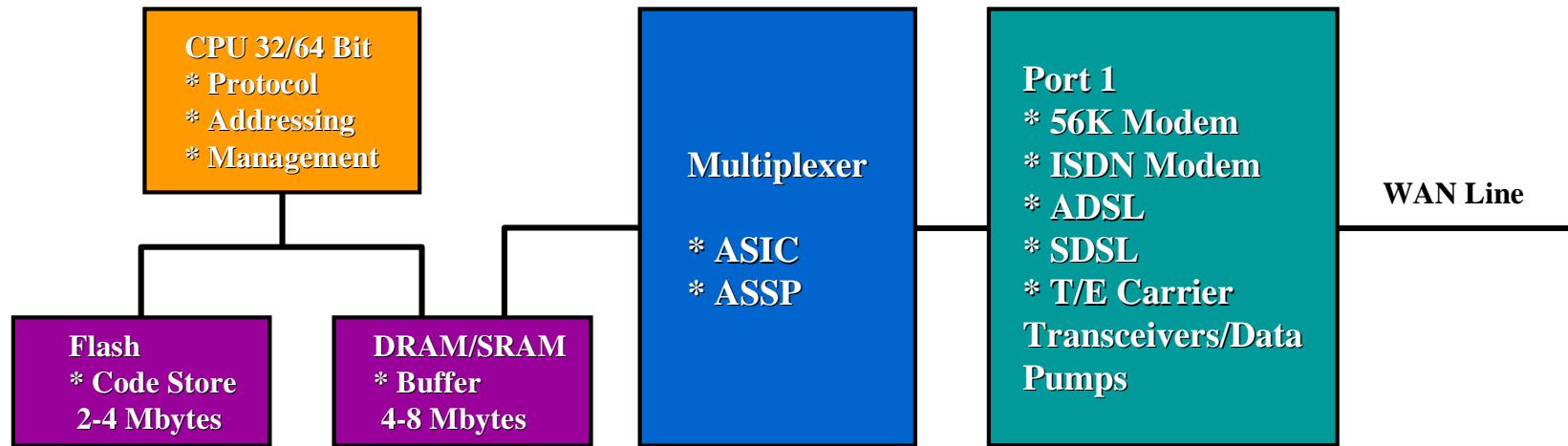
# ADSL Modem: Block Diagram



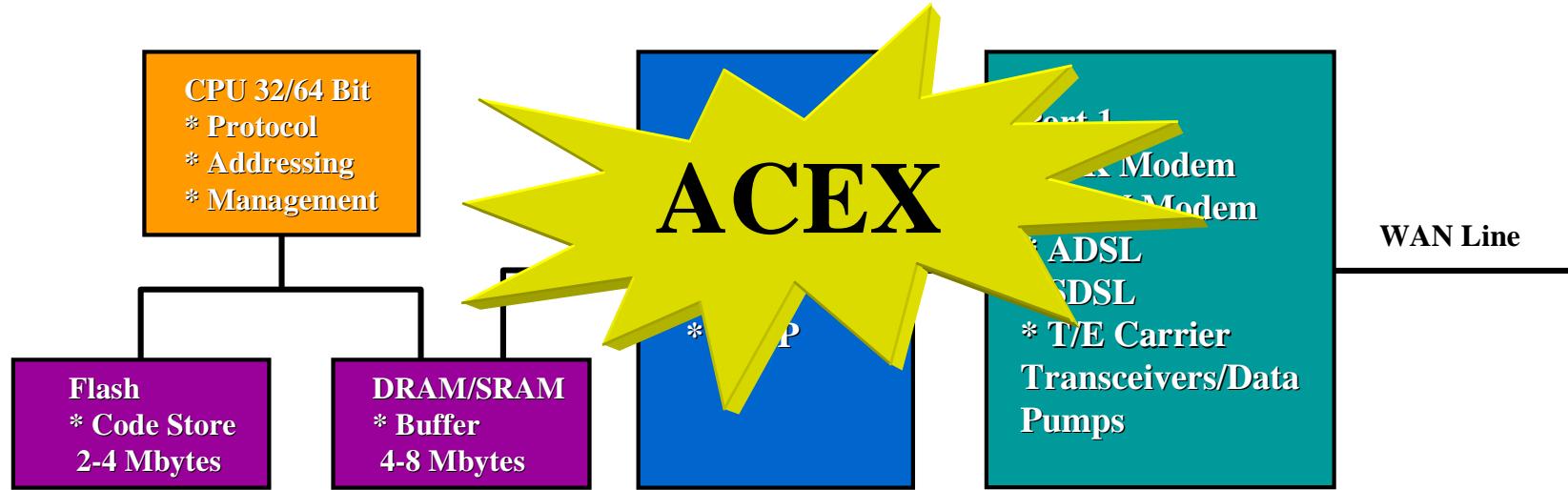
# ADSL Modem: Block Diagram



# Remote Access Controller: Block Diagram



# Remote Access Controller: Block Diagram



# The ACEX Products

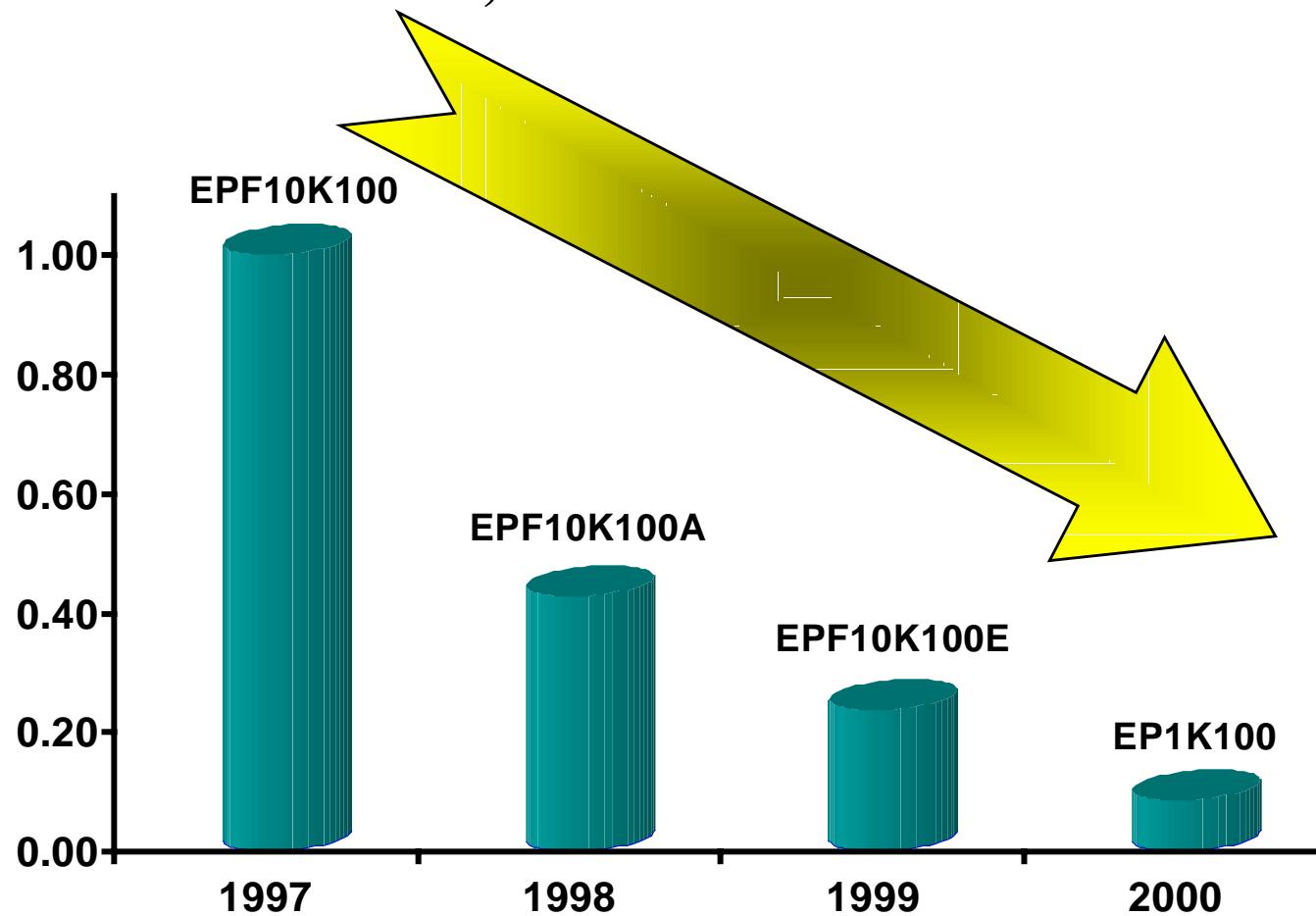
---

- Low-Cost, High-Performance Products
  - High-Volume Applications in the Communications Marketplace
- Multiple Families at Multiple Voltages
- Pricing
  - Establish Price Leadership in Low-Cost Marketplace

Low Price Leader

# The Altera Pricing Advantage

Normalized 100,000 Gate Device Volume Price



# ASIC Replacement

---

- ACEX Is The ASIC Replacement Solution
  - Cost Competitive with ASICs
  - All the Benefits of a Complete Programmable Solution
    - Fast Time-to-Market
    - Flexibility in Design
    - Reprogrammability
    - Advanced Development Tools
    - Drop-in Intellectual Property
  - No ASIC Risks. No ASIC NREs. No ASIC Restrictions.

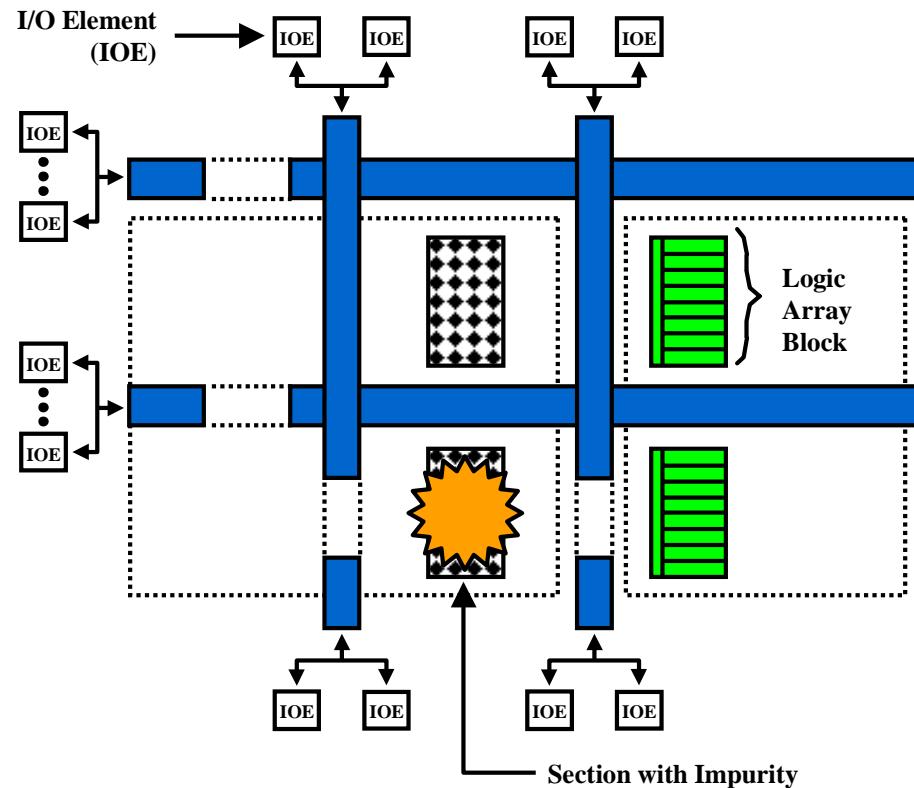
# ASSP Replacement

---

- Advanced Feature Sets Eliminate Specialized ASSPs
  - Advanced Capability PLLs
  - High-Speed FIFOs & Dual-Port RAM
  - Full 64-Bit, 66-MHz PCI Compliance
  - Advanced I/O Standards
  - MultiVolt I/O Capability
- Integrate ASSP Functionality into a Low-Cost PLD
  - Save Device Cost
  - Save Board Cost
  - Save Board Development Cost

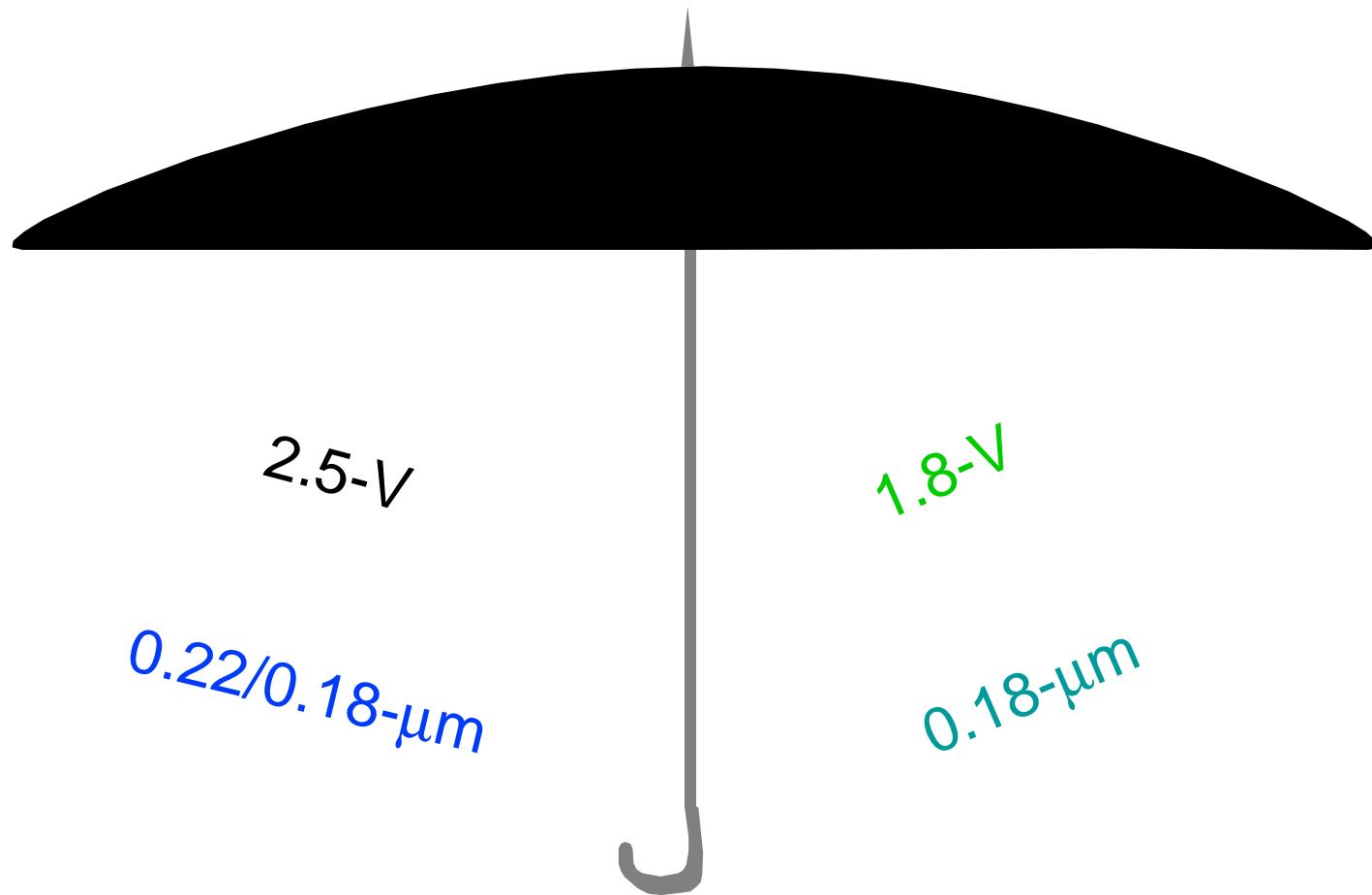
# Altera Redundancy Feature

- Altera-Patented Technology on Application to PLDs
- Significant Yield Improvement

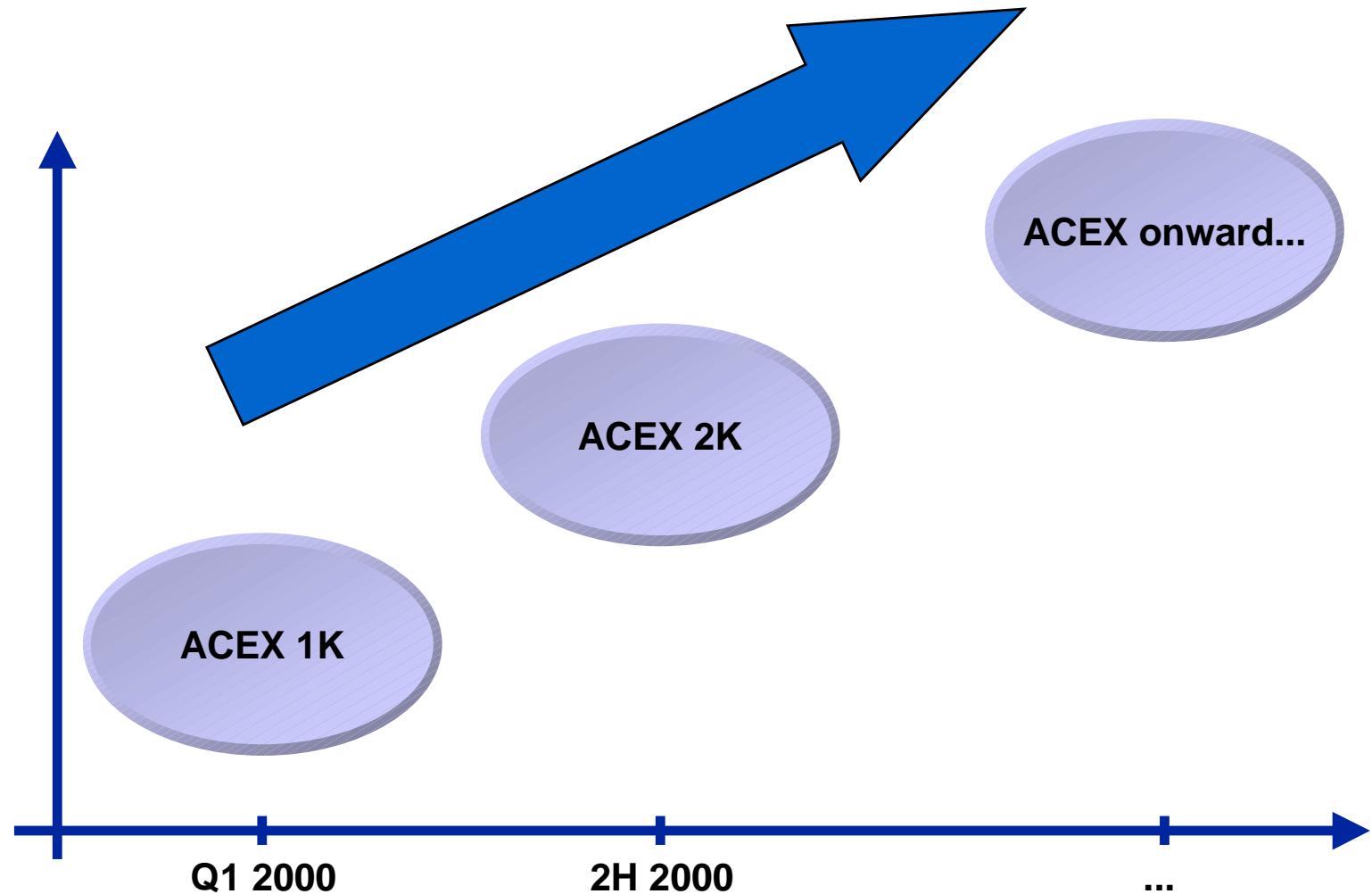


# The ACEX Product Umbrella

---



# The ACEX Roadmap



# The ACEX 1K Family

# The ACEX 1K Family

---

- 0.22/0.18- $\mu$ m, 5LM Hybrid Process
  - 2.5-V Core Operating Voltage
  
- Availability
  - Sample Availability in March, 2000
  - Software Support in MAX+PLUS II v9.6

# The ACEX 1K Family

---

## ■ The Altera Process Advantage

- Hybrid Process
  - 0.22- $\mu$ m Transistors
  - 0.18- $\mu$ m Metal Interconnect
  - Maintains 2.5-V Core Operating Voltage
  - Provides Key Cost Improvements
- Yield Improvements
  - Smaller Die Size Improves Yield
- Patented Redundancy Feature

# The ACEX 1K Family

---

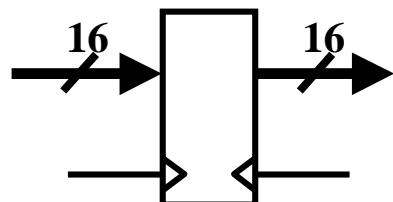
## ■ ACEX 1K Features

- 64-Bit, 66-MHz PCI Compliant
- PLL Support
  - ClockLock Synchronization Circuitry
  - ClockBoost Multiplication Circuitry
    - Simultaneous Clock Lock and Clock x2 Outputs
- Embedded Dual-Port Memory Blocks
  - 4 Kbit RAM Blocks
- MultiVolt™ I/O Interface
  - 5-Volt Tolerant I/O

# The ACEX 1K Feature Set

## Dual Port RAMs & FIFOs

Wr Data                            Rd Data



## PLL Capability

CLK

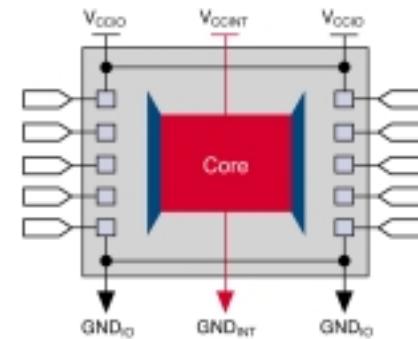
CLKx2

ClockLock

ClockBoost

ACEX  
1K

## MultiVolt I/O Interface



5-V Tolerant I/Os

## 64-Bit, 66-MHz PCI



# ACEX 1K Family Members

Feature	EP1K10	EP1K30	EP1K50	EP1K100
Typical Gates	10,000	30,000	50,000	100,000
Logic Elements	576	1,728	2,880	4,992
RAM Bits	12,288	24,576	40,960	49,152
User I/O Pins (Max.)	130	171	249	333
Package Options	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA <sup>1</sup>	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA <sup>1</sup>	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA <sup>1</sup> , 484-Pin BGA <sup>1</sup>	208-Pin PQFP, 256-Pin BGA <sup>1</sup> , 484-Pin BGA <sup>1</sup>
Available	Q3 '00	March	March	March

(1) 256- and 484-Pin Packages Are 1.0-mm FineLine BGA™

***Available in MAX+PLUS II v9.6***

# The ACEX Price Advantage

---

***ACEX Is The Low Price Programmable Leader***

ACEX	High-Volume Price
EP1K10	\$3.50
EP1K30	\$7.00
EP1K50	\$9.00
EP1K100	\$11.95

Note: End-2000 Pricing in High Volume Quantities

# The ACEX I/O Advantage

---

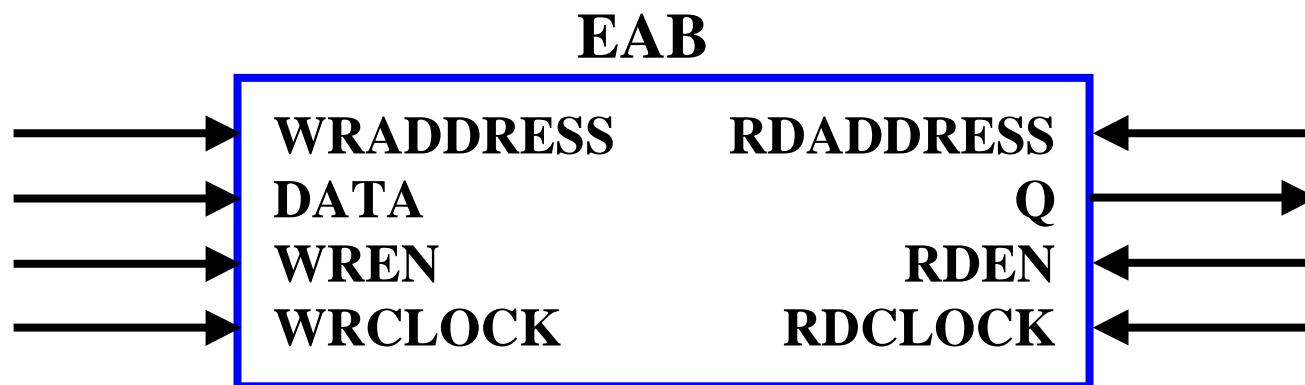
- Communications Applications Require High I/O Counts
  - Allows High Performance Communication
  - Wide Bandwidth Capabilities

Device	EP1K10	EP1K30	EP1K50	EP1K100
Max. I/O	130	171	249	<b>333</b>



# High-Performance Dual-Port RAM

- Independent Read/Write Ports
  - Synchronous/Asynchronous Access
  - 6.5-ns Access Time
- Wide Range of Configuration Options
  - 4 KBits/EAB for Flexibility
  - Width up to x16 for Maximum System Bandwidth
- Fast and Effective FIFO Implementation



# ClockLock - Improve I/O Performance

- ClockLock Increases I/O Performance

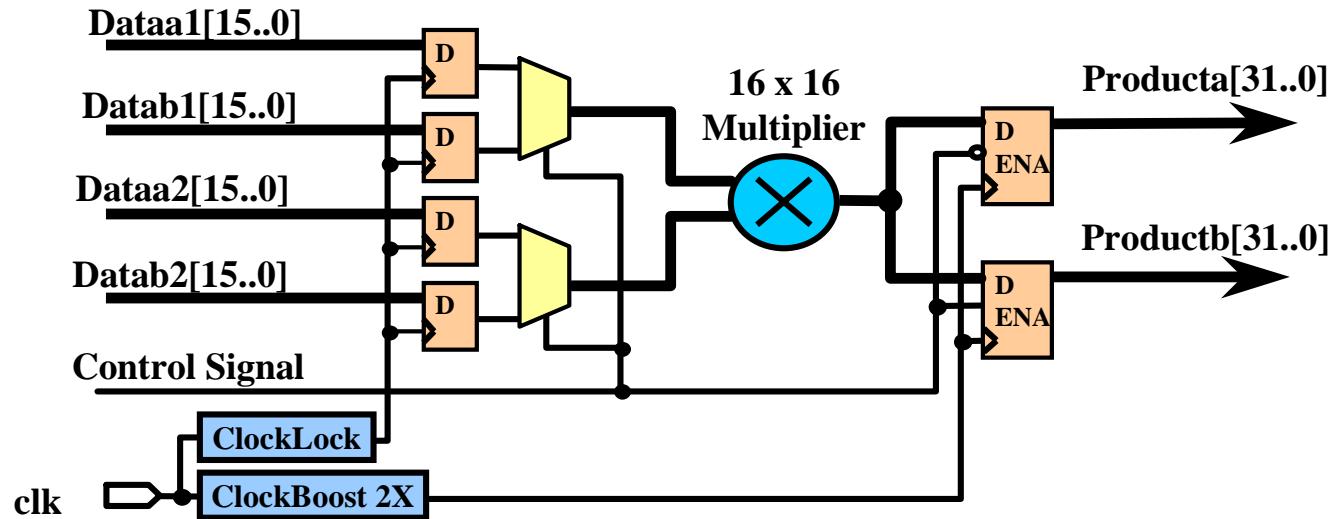
	T <sub>co</sub>	T <sub>su</sub>
<b>Without PLL</b>	5.2	2.0
<b>With PLL</b>	4.2	1.5

Improved Timing!

*Note: ACEX 1K data from MAX+PLUS II v9.6*

# ClockBoost - Time-Domain Multiplexing

- Multiplied Clock Used to Share Resources



Required LEs		
Design	Without ClockBoost	Without ClockBoost
Two 16 x 16 Multipliers	1,160	680
Four 16 x 16 Multipliers	2,320	873

# The ACEX 2K Family

# The ACEX 2K Family

---

- Advanced 0.18- $\mu$ m, 6LM Process
  - 1.8-V Core Operating Voltage
  - Altera Process Leadership
    - Volume Yields at Introduction via Excellent Defect Densities
- 20,000 to ~150,000 Gates
- Dual Port RAM Blocks
- Availability
  - Sample Availability in 2H '00
  - Software Support in Quartus only

# The ACEX 2K Family

---

## ■ ACEX 2K Features

- PCI-X Compliant
- 64-Bit, 66-MHz PCI Compliant
- Advanced Capability PLL
  - ClockLock Synchronization Circuitry
  - ClockBoost Multiplication Circuitry
    - Multiplication and Division by Factors as High as 133
  - ClockShift Phase & Delay Adjustment Circuitry
- Advanced I/O Standard Support
  - SSTL-2, SSTL-3, GTL+
  - HSTL, AGP, CTT
- Embedded Dual Port Memory Blocks

---

# The ACEX Advantage

# PCI Market Status

---

- PCI is the De Facto Bus Standard for Open Systems
  - Emerging I/O Standard for Embedded Applications
- 64-Bit, 66-MHz Required for High-Performance Systems
  - High-Performance Communications Applications
  - Gigabit Ethernet, Fiber Channel
  - High-end Systems Require 64-Bit Addressing
- PCI-X is the Next Generation Solution
  - Frequencies of up to 133 MHz



**ALTERA**<sup>®</sup>

# Altera PCI Solutions



## Megafuctions

32- & 64-Bit  
33- & 66- MHz  
PCI-X



## Devices

ACE X 1K  
ACE X 2K



**Verification**  
**Test Vectors**  
**Hardware Testing**



## Tools

MAX+PLUS II  
Quartus  
OpenCore Evaluation  
MegaWizard™ Plug-Ins  
Test Benches



# IP Solution Alternatives

---

- In-House ASIC Development
- Off-the-Shelf ASSP
- Programmable Logic Devices (PLDs)

Criteria	ASIC	ASSP	PLD
No NRE Cost	–	✓	✓
Fast Development Time	–	✓	✓
Fast Time-to-Market	–	✓	✓
Easy Customization	✓	–	✓
High Flexibility	✓	–	✓
Product Upgrade	–	–	✓

# Altera Megafunction Programs



- Sourced by IP Partners
- Wide Range of Functions
- Optimized for Altera

- Sourced by Altera
- Focused Set of Standard Functions
- Optimized for Altera

**Optimized IP for Altera Devices**

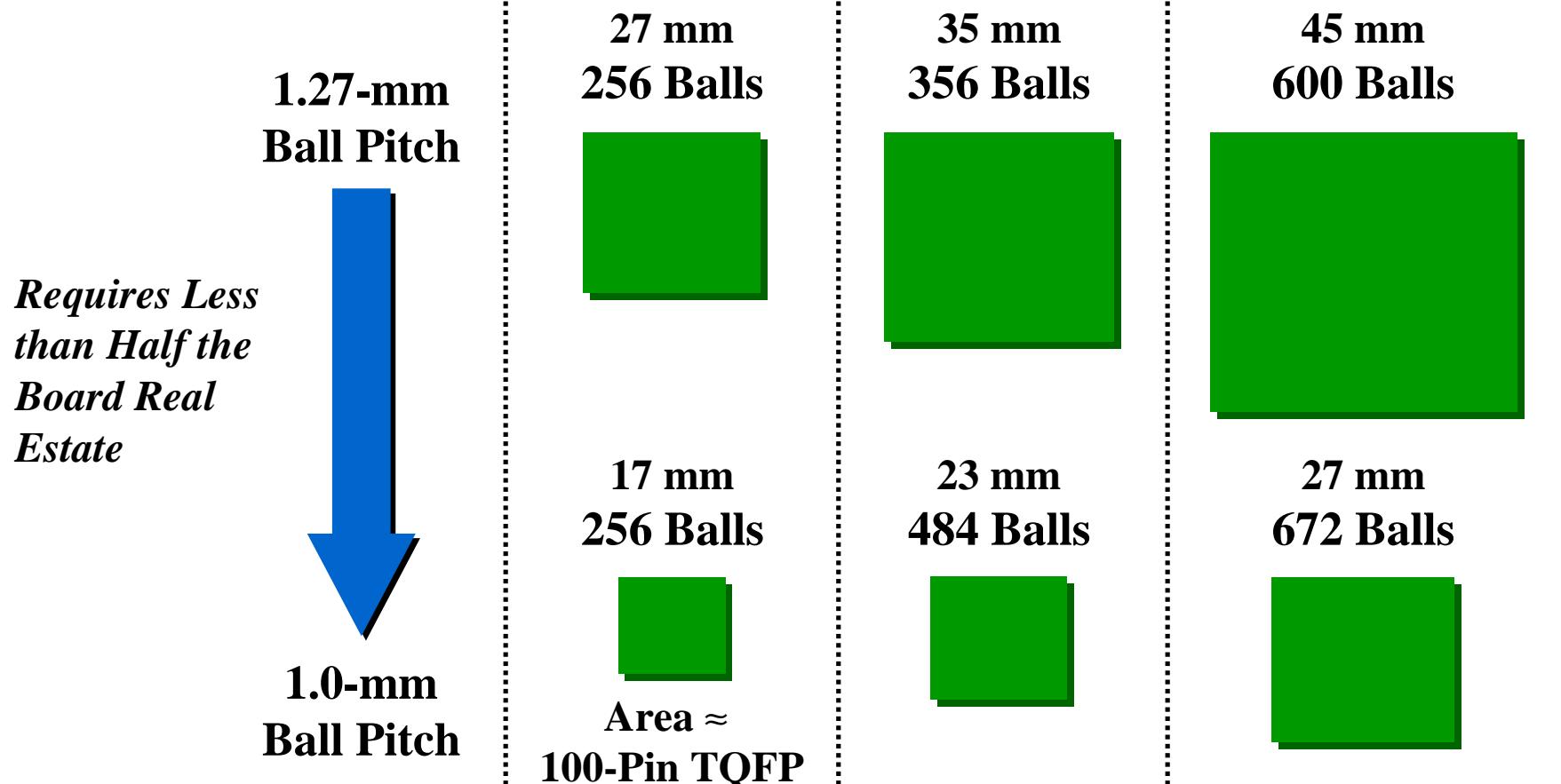
# 100+ Available IP Cores...

**10/100 Fast Ethernet MAC**  
**2910, 2910A Controllers**  
**29116A 16-Bit Processor**  
**49410 Controller**  
**68450 DMA Controller**  
**6850 ACIA**  
**8255A Interface**  
**16450/16550 UART**  
**6502 Processor**  
**Z80 Processor**  
**8031/8051 Processors**  
**8032/8052 Processors**  
**Adaptive Filters**  
**Convolutional Interleaver**  
**Cordic**

**Decimating Filter**  
**Digital Modulator**  
**Digital Data Acquisition Function**  
**DVB FEC Subsystem**  
**FFT/IFFT**  
**FIR Compiler**  
**FIR Filter**  
**HDLC**  
**IIC Master and Slave**  
**IIR Filter Library**  
**Image Processing Library**  
**Linear Feedback Shift Register**  
**Numerically Controlled Oscillator**  
**Packet over SONET Controller**  
**PCI Master/Target**

**PCI-PowerPC Bridge**  
**PowerPC Bus Arbiter**  
**PowerPC Bus Master**  
**PowerPC Bus Slave**  
**Reed-Solomon Decoder**  
**Reed-Solomon Encoder**  
**SDRAM Controllers**  
**SONET Byte Bus I/F**  
**Speedbridge FIFO**  
**Symbol Interleaver**  
**Telephony Tone Generation**  
**USB Function Controller**  
**USB Host Controller**  
**UTOPIA 2 Master/Slaves**  
**Viterbi Decoder**

# FineLine BGA Package Efficiency

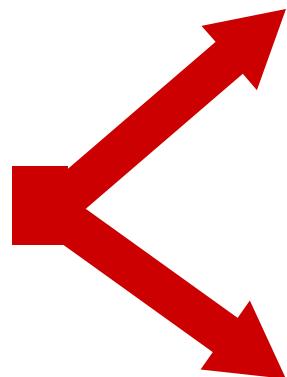
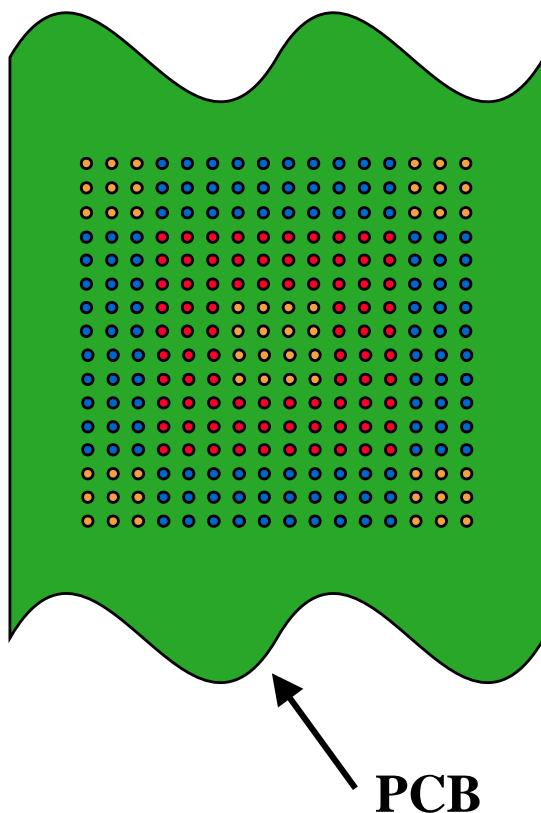


**Total BGA Solution**

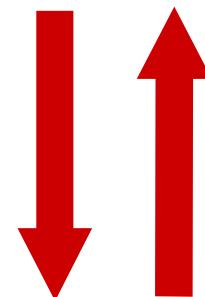
**ALTERA**<sup>®</sup>

# SameFrame™ Pin-Out Advantage

Layout PCB for  
484-Pin FineLine BGA



SameFrame  
Allows Package  
Migration in  
Either Direction



# ACEX Summary

---

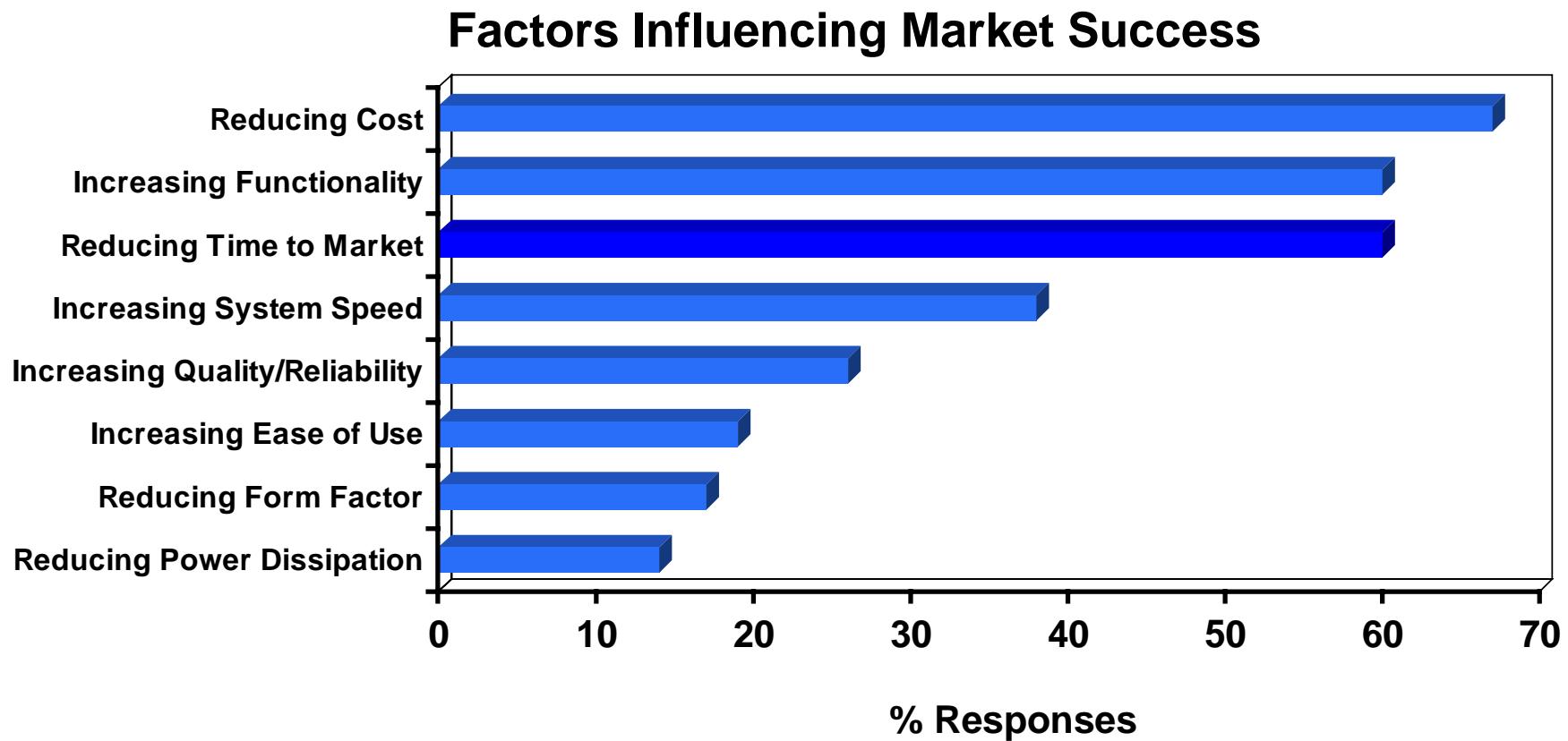
- The Premier Programmable Low-Cost Communications Solution
  - Low-Cost for High-Volume Use
  - High-Performance Capabilities for Communications Applications
  - Feature Rich Architectures
  - Software and Intellectual Property Leadership

***ACEX: The Low-Cost, High-Performance Communications Solution***

# Backup Slides

# Market Success Factors

■ ***Low Cost & Time-to-Market*** Critical for Success



Source: Dataquest  
© 2000 Altera Corporation

ALTERA®

# ACEX Time-to-Market Advantage

---

## ■ Quick to Prototyping

- In-System Design Verification
- Dramatically Reduced Simulation & Verification Time
- No Test Vectors Required
- No Prototype Lead-Times

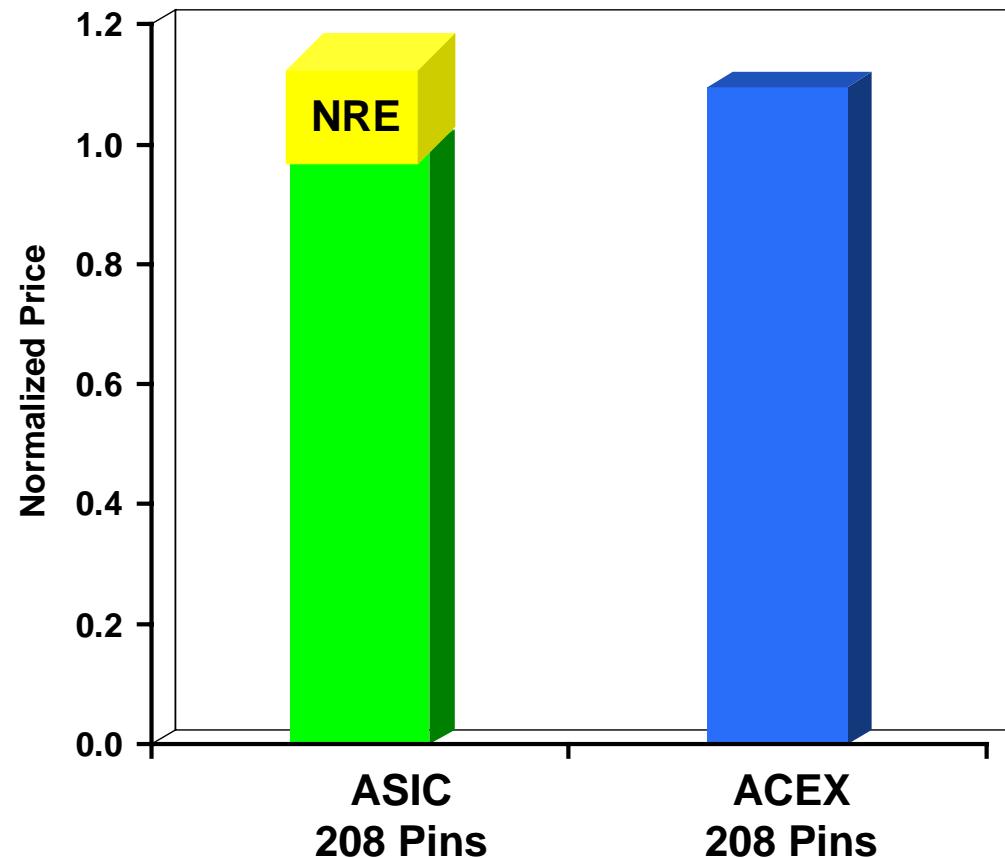
## ■ Quick to Production

- No Lengthy Sign-off Cycle
- No Production Lead Times



# Pricing vs. ASICs

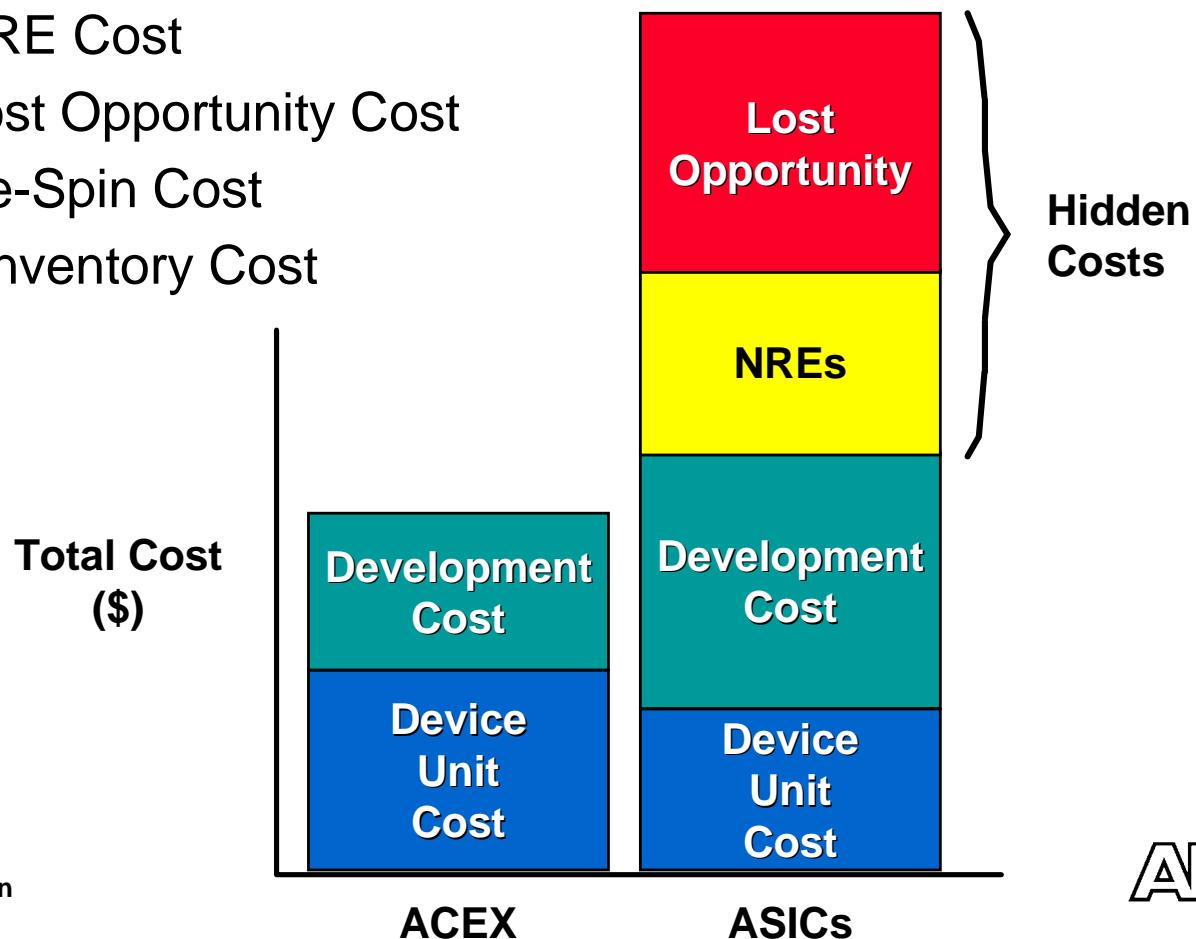
- Competitive with ASIC Unit Cost
- Benefits of Programmable Logic
  - **Faster to Market**
  - **Low Risk**
  - **No NRE**
  - **No Re-Spin Cost**
  - **Short Lead Times**
  - **Low Inventory Cost**



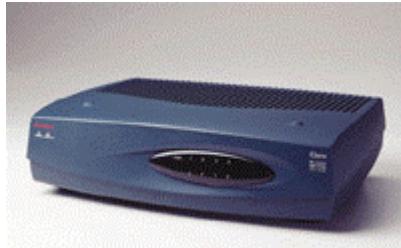
**ACEX Provides Low-Cost Flexibility**

# Total Cost vs. ASICs

- Total Cost = Device Unit Cost + Hidden Costs
- ACEX Minimizes Hidden Costs
  - No NRE Cost
  - No Lost Opportunity Cost
  - No Re-Spin Cost
  - Low Inventory Cost



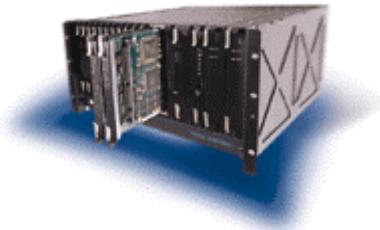
# ACEX & APEX Applications



Ethernet LAN Switch



Central Office Switch



Remote Access  
Concentrators



XDSL Modem



Layer 3 Switch



WAN Router

**ACEX**

**APEX**

# The ACEX Price Advantage

---

***ACEX Is The Industry's Lowest Price per Function***

ACEX	Cents/Logic Element
EP1K10	0.61
EP1K30	0.41
EP1K50	0.31
EP1K100	0.24

Note: End-2000 Pricing in High Volume Quantities

# ACEX Summary

## ■ ACEX Low-Cost Flexibility

Item	ASIC	ACEX
Device Cost	Low	Low
Total Cost	High	Low
Design Flow	✓	✓
No NRE	-	✓
Time-to-Market	-	✓
In-System Design Verification	-	✓
No Test Vectors	-	✓
No Re-Spin Cost	-	✓
Low Inventory Risk	-	✓