Timing Analyzer Guide

About This Manual

This manual describes Xilinx's Timing Analyzer program, a graphical user interface tool that performs static timing analysis of an FPGA or CPLD design.

The illustrations and examples in this user guide are based on the UNIX workstation version of the Timing Analyzer software. In most cases there are only minor differences in the appearance of the Timing Analyzer on all supported platforms. Any significant differences between platforms are described in this user guide.

Before using this manual, you should be familiar with the operations that are common to all Xilinx software tools: how to bring up the system, select a tool for use, specify operations, and manage design data. These topics are covered in the *Development System Reference Guide*.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this page. You can also directly access some of these resources using the provided URLs.

Resource	Description/URL
Tutorial	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answers Database	Current listing of solution records for the Xilinx software tools Search this database using the search function at http://support.xilinx.com/support/searchtd.htm

Resource	Description/URL
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Book	Pages from *The Programmable Logic Data Book*, which describe device-specific information on Xilinx device characteristics, including read-back, boundary scan, configuration, length count, and debugging http://support.xilinx.com/partinfo/databook.htm
Xcell Journals	Quarterly journals for Xilinx programmable logic users http://support.xilinx.com/xcell/xcell.htm
Tech Tips	Latest news, design tips, and patch information on the Xilinx design environment http://support.xilinx.com/support/techsup/journals/index.htm

Manual Contents

This manual covers the following topics.

- Chapter 1, “Introduction,” describes the Timing Analyzer’s function, place in the Xilinx design flow, key features, inputs and outputs, and the architectures with which it works. It also outlines the basic procedure for using the tool.
- Chapter 2, “Timing Analysis,” describes the basic path types and explains how the Timing Analyzer solves some basic design analysis problems.
- Chapter 3, “Getting Started,” describes how to access and exit the Timing Analyzer; how to use its menus, icons, Console window, dialog boxes, and filters; and how to use its online help facility.
- Chapter 4, “Using the Timing Analyzer,” explains how to perform most of the Timing Analyzer’s major functions.
- Chapter 5, “Menu Commands,” lists and describes all the menu commands available in the graphical interface.
- Chapter 6, “Command Line Syntax,” lists and describes all commands that you can enter in the Console window.
- Appendix A, “Glossary,” defines all the terms that you should understand to use the Timing Analyzer effectively.

Conventions

This manual uses the following typographical and online document conventions. An example illustrates each typographical convention.

Typographical

The following conventions are used for all documents.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: -100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement. However, braces "{ }" in Courier bold are not literal and square brackets "[ ]" in Courier bold are literal only in the case of bus specifications, such as bus [7:0].

  `rpt_del_net=`

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *design_name*

  - References to other manuals

    See the *Development System Reference Guide* for more information.

- Emphasis in text

  If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  edif2ngd [*option_name*] *design_name*

- Braces "{ }" enclose a list of items from which you must choose one or more.

  lowpwr ={**on**|**off**}

- A vertical bar " | " separates items in a list of choices.

  lowpwr ={**on**|**off**}

- A vertical ellipsis indicates repetitive material that has been omitted.

```
IOB #1: Name = QOUT'
IOB #2: Name = CLKIN'
.
.
.
```

- A horizontal ellipsis ". . ." indicates that an item can be repeated one or more times.

  allow block *block_name loc1 loc2* . . . *locn;*

Online Document

The following conventions are used for online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click the red-underlined text to open the specified cross-reference.
- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click the blue-underlined text to open the specified cross-reference.

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Chapter 4 Using the Timing Analyzer

Chapter 5 Menu Commands

Chapter 6 Command Line Syntax

Appendix A Glossary

Chapter 1

Introduction

The Timing Analyzer performs static timing analysis of an FPGA or CPLD design. The FPGA design must be mapped and can be partially or completely placed, routed or both. The CPLD design must be completely placed and routed. A static timing analysis is a point-to-point analysis of a design network. It does not include insertion of stimulus vectors.

The Timing Analyzer verifies that the delay along a given path or paths meets your specified timing requirements. It organizes and displays data that allows you to analyze the critical paths in your circuit, the cycle time of the circuit, the delay along any specified paths, and the paths with the greatest delay. It also provides a quick analysis of the effect of different speed grades on the same design.

The Timing Analyzer works with synchronous systems composed of flip-flops and combinatorial logic. In synchronous design, the Timing Analyzer takes into account all path delays, including clock-to-Q and setup requirements, while calculating the worst-case timing of the design. However, the Timing Analyzer does not perform setup and hold checks; you must use a simulation tool to perform these checks.

This chapter briefly describes the Timing Analyzer's function, place in the design flow, major features, inputs and outputs, and the architectures with which it works. It also outlines the basic procedure for using the tool. This chapter contains these sections.

- "Design Flow"
- "Inputs and Outputs"
- "Architectures"
- "Features"
- "Online Help"

Design Flow

You use the Timing Analyzer after mapping, placing, and routing, as shown in the following figure.

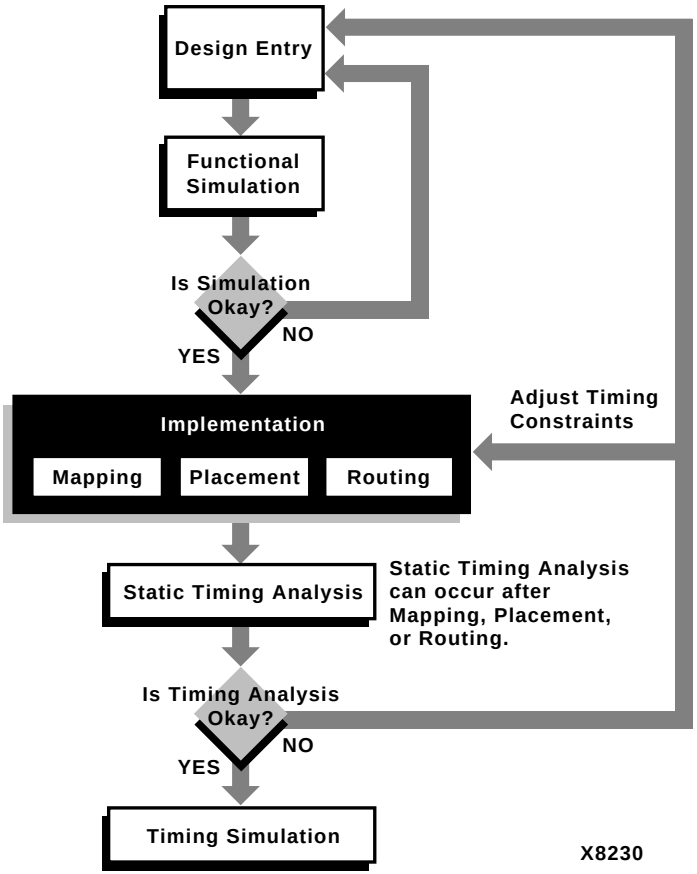


Figure 1-1 Timing Analyzer in the Design Flow

Inputs and Outputs

The Timing Analyzer has the following input and output capabilities:

- Accepts NCD design files and physical constraints files (PCF) output by the mapper for FPGAs
- Accepts VM6 (CPLD) design files output by the fitting software
- Loads macro files (XTM) as input
- Creates timing report (TWR) files as output
- Creates macro (XTM) files

Note: When you load a design, the Timing Analyzer also loads the default PCF file if it is present. The default PCF file is the physical constraints file with the same name and located in the same directory as the NCD file. You can load a different PCF file after the design is loaded. The order of the timing constraints in the PCF file is reflected in the Timing Analyzer reports. CPLD physical constraints information is contained in the VM6 file itself.

Architectures

You can use the Timing Analyzer with the following Xilinx devices:

- XC3000A™ / XC3000L™
- XC3100A™ / XC3100L™
- XC4000E™ / XC4000L™ / XC4000EX™ / XC4000XL™ / XC4000XV™ / XC4000XLA™
- XC5200™
- XC9500™ / XC9500XL™
- Spartan™ / SpartanXL™ / Spartan2™
- Virtex™

Features

The Timing Analyzer offers the following interface, report, filters, macro, and analysis interrupt features.

Interface

You can issue Timing Analyzer commands from the menus, toolbar, or Console window. You can also activate commands by running macros. The instructions in this user guide use only the menu commands or toolbar buttons, but the equivalent command-line syntax is given in the "Command Line Syntax" chapter.

Reports

The Timing Analyzer can create the following reports.

- Timing Constraints Analysis report compares design performance to the timing constraints.
- Advanced Design Analysis report displays the results of analyzing the constraints specified in the constraints file for FPGAs. If no constraints are specified, this report displays the maximum clock frequencies for all clocks in the design and the worst-case timing for all clock paths. For CPLDs, it displays all external synchronous path delays which include: pad-to-pad (t_{PD}), clock pad-to-output pad (t_{CO}), setup-to-clock-at-the-pad (t_{SU}), and internal clock-to-setup (t_{CYC}) paths.
- Custom Analysis report contains a detailed analysis of all specified paths and includes the worst-case path delays for all paths in the design. You can filter this report.
- Clocks report lists the names of all clocks in the design.
- Settings report lists the current settings set with commands in the Path Filters and Options menus.
- Query Nets report displays net delay information. (FPGA only)
- Query TimeGroups displays time group information. (FPGA only)

The content of these reports is described in the "Using the Timing Analyzer" chapter.

Path Filtering Commands

You can customize Timing Analyzer reports by specifying filters in the dialog boxes accessed through the commands in the Path Filters menu. The Reset Path Filters command resets the path filters to

default settings. The Path Filters menu contains the Timing Constraint Filters, Custom Filters, and Common Filters submenus which have the following functionality:

- Timing Constraint Filters commands affect only the Timing Constraints Analysis and Advanced Design Analysis reports.
- Custom Filters commands deal with specific paths whose starting points and ending points you can define. These commands apply to the Custom Analysis reports.
- Common Filters commands exclude or include paths with specific nets and control path tracing. These commands apply to the Timing Constraints Analysis, Advanced Design Analysis, and Custom Analysis reports.

Macros

You can create macros that execute multiple Timing Analyzer commands in one step. Macros are script files for running Timing Analyzer commands and options. The Console window records all the commands that you execute in any Timing Analyzer session. After entering the desired series of commands in this window, you can copy and paste the sequence into a macro document, save the macro document, and run it.

Analysis Interrupt

The commands in the Analyze menu have an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears. Clicking the button, the Esc key, or the Enter/Return key stops analysis. A report is not generated or displayed.

Online Help

The Timing Analyzer offers both context-sensitive help and a Help menu. See the “Obtaining Help” section of the “Getting Started” chapter for more information on the online help and instructions for accessing it.

Chapter 2

Timing Analysis

This chapter explains some of the concepts involved in static timing analysis and how to use the Timing Analyzer to resolve key analysis issues.

Xilinx software tools support two different methodologies of implementing timing analysis. For FPGAs, timing is analyzed through user-defined constraints specified with Timing Analyzer commands and filters. The commands in the Timing Constraints Filters submenu help you customize your analysis. See the "Timing Constraint Filters Submenu (Path Filters Menu)" section of the "Menu Commands" chapter and the *XILINX Software Conversion Guide from XACTstep v5.x.x to XACTstep vM1.x.x* for more information. CPLDs use system-defined paths for timing analysis. These paths are selected with commands in the Custom Filters submenu. See the "Custom Filters Submenu (Path Filters Menu)" section of the "Menu Commands" chapter for more information on these commands.

This chapter contains these main sections.

- "Basic Path Types"
- "Design Analysis Issues"

Basic Path Types

After you implement your design, you can use the Timing Analyzer to calculate your design's system performance, which is limited by seven basic types of timing paths. Each of these paths goes through a sequence of routing and logic. Because these path delays are affected by the results of the placement and routing that implement the design connectivity, these sequences can vary.

Before you read the Timing Analyzer reports, read the following sections for a description of the basic path types.

Clock to Setup

A clock-to-setup path starts at flip-flop clock inputs and ends at non-clock flip-flop register inputs, D or T, or the receiving flip-flop's t_{SU}, where that pin has a setup requirement before a clocking signal. Along the way, it propagates through the flip-flop Q output and any number of levels of combinatorial logic. It includes the clock-to-Q delay of a flip-flop, the path delay from that flip-flop to the next flip-flop, and the setup requirement of the next flip-flop.

The clock-to-setup path time is the maximum time required for the data to propagate through the source flip-flop, travel through the logic and routing, and arrive at the destination before the next clock edge occurs. When these flip-flops are clocked by the same clock, the delay on this path is equivalent to the cycle time of the clock. The following figures show a clock-to-setup path which uses the same clock. The "Clock-to-Setup Path (Same Clock) with Timing Diagram" figure also shows a timing diagram describing the path.

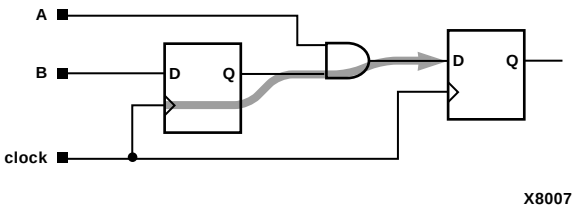


Figure 2-1 Clock-to-Setup Path

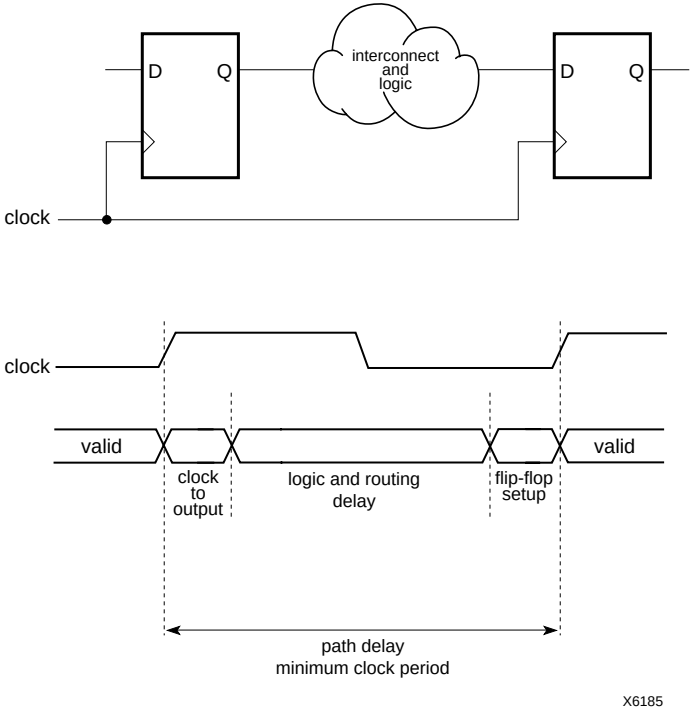


Figure 2-2 Clock-to-Setup Path (Same Clock) with Timing Diagram

Source and destination flip-flops can be clocked by the same clock on different clock edges. In these cases, the path delay limits the minimum clock high or clock low time as shown in the following two figures.

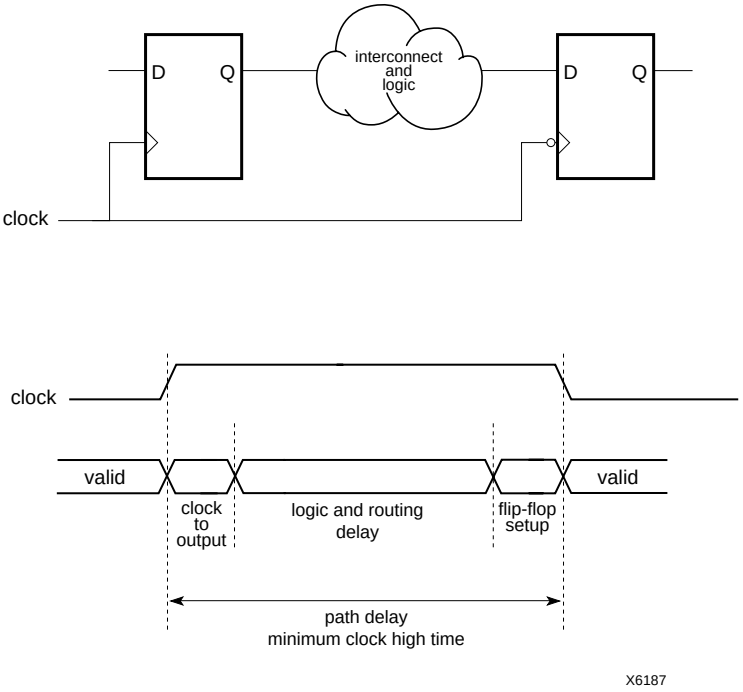


Figure 2-3 Clock-to-Setup Path (Rising to Falling Edge)

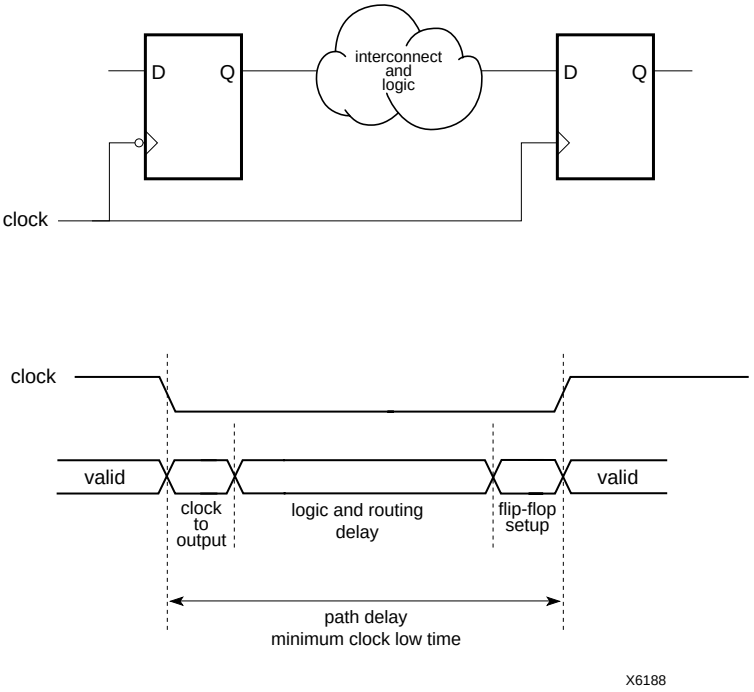


Figure 2-4 Clock-to-Setup Path (Falling to Rising Edge)

If the source and destination are clocked by different clock nets, the clock net on the destination must have a clock period greater than the path delay. The PERIOD constraints allow the Timing Analyzer to use the target flip-flop period for the delay path value. The following figure shows a path of this type.

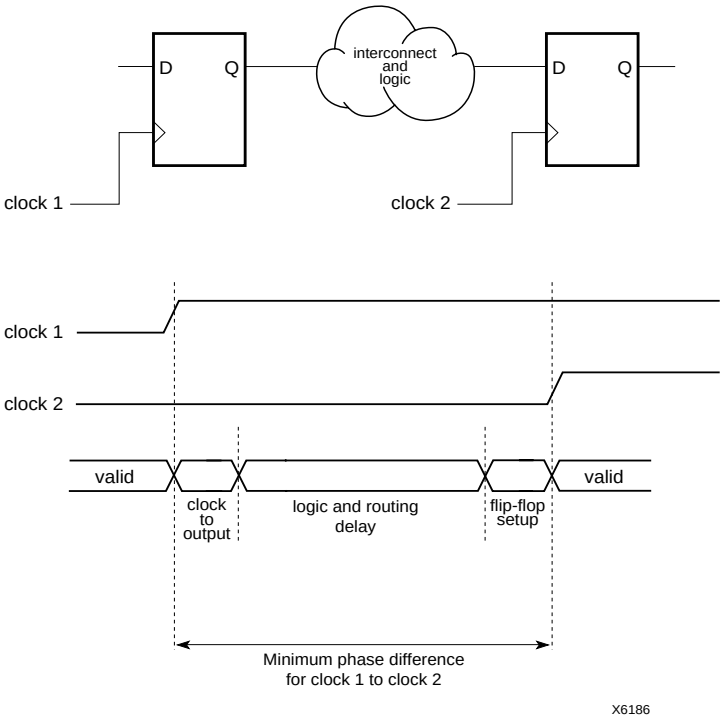


Figure 2-5 Clock-to-Setup Path (Different Clocks)

Clock-to-setup paths do not propagate from the flip-flop Q output through another flip-flop clock or asynchronous Set and Reset input as shown in the next figure. These paths are also broken at bidirectional pins.

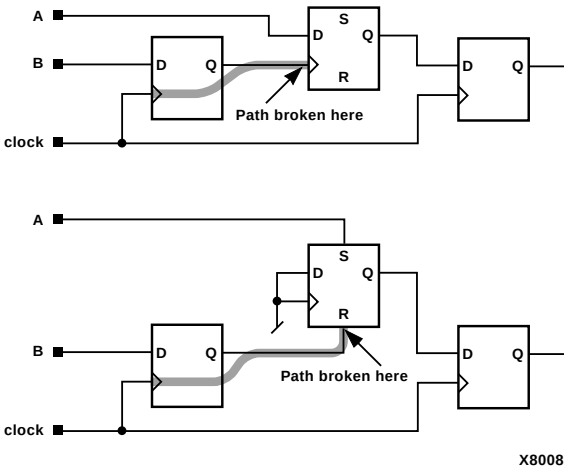


Figure 2-6 Not Propagating Through Asynchronous Set/Reset

Clock to Pad

A clock-to-pad path starts at a clock input of a flip-flop, propagates through the flip-flop Q output and any number of levels of combinatorial logic, and ends at an output pad. It includes the clock-to-Q delay of the flip-flop and the path delay from that flip-flop to the chip output. The clock-to-pad path time is the maximum time required for the data to leave the source flip-flop, travel through logic and routing, and leave the chip. When using the OFFSET constraint, the clock path is also used in the path delay. The following figure illustrates a clock-to-pad path, along with a timing diagram describing the path.

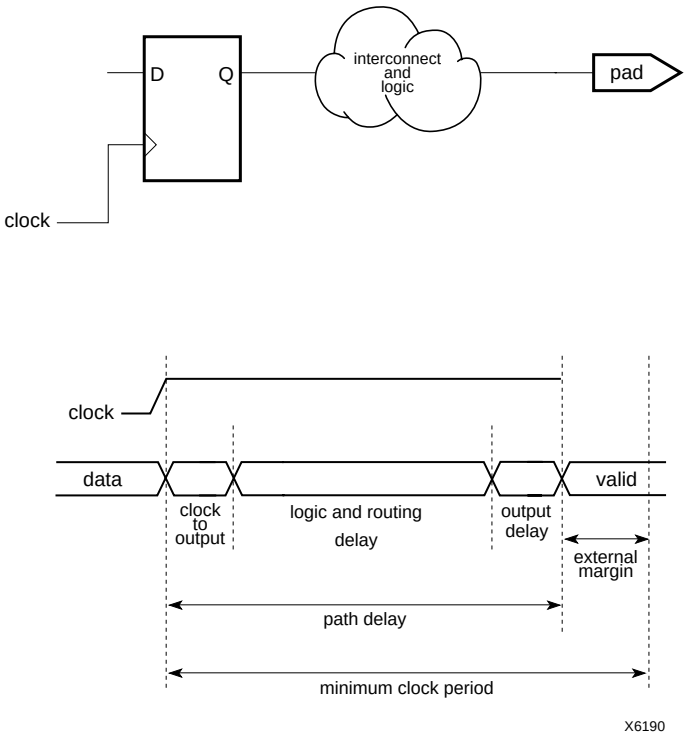


Figure 2-7 Clock-to-Pad Path

Clock-to-pad paths also trace through the enable inputs of tristate controlled pads, as shown in the next figure.

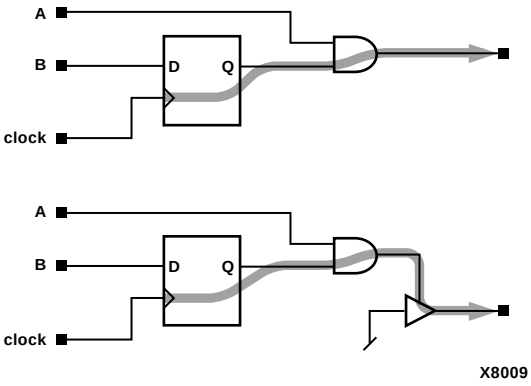


Figure 2-8 Through Tristate Controlled Pads

Clock-to-pad paths do not propagate from the Q output of a flip-flop through the clock of another flip-flop or asynchronous Set and Reset input as shown in the following figure. These paths are also broken at bidirectional pins.

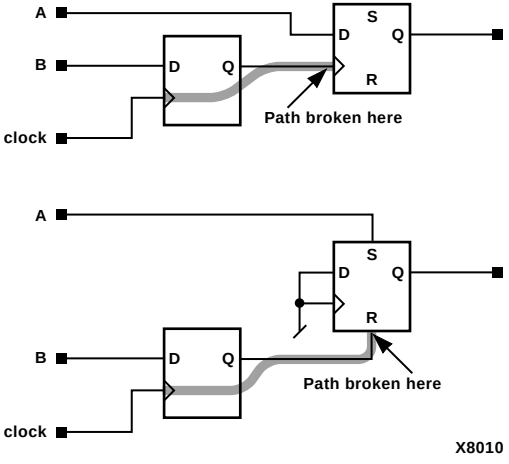


Figure 2-9 Clock-to-Pad Path Broken Through Set/Reset Inputs

Paths Ending at Clock Pin of Flip-Flops

A clock input path starts at a chip input or output. It propagates through any number of levels of combinatorial logic and ends at any clock pin on a flip-flip or latch enable. These paths do not propagate through flip-flops. The clock input path time is the maximum time required for the signal to arrive at the flip-flop clock input. Clock input paths help to determine system-level design timing.

The clock input time is the maximum time only; the Timing Analyzer currently does not calculate minimum clock times.

The next figure shows a clock input path.

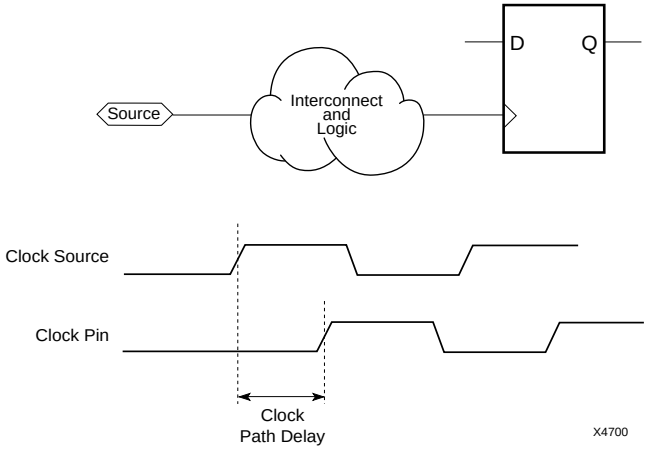


Figure 2-10 Paths Ending at Clock Pin of Flip-Flops

Setup to Clock at the Pad

A setup-to-clock-at-the-pad path starts at an input pad, propagates through input buffers and any number of levels of combinatorial logic, and ends at a flip-flop D/T input, which includes the receiving flip-flop's t_{SU}. This path does not propagate through flip-flops and is also broken at bidirectional pins.

This delay reports t_{SU} for data inputs relative to global or product term clock inputs. It is calculated according to the following formula for global and product term clocks.

```
tSU = Pad to Setup - Path Ending at Clock Pin of Flip-
Flop
```

Global clock paths start at global clock pads, propagate through global clock buffers and end at a flip-flop clock pin. Product term clock paths start at input pads, propagate through a single level of logic implemented in a clock product term, and end at the flip-flop clock pin. All three clock-at-the-pad paths are shown in the next figure.

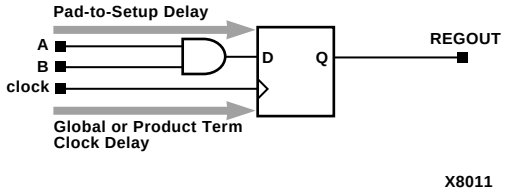


Figure 2-11 Setup-to-Clock-at-the-Pad Path

Clock Pad to Output Pad

A clock-pad-to-output-pad path starts at input pads and trace through all paths that include a flip-flop clock input (except when that path includes a flip-flop asynchronous Set/Reset input) before ending at an output pad. Clock-pad-to-output-pad paths trace through tristate controlled pad enable inputs.

Pad to Pad

A pad-to-pad path starts at an input pad of the chip, propagates through one or more levels of combinatorial logic, and ends at an output pad of the chip. Combinatorial paths also trace through the enable inputs of tristate controlled pads. The pad-to-pad path time is the maximum time required for the data to enter the chip, travel through logic and routing, and leave the chip. It is not controlled or affected by any clock signal. A pad-to-pad path, along with a timing diagram describing the path is displayed in the following figure.

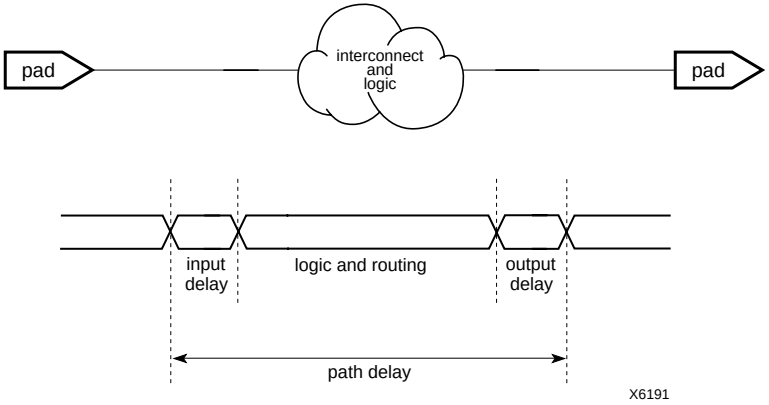


Figure 2-12 Pad-to-Pad Delay

Combinatorial paths are not traced through flip-flops. These paths are also broken at bidirectional pins. A second representation is shown in the next figure.

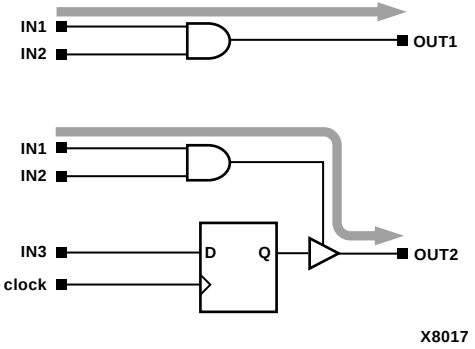


Figure 2-13 Pad-to-Pad Path

Pad to Setup

A pad-to-setup path starts at an input pad of the chip and ends at a D/T input to a flip-flop, latch, RAM, or the receiving flip-flop's t_{SU}, wherever there is a setup time against a control signal. Along the way, it propagates through input buffers and any number of combinatorial logic levels. Pad-to-setup paths do not propagate through flip-flops and are broken at bidirectional pins. The pad-to-setup path time is the maximum time required for the data to enter the chip, travel

through logic and routing, and arrive at the output before the clock or control signal arrives. A pad-to-setup path and timing diagram is shown in the following figure.

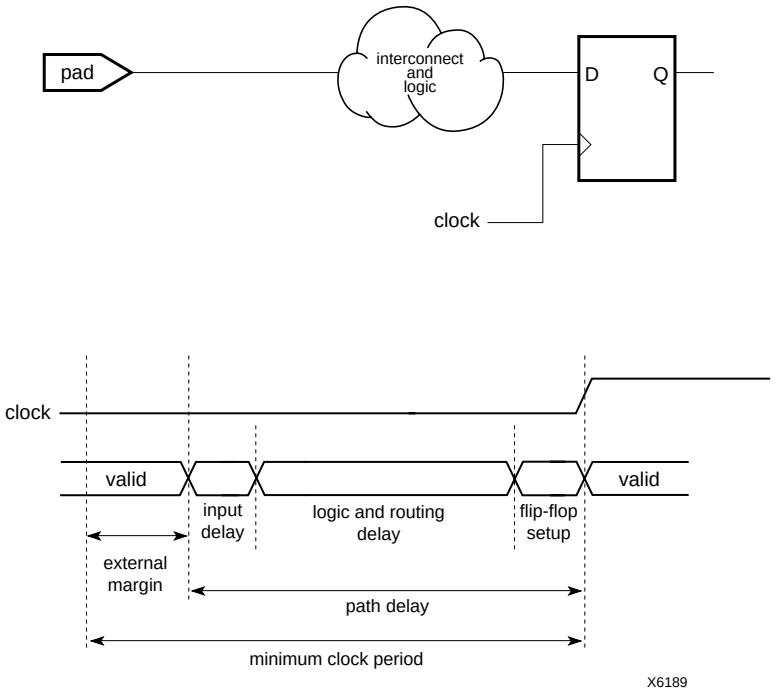


Figure 2-14 Pad-to-Setup Path

Design Analysis Issues

The Timing Analyzer can help you resolve some of the most frequently encountered design problems. This section describes common problems and solutions.

Feedback Loops

Asynchronous feedback paths in a design can cause many paths to be reported that may not actually be timing problems. The most common cases are feedback paths through asynchronous Set or Reset to banks of flip-flops, like a state machine or a counter. Another example is the construction of latches from function generators, which are built using asynchronous feedback paths.

To exclude specific nets that create feedback paths, such as an illegal-state Reset logic loop for a state machine, you can use the Exclude Paths with Nets command to exclude any paths that contain those nets from the timing report.

With the Control Path Tracing command, you can control some asynchronous points through logic; for example, you can exclude the asynchronous Reset of a flip-flop or TBUF input to output.

Timing Constraints

If you entered timing constraints before compiling your design with the mapper, you can use the Timing Analyzer to verify whether your constraints were met. The following example of portions of a Timing Analysis report shows how the Timing Analyzer finds paths that did not meet timing constraints; five errors occurred and three constraints were not met.

```
================================================================================
Timing constraint: TS01 = MAXDELAY FROM TIMEGRP "FFS" TO TIMEGRP "FFS"
2000.000000 pS PRIORITY 0 ;
 1 item analyzed, 1 timing error detected.
 Maximum delay is   3.340ns.
--------------------------------------------------------------------------------
Slack:    -1.340ns path $1N11 to $1N11 relative to
           2.000ns delay constraint

Path $1N11 to $1N11 contains 2 levels of logic:
Path starting from Comp: CLB.K (from $1N19)
To                   Delay type         Delay(ns)  Physical Resource
                                                   Logical Resource(s)
-------------------------------------------------  --------
CLB.XQ               Tcko                  1.830R  $1N11
                                                   $1N11
CLB.F2               net (fanout=2)     e  0.380R  $1N11
CLB.K                Tick                  1.130R  $1N11
                                                   $1N15
                                                   $1N11
-------------------------------------------------
Total (2.960ns logic, 0.380ns route)       3.340ns (to $1N19)
      (88.6% logic, 11.4% route)
.
.
.
```

```
3 constraints not met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock ck1_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    6.202(R)|            |
start_i        |    2.213(R)|    0.000(R)|
---------------+------------+------------+
.
.
.


Table of Timegroups:
--------------------
TimeGroup PADS:
BELs:
 OUT  D    C    CLR

TimeGroup FFS:
BELs:
 $1N11


Timing summary:
---------------

Timing errors: 5  Score: 15874

Constraints cover 5 paths, 0 nets, and 5 connections (100.0% coverage)


Design statistics:
   Maximum path delay from/to any node:  10.716ns


Analysis completed Wed Feb 24 14:29:35 1999
--------------------------------------------------------------------------------
```

Clock Skew

The Timing Analyzer can report clock skew, which is the difference between the time a clock signal arrives at the source flip-flop in a path and the time it arrives at the destination flip-flop on the same clock net. Clock skew occurs most often when global routing is not used to route clock nets, because other routing is less predictable. The arrival of clock signals at different times can affect the required clock period. This section describes negative and positive clock skew and how the Timing Analyzer reports clock skew.

Negative Clock Skew

When the destination is clocked before the source, the clock skew is called negative clock skew. Negative clock skew means that the clock period must be longer than the path delay plus the amount of clock skew between the flip-flops. Negative clock skew is illustrated in the next figure.

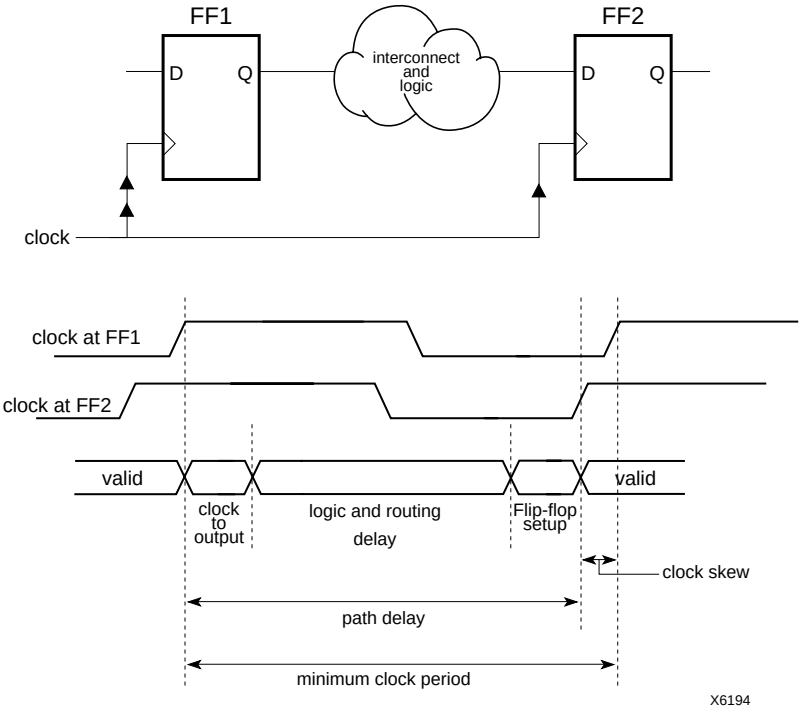


Figure 2-15 Negative Clock Skew

Positive Clock Skew

When the source is clocked first, the clock skew is called positive clock skew. Positive clock skew means that the clock period could be shorter than the path delay by the minimum amount of clock skew. The Timing Analyzer does not account for positive clock skew; it truncates positive clock skew to zero. Positive clock skew is illustrated in the following figure.

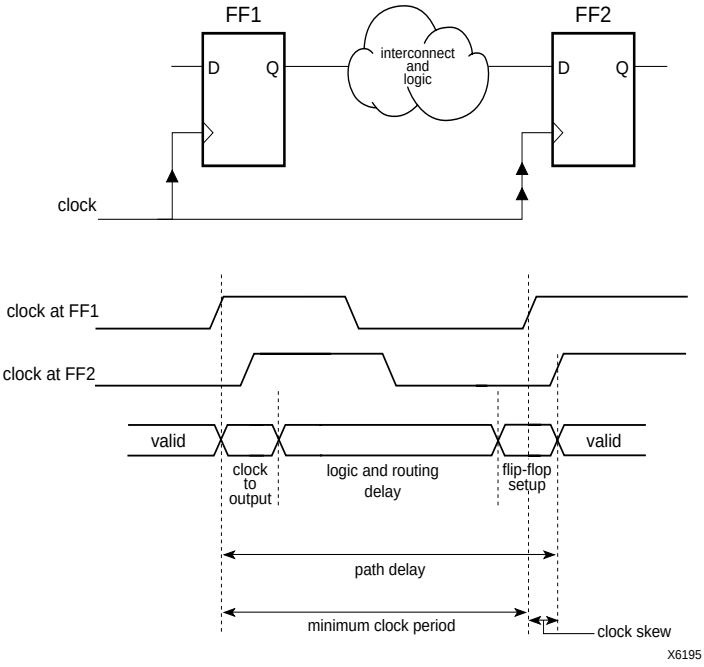


Figure 2-16 Positive Clock Skew

During Timing Analysis

The Timing Analyzer uses the timing constraints specified in the Physical Constraints File (FPGAs) or the VM6 design file (CPLD); it does not infer extra timing constraints. The Timing Analyzer accounts for clock skew for all register to register paths. The following example shows the clock skew portion of a Timing Constraints Analysis report.

```
Slack: 12.667ns path SOURCE to DEST relative to
        4.633ns total path delay
       -2.300ns clock skew
       15.000ns delay constraint
Path SOURCE to DEST contains 2 levels of logic:
Path starting from Comp: CLB_R14C13.K (from SIG_CLK)
To                  Delay type        Delay(ns)  Physical Resource
                                                 Logical Resource(s)
------------------------------------------------- --------
CLB_R14C13.YQ       Tcko 2.090R SOURCE
                                                 BEL_SOURCE.FFY
CLB_R14C14.C4       net (fanout=1)        1.533R DATA_SRC_DST
CLB_R14C14.K        Tdick 1.010R DEST
                                                 BEL_DEST.FFY
-------------------------------------------------
Total (3.100ns logic, 1.533ns route)      4.633ns (to SIG_CLK)
      (66.9% logic, 33.1% route)
```

You can use **Analyze** → **Query** → **Nets** to generate a Query Nets report to display the clock skew across specific clock nets. See the "Querying for Information" section of the "Using the Timing Analyzer" chapter for the procedure to generate a Query Nets Report, an example of a Query Nets Report, and information on the report format.

Off-Chip Delay

To determine system-level clock speed, you must add any external delay to paths that travel off-chip. This way, the Timing Analyzer includes this external delay when calculating the delay for the path. There is no default delay; the Timing Analyzer does not add off-chip delay unless you specify it. See the *XILINX Software Conversion Guide from XACTstep v5.x.x to XACTstep vM1.x.x* for information on how to specify these delays with the OFFSET constraint in the UCF (User Constraints File) file.

Chapter 3

Getting Started

This chapter describes starting and exiting the Timing Analyzer, using menus, buttons, Console windows, dialog boxes, and online help. It contains these sections.

- "Starting the Timing Analyzer"
- "Timing Analyzer Window"
- "Console Window"
- "Dialog Boxes"
- "Basic Timing Analysis Procedure"
- "Obtaining Help"
- "Exiting the Timing Analyzer"

Starting the Timing Analyzer

The Timing Analyzer runs on PCs and workstations. On the PC, the graphical user interface is based on Microsoft Windows. On the workstation, the interface is based on OSF Motif.

You can start the Timing Analyzer from the Windows Program Manager, the Xilinx Design Manager, or the command line.

From the Design Manager

To start the Timing Analyzer from the Design Manager window (PC or workstation), click on the Timing Analyzer icon (shown in the following figure) or select **Tools** → **Timing Analyzer**.

Stand-Alone Tool

If you installed the Timing Analyzer as a stand-alone tool on a PC, click on the Timing Analyzer icon (shown in the previous figure) on the Windows desktop or select timingan.exe from the Windows 95 or Windows NT Start button.

From the Command Line

To start the Timing Analyzer from a UNIX command line, type the following command.

timingan

These are a number of variations for starting the Timing Analyzer from the command line.

- To run the tool as a background process, end the command with an ampersand (&).

  timingan &

- To start the Timing Analyzer and open an existing FPGA or CPLD design, type the following.

  timingan {*design_name*.**ncd|***design_name*.**vm6}**

  For FPGA designs, if a physical constraints file (PCF) exists in the same directory as the design and has the same name, except for the extension, that *design_name*.**pcf** file is automatically opened.

- To start the tool, open an existing FPGA design and the corresponding physical constraints file, type the following. Physical constraints files only apply to FPGAs.

  timingan *design_name*.**ncd –pcf** *pcf_file_name*.**pcf**

- Use the **–run** option followed by a macro file name to run a macro. If a design and PCF file are specified on the command line also, the macro is run after the design and PCF file are loaded. The macro may contain an Exit command.

timingan *design_name*.**ncd –pcf** *pcf_file_name*.**pcf –run** *macro_name*

- To start the tool and open a Timing Analyzer report in a Hierarchical Report viewing window, type the following.

  timingan *filename*.**twr**

- To start the tool and open a Timing Analyzer report in a text editor window, type the following.

  timingan *filename*

Timing Analyzer Window

This section describes the Timing Analyzer's main window, menus, toolbar, and status bar. You can execute Timing Analyzer commands from the menus, toolbar, or the Console Window.

When you start the application, the Timing Analyzer window appears. The window contains pull-down menus, a toolbar at the top of the window, and a status bar at the bottom of the window. The menus are described in the "Menus" section.

Note: The Edit menu is only enabled when a design, report, or macro file is open and is the active window. Also, most of the toolbar buttons are not enabled unless a file is open and active.

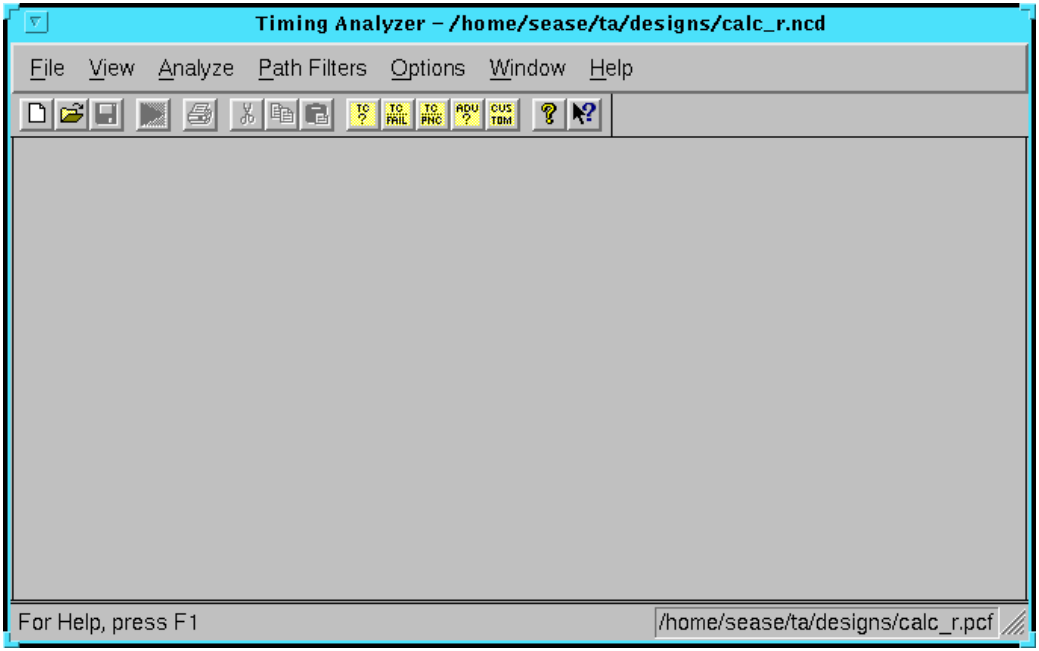


Figure 3-1 Timing Analyzer Window

The toolbar and status bar appear by default when you start the Timing Analyzer. You can hide them from view by selecting the Toolbar or the Status Bar commands, respectively, from the View menu.

Menus

Most of the Timing Analyzer commands are available in the pull-down menus. However, unless a design is loaded, most of the commands are disabled and not available. Certain commands and some command options are disabled and not available, depending whether the open design is an FPGA or a CPLD design.

You can select menu commands with the mouse or the keyboard. With the mouse, click the left mouse button on the desired command. With the keyboard, press the Alt key and type in the letter underlined in the menu for that command. When you select a menu command with either method, a brief description of the command's function appears in the Status Bar at the bottom of the Timing Analyzer window.

For complete command descriptions, select **Help** → **Help Topics** or see the "Menu Commands" chapter of this manual.

Toolbar

The toolbar appears at the top of the window, just below the menu bar. The toolbar provides button access to frequently used commands in the menus. Textual labels for the buttons appear when you move the cursor arrow over a button. This feature is called a tool tip. A longer description also appears in the status bar. These buttons are shown and described in the "Toolbar" section of the "Menu Commands" chapter.

Status Bar

By default, the status bar appears at the bottom of the window. When you select a menu command, a brief description of the command's function appears in the status bar. As the Timing Analyzer processes, status messages are dynamically updated and displayed.

To hide or show the status bar, select **View** → **Status Bar**.

Console Window

The Console window displays the sequence of commands that you have used in a Timing Analyzer session. It is primarily used for creating macros, but it has a command line field, in which you can type and execute keyboard commands. The Console window also contains a Show Command Status box that you can click on to display or hide status messages. For information on creating and using macros, see the "Creating a Macro" section of the "Using the Timing Analyzer" chapter.

Commands that you can enter in the Console window are described in the "Command Line Syntax" chapter.

You can open the Console window by selecting **View** → **Console**.

Dialog Boxes

Many Timing Analyzer menu commands display dialog boxes in which you can enter information and set options. This section describes dialog box common fields, how to move items in list boxes, and how to use filters.

Common Fields

The fields shown in the following table are common to most dialog boxes.

Table 3-1 Common Dialog Box Fields

Dialog Box Field	Function
OK	Closes the dialog box and implements the intended action according to the settings in the dialog box
Cancel	Closes the dialog box without effecting any action
Help	Displays information on that particular dialog box

Moving Items in List Boxes

Many of the dialog boxes in the Timing Analyzer feature list boxes, such as Available Nets and Selected Nets in the next figure. You can select and move items from one list box to another using either the mouse or the keyboard, or a combination of these methods.

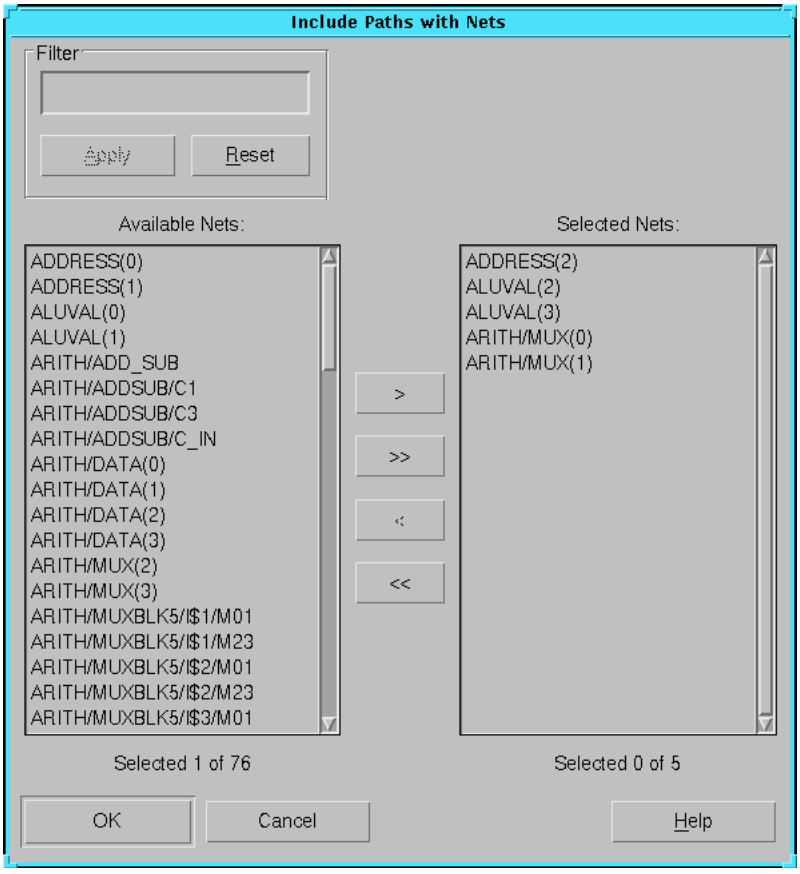


Figure 3-2 List Boxes Within a Dialog Box

Using the Mouse

Use the mouse to select items in list boxes as follows.

- To move an item to a list box on the right, select it with the left mouse button. Click the **>** button. To move an item to a list box on the left, select it, then click the **<** button.
- To move all items to a list box on the right, click the **>>** button. To move all items to a list box on the left, click the **<<** button.
- To move sequential items, select the first one with the left mouse button. Hold down the **Shift** key. Select the last item and release

the **Shift** key. Click the **>** or **<** button to move the selected items to the right or left list box, respectively.

You can also select the first item; drag the mouse up or down until all the desired items are highlighted; and then click the **>** or **<** button.

- To move multiple items in any order, hold down the **Ctrl** key while clicking individual items. When you finish selecting, release the **Ctrl** key and click the **>** or **<** button.

Using the Keyboard

To navigate within dialog boxes using the keyboard, use these methods.

- Use the Tab key to move to fields within dialog boxes.
- To move to previous fields within dialog boxes, press and hold the Shift key, then press the Tab key.
- To scroll down the list box to select items that are not visible in the list box, tab to the list box and hold down the down arrow key until the item is highlighted.
- Pressing the Escape key closes the dialog box without effecting any action (equivalent to clicking the Cancel button).

Use the keyboard to select items in list boxes as follows.

- To move an item in a list box, press the **Tab** key until the first item in the list box is highlighted. Press the down arrow key to select the desired item. Tab to the **>** or **<** button to move it to the right or left list box, respectively. Press **Enter**.
- To move all items to a list box on the right, tab to the **>>** button and press **Enter**. To move all items to a list box on the left, tab to the **<<** button and press **Enter**.
- To move consecutive items, tab to the first item in the list box. Use the down arrow key to highlight the first desired item. Press and hold the **Shift** key while using the down arrow key to select the other items in the sequence. Tab to the **>** button. Press **Enter**.
- *On workstations only*: To move multiple items in any order, tab to the list box and press **Shift F8**. Use the up and down arrow

keys to navigate within the list box. Press the space bar to select each item. Tab to the **>** button. Press the **Enter** key.

Using Filters with Commands

Several Timing Analyzer menu commands open dialog boxes that allow you to filter a list of choices, that is, display a subset of the listed items. You use these filters to produce more specific information in Timing Analysis reports. These dialog boxes contain a Filter field and Apply and Reset buttons, such as those shown in the "List Boxes Within a Dialog Box" figure.

This section describes valid filter inputs and wildcards, matching text strings, and an example of how apply a filter in a menu command dialog box.

Valid Inputs and Wildcards

In filter fields, you can enter a text string consisting of characters and wildcards.

- Characters can be any alphanumeric characters, text spaces, and the characters that appear on the top of the number keys on a keyboard. Alphabetic characters are case-sensitive. No control characters are permitted.
- A wildcard can be an asterisk (*), which can represent any number of characters, or a question mark (?), which represents a single character.

You cannot enter a range of characters in filter fields.

Matching Text Strings

The Timing Analyzer does not strictly match patterns; it matches entire text strings. It does not find a string if it is embedded in a larger string, unless you use wildcards. For example, it does not find $1N36 if it is embedded in ABC$1N36XYZ. However, if you searched for *$1N36*, it would find that string in ABC$1N36XYZ.

Example Procedure

Following is a basic example of how to use filters and move items in list boxes.

1. Select **Path Filters** → **Common Filters** → **Include Paths with Nets**.

   The Include Paths with Nets dialog box appears as shown in the following figure. All the nets in the design are listed in the Available Nets list box.

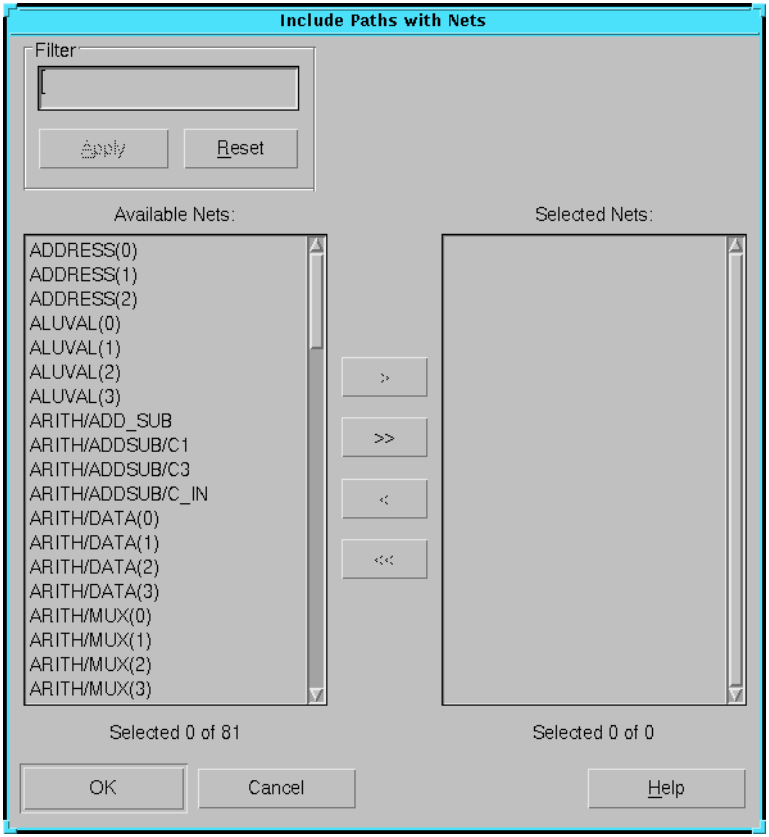


Figure 3-3 Dialog Box Before Applying a Filter

2. Type **ARITH*** in the Filter field.

   When you enter text in the filter field, the Apply button is enabled.

3. Click **Apply**.

   Because the number of nets in the design can be cumbersome, as shown in the following figure, applying a filter reduces the

number of nets displayed in the Available Nets list box. Only the nets whose names begin with ARITH now appear in the list box.

To clear the filter, click **Reset**. Reset clears the filter and restores all items to the left list box that are not in the right list box. You can also backspace over the information in the filter text box, but to affect the list box, you must then click on Apply or Reset.

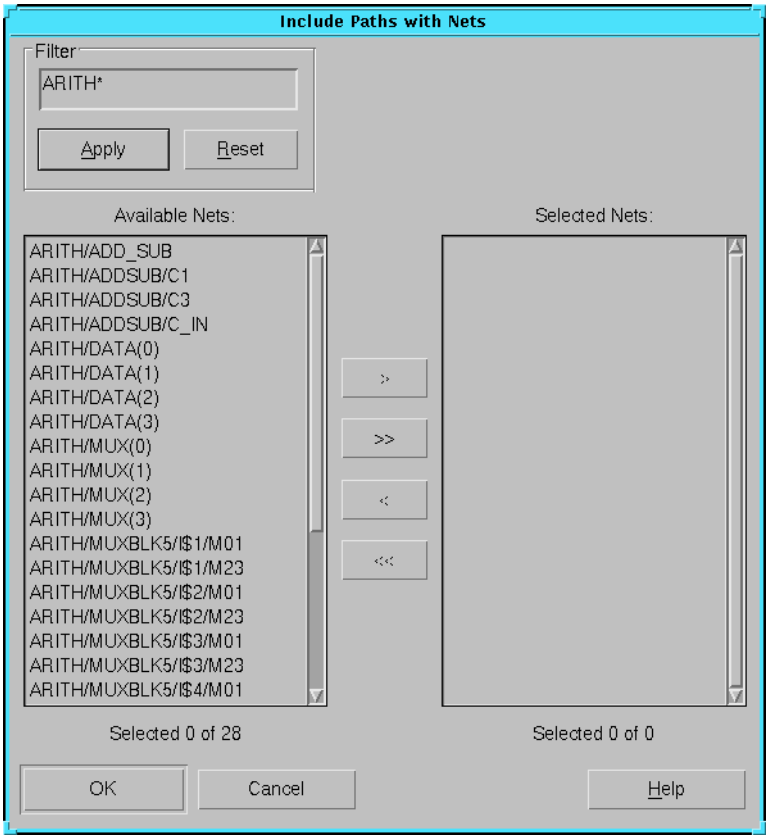


Figure 3-4 Dialog Box After Applying a Filter

4. Move ARITH/DATA* from the Available Nets list box to the Selected Nets list box, using the methods described in the "Moving Items in List Boxes" section.

If you are only interested in nets ARITH / DATA(0) through ARITH / DATA(3), in this analysis, this step moves those nets to the Selected Nets list box, as illustrated in the following figure.

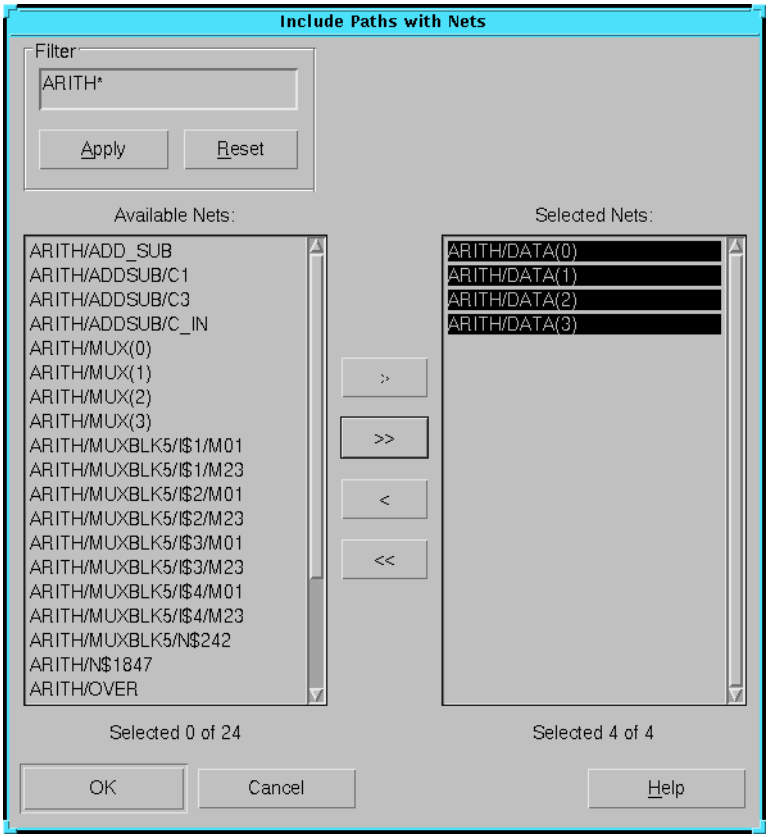


Figure 3-5 Nets Included in Analysis

Basic Timing Analysis Procedure

The typical procedure for using the Timing Analyzer is as follows.

1. Open the Timing Analyzer and load your design.

   For FPGAs, if a physical constraints file (PCF) with the same name as your design exists in the directory, the Timing Analyzer also loads that file, by default. (The PCF file is generated when a design is mapped.)

2. If you are unfamiliar with the Timing Analyzer, explore its features. You can use the online help facility to help you with this process. To run the online help, select **Help** → **Help Topics**.
3. You can optionally generate a report to obtain a basic overview of the design's timing before you begin to analyze it in detail. The Advanced Design Analysis report provides that information. Choose the Advanced Design command from the Analyze menu to generate and display an Advanced Design Analysis report.
4. Select commands from the Path Filters menu to determine which types of paths to analyze and report. You can filter out paths you are not interested in.
5. Select commands from the Options menu to change the speed grade for analysis or to specify report options.
6. Select commands from the Analyze menu to specify the kinds of reports you want to generate.
7. Select commands from the Edit menu to search or edit reports.
8. Select commands from the File menu to save or print reports.
9. Optionally, you can create macros comprising the commands just issued.

These steps are described in more detail in the "Using the Timing Analyzer" chapter.

Obtaining Help

You can obtain help on the Timing Analyzer's commands and procedures by selecting commands in the Help menu, by selecting the Help button in the toolbar, by clicking the Help button in dialog boxes, or by pressing the F1 key. The Help button in the toolbar, the ones contained in some menu command dialog boxes, and the F1 key provide context-sensitive help for what you click on or that dialog box, respectively. Context-sensitive help is discussed in the "Context-Sensitive Help" section.

Help Menu

The Help menu contains the following commands.

- Help Topics lists the online help topics available for the Timing Analyzer. From the opening screen, you can jump to command information or step-by-step instructions for using the Timing Analyzer. After you start the help, you can click the Contents button (first button in the top-left corner) in the Help window whenever you want to return to the help topics list.
- About Timing Analyzer displays a pop-up window that displays the version number of the Timing Analyzer software.

Context-Sensitive Help

You can obtain context-sensitive help on the Timing Analyzer by using the Help button in the toolbar or the Help button contained in many of the menu command dialog boxes. This section describes both methods of how to access the context-sensitive help.

Toolbar Button

To access context-sensitive help from the toolbar, follow this procedure.

1. Click on the Help button from the toolbar, shown in the following figure.

   The cursor changes to an arrow and question mark, like the button.

2. For help on menu commands, click (with the left mouse button) on the menu, then click the command in that menu or submenu. For help on toolbar buttons, click once on the particular button.

   The Timing Analyzer displays information about the selected command or button.

Help Button in Dialog Boxes

Many of the dialog boxes associated with Timing Analyzer menu commands have a Help button. You can click on the button to obtain help on that dialog box. A window opens with the information.

F1 Key

Pressing the F1 key when the cursor is placed on a dialog box displays help for that dialog box.

Exiting the Timing Analyzer

To exit the Timing Analyzer, click **File** → **Exit** or type exit at the prompt in the Console window.

If you have unsaved reports open, a prompt box similar to that in the next figure appears.

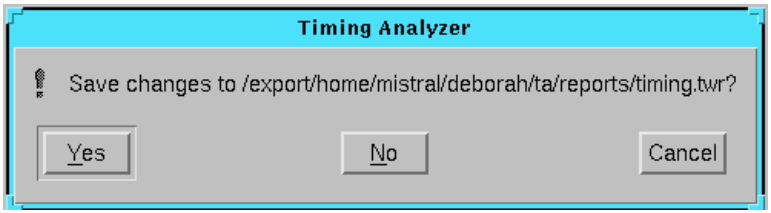


Figure 3-6 Exit Prompt Box

Click **Yes** to save the report, then follow the procedure described in the "Saving a Report" section of the "Using the Timing Analyzer" chapter.

You are prompted for confirmation before exiting, even if there is no unsaved data. However, if SetForce is on, an Exit command in a macro causes the Timing Analyzer to exit without asking for confirmation.

Chapter 4

Using the Timing Analyzer

This chapter describes the various functions you can perform with the Timing Analyzer. It contains the following main sections.

- "Opening a Design"
- "Opening Physical Constraints Files"
- "Viewing Settings"
- "Viewing Clocks"
- "Querying for Information"
- "Creating Reports"
- "Specifying Report Appearance and Content"
- "Changing the Speed Grade"
- "Using Path Filtering Commands"
- "Using the Console Window"
- "Using Macros"

Note: The commands and dialog boxes in this chapter are used in the context of procedures, but they are not explained in detail. For a detailed explanation of them, see the "Menu Commands" chapter.

Opening a Design

Before you can create a timing report using the Timing Analyzer, load a mapped NCD (FPGA) or a completed placed and routed VM6 (CPLD) design file. The NCD (FPGA) can be mapped, placed, or routed. To open a design for timing analysis, follow these steps.

1. Select **File** → **Open Design**, or click on the Open Design toolbar button.

The Open Design dialog box appears, as shown in the "Open Design Dialog Box" figure of the "Menu Commands" chapter.

2. In the Look in / Directories list box, click on the directory containing the NCD (FPGA) or VM6 (CPLD) file to load.
3. Under Files of Type / List Files of Type, click on the pull-down the list box and select FPGA Designs (*.ncd) or CPLD Designs (*.vm6).

   All the available NCD or VM6 files are displayed in the list box.
4. Select an NCD or a VM6 file from the list box, or type the name in the field below File Name. (*.ncd appears by default; backspace over the asterisk before typing in the design file name.)
5. Click **OK**.

   The Timing Analyzer reads your design and device information, processes any timing constraints, and then loads your design. For FPGA designs, the Timing Analyzer also reads the .pcf physical constraints file with the same name as the design file, if one exists in the same directory as the design file (the PCF file contains physical constraints information). The order of the constraints in the PCF file is reflected by the Timing Analyzer.

   When your design is loaded, the path name and design file name appear at the top of the Timing Analyzer window.

You can now create a timing report. Refer to the "Creating Reports" section for instructions on this procedure.

Warning: If you open a design when another design is open, the Timing Analyzer resets the current settings to the defaults. If you re-open a design that is already open, the Timing Analyzer also resets the current settings to the defaults and opens the default PCF, if it exists.

Opening Physical Constraints Files

Physical Constraints Files (PCF) contain physical constraint information. They apply only to FPGAs, because CPLD timing information is contained in the (VM6) design file itself. The order of the timing constraints in the PCF file is reflected by the Timing Analyzer. This section describes methods for loading and opening Physical Constraints Files.

Automatically Opening a Physical Constraints File

When you open a design using **File** → **Open Design**, the Timing Analyzer automatically loads the default Physical Constraints File if it exists. The default Physical Constraints File is a physical constraints file with the same name as the design in the same directory as the design file.

A message similar to the following appears on the right side of the status bar at the bottom of the Timing Analyzer window.

```
/home/user/ta/designs/design10.pcf
```

If there is no default physical constraints file, a message box appears with a message similar to the following.

```
No default Physical Constraints File found for design
"/home/user/ta/designs/design10.ncd"
```

Manually Opening a Physical Constraints File

If you already have a design open and wish to load a different Physical Constraints File for use with the current design, follow these steps.

1. Select **File** → **Open Physical Constraints**.

   The Open Physical Constraints dialog box appears.

2. In the Look in / Directories list box, click on the directory containing the PCF file to load.

3. Under Files of Type / List Files of Type, Physical Constraints (*.pcf) is the default and the only file type you can select.

   All the available PCF files are displayed in the list box.

4. Select a PCF file from the list box, or type the name in the field below File name. (*.pcf appears by default; backspace over the asterisk before typing in the physical constraints file name.)
5. Click **OK**.

   The Timing Analyzer reads the PCF file and the path name appears on the right side of the status bar at the bottom of the Timing Analyzer window.

Viewing a Physical Constraints File

In some cases you may want to open a PCF file for viewing from within the Timing Analyzer. When you open a PCF file by this method, the Timing Analyzer does not load the PCF file for use with the current design. It just opens the file for viewing but does not replace the PCF file that is loaded for use with the current design. To open a PCF file in this way, follow these steps.

1. Select **File** → **Open**.

   The Open dialog box appears.
2. Under Files of Type / List Files of Type, select All Files (*.*).
3. Select a PCF file from the list box, or type it in the field below File Name.
4. Click **OK**.

The PCF file is displayed in a window but the path name on the right side of the status bar at the bottom of the Timing Analyzer window does not change since opening a PCF file by this method does not load the PCF file for processing with the current design.

Viewing Settings

To view current Timing Analyzer settings, select **View** → **Settings**.

The Timing Analyzer displays a pop-up window with the current settings and options. The following figure displays an example of the Settings window.

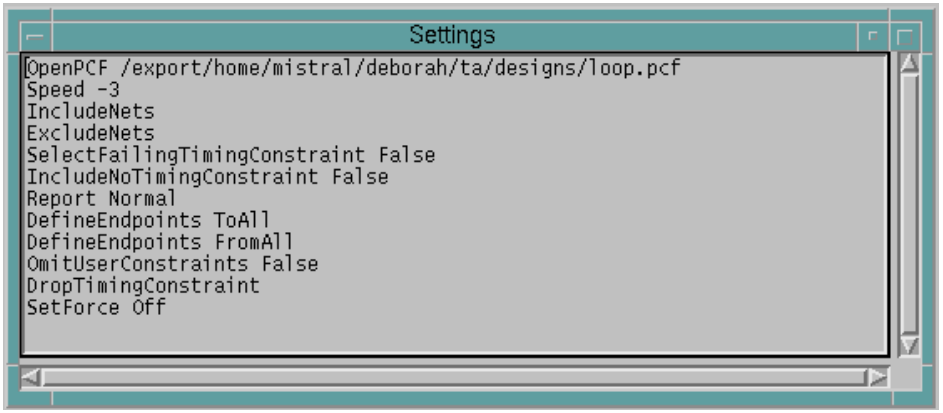


Figure 4-1 Settings Window

When this window is the active window and you change an option setting or a path filter, the change is immediately reflected in the window. If it is not the active window and you change an option or a filter, you must click inside the Settings window to update it automatically.

The contents of the window can be saved as an .xtm file to save the settings as a macro to return the system to the same state as when the settings were saved. See the "Saving a New Macro" and the "Running a Macro" sections for more information. You can also save the contents of the window to a .twr file. TWR files are listed as Timing Analysis Reports (*.twr) under List Files of Type in File menu command dialog boxes. See the "Saving a Report" section for the procedure to save a report.

Viewing Clocks

The Clocks report lists the names of all of the clocks in the design. To generate a Clocks report, select **View** → **Clocks**. The Timing Analyzer displays the Clocks report in a pop-up window. You can save the contents of the window as a (.twr) file. TWR files are listed as Timing Analysis Reports (*.twr) under List Files of Type in File menu command dialog boxes. See the "Saving a Report" section for the procedure to save a report.

Querying for Information

You may want to focus on the source, destination, and timing of a particular net or time group. You can obtain information about the timing of particular nets or the members of a time group using the Query command. This command only applies to FPGAs; it is disabled if a CPLD design is open.

To perform a query, follow this procedure.

1. Select **Analyze** → **Query**.

   The Query dialog box appears, as shown in the "Query Dialog Box" figure of the "Menu Commands" chapter.

2. Select the subject of the query by clicking on Nets or TimeGroups. Nets is the default.

   The following information is generated for each option.

   - Nets — The Timing Analyzer shows the fanout, the timing from the source CLB to each of the destination CLBs, and the CLB names in the generated Query Nets Report.
   - TimeGroups — The Timing Analyzer lists the elements in the specified timing groups in the generated Query TimeGroups Report.

   The other fields in the dialog box change to *Nets* or *TimeGroups* with your selection.

3. If you select Nets, enter a value in the Delay Greater Than field of the Filter for Available *Nets* / *TimeGroups* section, if desired. This field is disabled if you select TimeGroups.

   The Delay Greater Than value specifies a minimum net delay in nanoseconds. The Timing Analyzer displays only those paths that have a delay greater than or equal to the specified value.

4. Enter a filter in the other portion of the Filter for Available *Nets* / *TimeGroups* section, if desired, and click **Apply**.

   If you enter a value in the Delay Greater Than and a filter in the filter field, the Timing Analyzer lists the nets that meet both criteria. See the "Using Filters with Commands" section of the "Getting Started" chapter for valid filter inputs.

5. Select the nets or timing groups that you want to query from the Available *Nets* / *TimeGroups* list box and move specific ones or all of them to the Selected *Nets* / *TimeGroups* list box.

   See the "Moving Items in List Boxes" section of the "Getting Started" chapter for details on selecting and moving items between list boxes.

6. Click **OK**.

   The Timing Analyzer displays the Query *Nets/TimeGroups* Report in a pop-up window, which can be saved as a TWR file. *Nets/TimeGroups* is Nets or TimeGroups, corresponding with your selection in step 2. See the "Saving a Report" section for the procedure to save a report.

Query Nets Report

The following is an example of Query Nets Report.

```
M-- $1N15 ............... $1I37.O.............. 4.0 $1N6.F4
                                                $1I45.O 4.0 $1N6.F4

--- $1N32 ............... C.I2.................. 2.0 $1I45.T
                                                    2.0 $1N6.F3

--- $1N34 ............... D.I2.................. 1.0 $1N6.F1

--- $1N6 ................ $1N6.X................ 1.0 O1.O
                                                    1.0 O2.O

--- $1N51 ............... A1.I2................. 0.0 $1I45.I

--- $1N38 ............... B.I2.................. 2.0 $1I37.T

--- $1N41 ............... A.I2.................. 2.0 $1I37.I
```

The contents of the Query Nets Report example have been placed in the following table to illustrate the format of the report. Connections are listed by net, then by source; each is only listed once. Explanations of the information in Net Characteristics and Delay columns follow the table.

Table 4-1 Query Nets Report Format

Net Characteristics	Net Name	Driver Pin Name	Delay Value	Load Pin Name
M--	$1N15	$1I37.O	4.0	$1N6.F4
		$1I45.O	4.0	$1N6.F4
---	$1N32	C.I2	2.0	$1I45.T
			2.0	$1N6.F3
---	$1N34	D.I2	1.0	$1N6.F1
---	$1N6	$1N6.X	1.0	O1.O
			1.0	O2.O
---	$1N51	A1.I2	0.0	$1I45.I
---	$1N38	B.I2	2.0	$1I37.T
---	$1N41	A.I2	2.0	$1I37.I

Net Characteristics

The entries in the Net Characteristics column are comprised of three characters. The characters indicate aspects of the net(s) you query. Each character position is independent of the others. The character position and values of each position are illustrated in this table.

Left = Net Source	Middle = Net Load	Right = If Critical
S = No Source	L = No Load	C = Net marked with CRITICAL property in the design or Net PRI is ≥ 10
M = Multiple Sources		- = Not Critical

Delay Value

The entries in the Delay Value column can include asterisks (*), question marks (?), or tildes (~).

- The pin is unrouted or one or both pins are not yet placed if three asterisks (***) appear as the delay value. An asterisk preceding a number, *3 for example, indicates the connection delay is estimated, if timing analysis is performed on an unrouted design. Because the Timing Analyzer can perform timing analysis on mapped FPGA designs, generating a Query Nets report can determine if a design does not meet timing requirements before a design is routed.
- A question mark (?) indicates the net was routed incorrectly.
- A tilde (~) preceding a delay value indicates that the delay value is approximate. The delay can be longer than estimated.

Query Time Groups Report

The Query Time Groups report lists the contents of each time group that you select. Time group information is also generated in the Timing Constraints Analysis report.

Creating Reports

After you load a design file, you can decide what kind of report you want to generate. This section describes how to create all the reports available in the Timing Analyzer as well as how to save and print them.

With the Find command on the Edit menu, you can search for specific text strings in reports. Directions for this procedure are given in the "Searching for Text in a Report" section.

The Timing Analyzer has default settings that you can change using filters with various commands. Filters modify the scope of generated reports by specifying which paths you want to analyze. For more information, refer to the "Using Path Filtering Commands" section. To view the current settings, refer to the "Viewing Settings" section.

Timing Constraints Analysis

The Timing Constraints Analysis report compares the design's performance to the timing constraints.

There are several ways to generate a Timing Constraints Analysis report. You can use the following toolbar buttons to generate a Timing Constraints Analysis report.

These buttons from left to right are as follows.

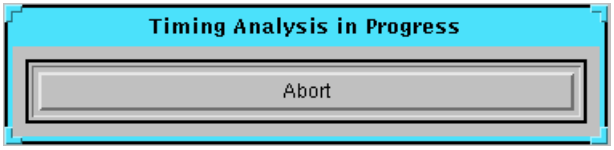
- Report Paths in Timing Constraints
- Report Paths Failing Timing Constraints
- Report Paths Not Covered by Timing Constraints

In addition to these buttons the **Analyze** → **Timing Constraints** submenu contains the following commands.

- Report Paths in Timing Constraints (Analyze Menu)
- Report Paths Failing Timing Constraints (Analyze Menu)
- Report Paths Not Covered by Timing Constraints (Analyze Menu)

To generate a Timing Constraints Analysis report, select one of the three commands in the **Analyze** → **Timing Constraints** submenu, or click one of the three Timing Constraints Analysis buttons in the toolbar.

This command has an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears.



Clicking the Abort button, the Esc key, or the Enter/Return key aborts the analysis and no report is generated or displayed.

In addition to using the above buttons and commands, you can use the following path filter commands to modify the Timing Constraints Analysis report (See “Using Path Filtering Commands” section for more details).

- Disable Timing Constraints (Path Filters Menu)
- Include Paths with Nets (Path Filters Menu)

- Exclude Paths with Nets (Path Filters Menu)
- Control Path Tracing (Path Filters Menu)

After processing the design, the Timing Analyzer displays the Timing Constraints Analysis report in a pop-up window. The contents of the window can be saved as a TWR file; see the "Saving a Report" section for the procedure to save a report. Following is an example of a Timing Constraints Analysis report.

```
--------------------------------------------------------------------------------
Timing Analyzer 2.1i
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.

Design file:              testclk.ncd
Physical constraint file: testclk.pcf
Device,speed:             xcv100,-5 (x1_0.71 1.76 Advanced)
Report level:             verbose report, limited to 1 item per constraint
--------------------------------------------------------------------------------

================================================================================
Timing constraint: TS_ck1_i = PERIOD TIMEGRP "ck1_i"  20 nS   HIGH 50.000
% ;
 955 items analyzed, 0 timing errors detected.
 Minimum period is  14.655ns.
--------------------------------------------------------------------------------
Slack:     5.345ns path core_inst1/counter1/cont<1> to core_inst1/
counter1/cont<9> relative to
          20.000ns delay constraint
Path core_inst1/counter1/cont<1> to core_inst1/counter1/cont<9> contains
12 levels of logic:
Path starting from Comp: CLB_R10C8.S0.CLK (from ck1)
To                    Delay type         Delay(ns)  Physical Resource
                                                    Logical Resource(s)
-------------------------------------------------  --------
CLB_R10C8.S0.YQ       Tcko                  1.203R  core_inst1/counter1/
                                                    cont<1>
                                                    core_inst1/counter1/
                                                    cont_reg<1>
CLB_R11C10.S0.G1      net (fanout=5)        3.073R  core_inst1/counter1/
                                                    cont<1>
CLB_R11C10.S0.COUT    Topcyg                1.545R  core_inst1/counter1/C9/
                                                    C3/C1/O C369
                                                    core_inst1/counter1/
                                                    C9/C3/C1
.
```

```
.
.
CLB_R9C10.S1.F1      net (fanout=1)       1.491R  core_inst1/counter1/N362
CLB_R9C10.S1.CLK     Tas                   1.043R  core_inst1/counter1/
                                                   cont<9>
                                                   C303
                                                   core_inst1/counter1/
                                                   cont_reg<9>
--------------------------------------------------
Total (6.638ns logic, 8.017ns route)      14.655ns (to ck1)
      (45.3% logic, 54.7% route)
--------------------------------------------------------------------------
.
.
.
All constraints were met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock ck1_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    6.202(R)|            |
start_i        |    2.213(R)|    0.000(R)|
---------------+------------+------------+

Setup/Hold to clock ck2_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    5.861(R)|            |
---------------+------------+------------+

Clock ck1_i to Pad
---------------+------------+
               | clk (edge) |
Destination Pad|   to PAD   |
---------------+------------+
out1_o         |   16.691(R)|
```

```
---------------+------------+

Clock ck2_i to Pad
---------------+------------+
               | clk (edge) |
Destination Pad|   to PAD   |
---------------+------------+
out2_o         |   14.969(R)|
---------------+------------+

Clock to Setup on destination clock ck1_i
- | Src/Dest| Src/Dest| Src/Dest| Src/Dest|
Source Clock   |Rise/Rise|Fall/Rise|Rise/Fall|Fall/Fall|
---------------+---------+---------+---------+---------+
ck1_i          |   14.655|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock ck2_i
---------------+---------+---------+---------+---------+
               | Src/Dest| Src/Dest| Src/Dest| Src/Dest|
Source Clock   |Rise/Rise|Fall/Rise|Rise/Fall|Fall/Fall|
---------------+---------+---------+---------+---------+
ck1_i          |   11.886|         |         |         |
ck2_i          |   14.813|         |         |         |
---------------+---------+---------+---------+---------+


Table of Timegroups:
--------------------
TimeGroup ck1_i:
BELs:
 core_inst1/counter1/regist1_reg<0>  core_inst1/counter1/regist1_reg<1>
core_inst1/counter1/regist1_reg<2>
 core_inst1/counter1/regist1_reg<3>  core_inst1/counter1/regist1_reg<4>
core_inst1/counter1/regist1_reg<5>
 core_inst1/counter1/regist1_reg<6>  core_inst1/counter1/regist1_reg<7>
core_inst1/counter1/regist1_reg<8>
 core_inst1/counter1/regist1_reg<9>  core_inst1/counter1/regist0_reg<0>
core_inst1/counter1/regist0_reg<1>
 core_inst1/counter1/regist0_reg<2>  core_inst1/counter1/regist0_reg<3>
core_inst1/counter1/regist0_reg<4>
 core_inst1/counter1/regist0_reg<5>  core_inst1/counter1/regist0_reg<6>
core_inst1/counter1/regist0_reg<7>
 core_inst1/counter1/regist0_reg<8>  core_inst1/counter1/regist0_reg<9>
core_inst1/counter1/cont_reg<0>
```

```
 core_inst1/counter1/cont_reg<1>     core_inst1/counter1/cont_reg<2>
core_inst1/counter1/cont_reg<3>
 core_inst1/counter1/cont_reg<4>     core_inst1/counter1/cont_reg<5>
core_inst1/counter1/cont_reg<6>
 core_inst1/counter1/cont_reg<7>     core_inst1/counter1/cont_reg<8>
core_inst1/counter1/cont_reg<9>

TimeGroup ck2_i:
BELs:
 core_inst2/counter1/regist1_reg<0>  core_inst2/counter1/regist1_reg<1>
core_inst2/counter1/regist1_reg<2>
 core_inst2/counter1/regist1_reg<3>  core_inst2/counter1/regist1_reg<4>
core_inst2/counter1/regist1_reg<5>
 core_inst2/counter1/regist1_reg<6>  core_inst2/counter1/regist1_reg<7>
core_inst2/counter1/regist1_reg<8>
 core_inst2/counter1/regist1_reg<9>  core_inst2/counter1/regist0_reg<0>
core_inst2/counter1/regist0_reg<1>
 core_inst2/counter1/regist0_reg<2>  core_inst2/counter1/regist0_reg<3>
core_inst2/counter1/regist0_reg<4>
 core_inst2/counter1/regist0_reg<5>  core_inst2/counter1/regist0_reg<6>
core_inst2/counter1/regist0_reg<7>
 core_inst2/counter1/regist0_reg<8>  core_inst2/counter1/regist0_reg<9>
core_inst2/counter1/cont_reg<0>
 core_inst2/counter1/cont_reg<1>     core_inst2/counter1/cont_reg<2>
core_inst2/counter1/cont_reg<3>
 core_inst2/counter1/cont_reg<4>     core_inst2/counter1/cont_reg<5>
core_inst2/counter1/cont_reg<6>
 core_inst2/counter1/cont_reg<7>     core_inst2/counter1/cont_reg<8>
core_inst2/counter1/cont_reg<9>

Timing summary:
---------------

Timing errors: 0  Score: 0

Constraints cover 2184 paths, 0 nets, and 380 connections (100.0%
coverage)

Design statistics:
   Minimum period:  14.813ns (Maximum frequency:  67.508MHz)
   Minimum input arrival time before clock:   6.202ns
   Minimum output required time after clock:  16.691ns

Analysis completed Fri Mar 12 12:10:11 1999
--------------------------------------------------------------------------
```

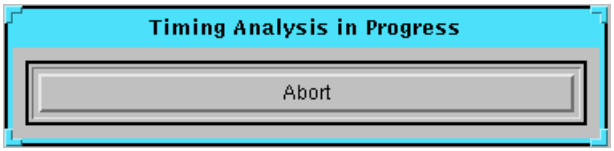
Advanced Design Analysis

The Advanced Design Analysis report provides a set of summary statistics for the paths from the timing requirements submitted for analysis. This report is essentially an error report that displays a summary header for each constraint whether it passes or not and lists paths in error for constraints that are violated.

If the PCF file contains no constraints, the Advanced Design Analysis report creates four basic constraints: PERIOD, OFFSET IN, OFFSET OUT, and PAD TO PAD.

To generate an Advanced Design Analysis report, select **`Analyze`** → **`Advanced Design`**, or click on the Advanced Design button in the toolbar.

This command has an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears.



Clicking the Abort button, the Esc key, or the Enter/Return key aborts the analysis. A report is not generated or displayed.

After processing the design, the Timing Analyzer displays the Advanced Design Analysis report in a pop-up window. The contents of the window can be saved as a TWR file; see the “Saving a Report” section for the procedure to save a report. Following is an example of an FPGA Advanced Design Analysis report.

```
--------------------------------------------------------------------------------
Timing Analyzer 2.1i
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.

Design file:              C:\designs\loop.ncd
Physical constraint file: C:\designs\loop.pcf
```

```
Device,speed:             xc4036ex,-3 (x1_0.08 3.7f )
Report level:             error report, limited to 1 item per constraint
--------------------------------------------------------------------------------


================================================================================
Timing constraint: TS01 = MAXDELAY FROM TIMEGRP "FFS" TO TIMEGRP "FFS"
2000.000000 pS PRIORITY 0 ;
 1 item analyzed, 0 timing errors detected.
 Maximum delay is   3.340ns.
--------------------------------------------------------------------------------


================================================================================
Timing constraint: TS02 = MAXDELAY FROM TIMEGRP "PADS" TO TIMEGRP "FFS"
1500.000000 pS PRIORITY 0 ;
 3 items analyzed, 3 timing errors detected.
 Maximum delay is   4.006ns.
--------------------------------------------------------------------------------
Slack:    -2.506ns path D to $1N11 relative to
           1.500ns delay constraint

Path D to $1N11 contains 2 levels of logic:
Path starting from Comp: IOB.PAD
To                  Delay type         Delay(ns)  Physical Resource
                                                  Logical Resource(s)
-------------------------------------------------  --------
IOB.I1              Tpid                  1.810R  D
                                                  D
                                                  $1N13
CLB.F1              net (fanout=1)     e  1.066R  $1N13
CLB.K               Tick                  1.130R  $1N11
                                                  $1N15
                                                  $1N11
-------------------------------------------------
Total (2.940ns logic, 1.066ns route)       4.006ns (to $1N19)
      (73.4% logic, 26.6% route)

--------------------------------------------------------------------------------


================================================================================
Timing constraint: TS03 = MAXDELAY FROM TIMEGRP "FFS" TO TIMEGRP "PADS"
2500.000000 pS PRIORITY 0 ;
 1 item analyzed, 1 timing error detected.
 Maximum delay is  10.716ns.
```

```
--------------------------------------------------------------------------------
Slack:    -8.216ns path $1N11 to OUT relative to
           2.500ns delay constraint

Path $1N11 to OUT contains 2 levels of logic:
Path starting from Comp: CLB.K (from $1N19)
To                  Delay type         Delay(ns)  Physical Resource
                                                  Logical Resource(s)
-------------------------------------------------  --------
CLB.XQ              Tcko                  1.830R  $1N11
                                                  $1N11
IOB.O               net (fanout=2)     e  1.066R  $1N11
IOB.PAD             Tops                  7.820R  OUT
                                                  OUT.OUTBUF
                                                  OUT
-------------------------------------------------
Total (9.650ns logic, 1.066ns route)      10.716ns
      (90.1% logic, 9.9% route)

--------------------------------------------------------------------------------


2 constraints not met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock ck1_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    6.202(R)|            |
start_i        |    2.213(R)|    0.000(R)|
---------------+------------+------------+
.
.
.

Table of Timegroups:
-------------------
TimeGroup PADS:
BELs:
```

```
 OUT  D    C    CLR

TimeGroup FFS:
BELs:
 $1N11



Timing summary:
---------------

Timing errors: 4  Score: 15874

Constraints cover 5 paths, 0 nets, and 5 connections (100.0% coverage)


Design statistics:
   Maximum path delay from/to any node:  10.716ns


Analysis completed Wed Mar 3 14:30:42 1999
--------------------------------------------------------------------------------
```

The format of a CPLD Advanced Design Analysis report differs from the FPGA report format, as shown in the following report excerpt.

```
Design:     tspec1d
Device:     XC9572-7-PC84
Program:    Timing Report Generator Version Internal-M1.0.0a
Date:       Thu Feb 18 10:41:18 1999

Performance Summary:

Worst case Pad to Pad path delay  :     9.0ns (1 macrocell levels)
 (Includes an external input margin of 0.0ns.)
 (Includes an external output margin of 0.0ns.)
Pad 'X19' to Pad 'Y1'

--------------------------------------------------------------------------------
                Combinational Pad to Pad Delays(nsec)

\ From        B    B    C    C    X    X    X    X   X    X    X    X
 \                 B         C    0    1    1    1   1    1    1    1
  \                                     0    1   2    3    4    5
   \
    \
     \
```

```
      \
    To \-------------------------------------------------------------

Y1          7.5     7.5         7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5
Y2                              7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5
Y3              9.0      9.0
Y4

------------------------------------------------------------------------

               Combinational Pad to Pad Delays(nsec)

\ From        X    X    X    X    X    X    X    X    X    X    X    X
 \            1    1    1    1    2    3    4    5    6    7    8    9
  \           6    7    8    9
   \
    \
     \
      \
    To \-------------------------------------------------------------

Y1          7.5  7.5  9.0  9.0  7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5
Y2                             7.5  7.5  7.5  7.5  7.5  7.5  7.5 7.5
Y3
Y4

.

.

.
```

Path Type Definition:

Pad to Pad (tPD) - Reports pad to pad paths that start at input pads and end at output pads. Paths are not traced through registers.

Clock Pad to Output Pad (tCO) - Reports paths that start at input pads trace through clock inputs of registers and end at output pads. Paths are not traced through PRE/CLR inputs of registers.

Setup to Clock at Pad (tSU) - Reports external setup time of data to clock at pad. Data path starts at an input pad and end at register D/T input. Clock path starts at input pad and ends at the register clock input. Paths are not traced through registers.

Clock to Setup (tCYC) - Register to register cycle time. Include source register tCO and destination register tSU.

You can use the following path filtering commands to modify the scope of the Advanced Design Analysis report.

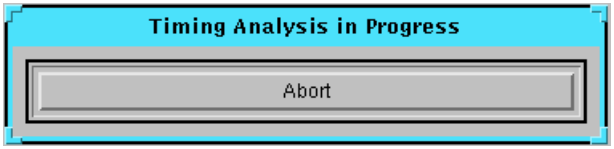
- Include Paths with Nets (Path Filters Menu)
- Exclude Paths with Nets (Path Filters Menu)
- Control Path Tracing (Path Filters Menu)

Custom Analysis

The Custom Analysis report displays a detailed analysis of all specified paths. It contains the worst-case path delays for all paths that are not filtered out.

To generate a Custom Analysis report, select **Analyze** → **Custom**, or click on the Custom button in the toolbar.

This command has an interrupt function when analyzing FPGA designs. A Timing Analysis in Progress dialog box with an Abort button appears.



Clicking the Abort button, the Esc key, or the Enter/Return key aborts the analysis. A report is neither generated nor displayed.

After processing the design, the Timing Analyzer displays the Custom Analysis report in a pop-up window. The contents of the window can be saved as a TWR file; see the "Saving a Report" section for the procedure to save a report. An example is shown following.

```
--------------------------------------------------------------------------------
Timing Analyzer 2.1i
Copyright (c) 1995-1999 Xilinx, Inc.  All rights reserved.

Design file:              C:\designs\loop.ncd
Device,speed:             xc4036ex,-3 (x1_0.08 3.7f )
Report level:            verbose report, limited to 1 item per constraint
--------------------------------------------------------------------------------


================================================================================
Timing constraint: PATH "PATHFILTERS" = FROM TIMEGRP "SOURCES" TO TIMEGRP
"DESTINATIONS" ;
 5 items analyzed, 0 timing errors detected.
 Maximum delay is  10.716ns.
--------------------------------------------------------------------------------
Delay:    10.716ns $1N11 to OUT

Path $1N11 to OUT contains 2 levels of logic:
Path starting from Comp: CLB.K (from $1N19)
To                    Delay type         Delay(ns)  Physical Resource
                                                    Logical Resource(s)
-------------------------------------------------  --------
CLB.XQ                Tcko                  1.830R  $1N11
                                                    $1N11
IOB.O                 net (fanout=2)     e  1.066R  $1N11
IOB.PAD               Tops                  7.820R  OUT
                                                    OUT.OUTBUF
                                                    OUT
-------------------------------------------------
Total (9.650ns logic, 1.066ns route)      10.716ns
      (90.1% logic, 9.9% route)
```

```
--------------------------------------------------------------------------------


All constraints were met.


Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock ck1_i
---------------+------------+------------+
               |  Setup to  |  Hold to   |
Source Pad     | clk (edge) | clk (edge) |
---------------+------------+------------+
res_i          |    6.202(R)|            |
start_i        |    2.213(R)|    0.000(R)|
---------------+------------+------------+
.
.
.


Table of Timegroups:
--------------------
TimeGroup SOURCES:
BELs:
 $1N11  OUT    D      C      CLR

TimeGroup DESTINATIONS:
BELs:
 $1N11  OUT    D      C      CLR



Timing summary:
---------------

Timing errors: 0  Score: 0

Constraints cover 5 paths, 0 nets, and 5 connections (100.0% coverage)


Design statistics:
```

```
   Maximum path delay from/to any node:  10.716ns

Analysis completed Wed Mar 3 14:31:19 1999
------------------------------------------------------------------------
```

You can use the following path filtering commands to modify the scope of the Custom Analysis report.

- Select Sources (Path Filters Menu)
- Select Destinations (Path Filters Menu)
- Include Paths with Nets (Path Filters Menu)
- Exclude Paths with Nets (Path Filters Menu)
- Control Path Tracing (Path Filters Menu)

Viewing a Report

When a Timing Analysis report (TWR file) is opened in the Timing Analyzer window, the report window contains three sub-windows, as shown in the following figure.

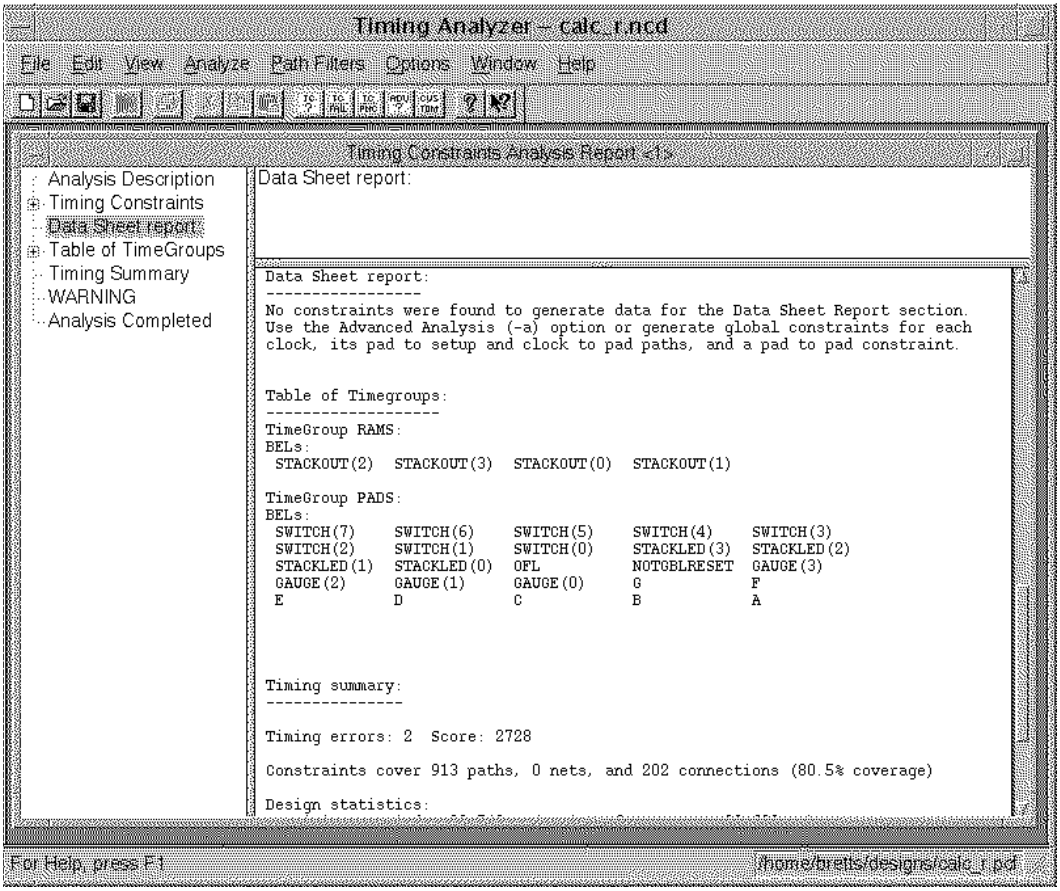


Figure 4-2 Timing Analyzer Report Window

The report itself is displayed in the lower right window. The upper right window shows what section of the report is currently displayed on the screen. As you scroll through the report, the section name in the upper right window automatically changes.

The window on the left contains a hierarchical display of the headings in the report. Selecting a heading causes the report to scroll immediately to that location. You can click on a box with a plus sign (+) in it to show the sections within that heading.

The size of the three windows can be adjusted as needed.

Saving a Report

Follow this procedure to save a generated report as a file.

1. Make sure the report that you want to save is the active window by clicking on it. The active window has a colored border.
2. Select **File** → **Save**, or click the Save button.

   The Timing Analyzer displays the Save As dialog box, illustrated in the "Save As Dialog Box" figure of the "Menu Commands" chapter.
3. Under List Files of Type, click on the down arrow to display the pull-down list box of available file types. Highlight Timing Analysis Reports (*.twr) to select it. File names of that format appear in the list box below the File Name field.
4. In the File Name field, type in the name of the file in which to store the report. The .twr extension is added automatically.

   If this is the first time you are saving the file, the Timing Analyzer provides a default name corresponding with the type of information contained in the window (timing constraints, clocks, and so forth).

   If you want to overwrite an existing file with the new report, click on that file name in the list box, so it appears in the File Name field.

   You can use word processor applications to open and edit the report file.
5. In the Save in field / Directories list box, select the directory in which you want to save the report.
6. Click **OK**.

   The Save As dialog box closes.

Searching for Text in a Report

You can use the Find command to search for any text string in the active report window, including normal grammatical symbols like hyphens or underscores. You cannot search for special characters like tabs or hard returns, however.

To search for a text string in a report, do the following.

1. Open or select the report window in which you want to search.
2. Select **Edit** → **Find**.

   The Find dialog box appears, as shown in the "Find Dialog Box" figure of the "Menu Commands" chapter.
3. Enter the text string that you want to search for in the Find What field.
4. You can optionally match the case of the search string by selecting Match Case. Then only instances that have the same case as the text string will be found. By default, case is ignored.
5. Indicate the search direction, as follows.
   - Up searches backward from the present location of the cursor to the beginning of the report. Searching stops at the beginning of the report.
   - Down searches forward from the present location of the cursor to the end of the report. Searching stops at the end of the report. This direction is the default.
6. Click the Find Next button, the F3 key, or select **Edit** → **Find Next** to find the next instance of the text string.
7. Click **Cancel** to close the Find dialog box.

Printing a Report

You can send a Timing Analyzer report to your default printer, or you can send it to a printer that you specify.

Note: Print dialog boxes vary between platforms and window operating systems. The procedure in this section is basic; consult your specific system documentation for details.

To send a report to the default printer, follow these instructions.

1. Select **File** → **Print**, or click the Print button.

   The Timing Analyzer displays the Print dialog box, shown in the "Print Dialog Box" figure of the "Menu Commands" chapter.

2. If you want to print more than one copy, enter the number of copies that you want to print in the Copies field.
3. If you want to print a range of pages, enter "From" and "To" pages in the corresponding boxes.
4. If you want to print to a file, select Print to File.
5. Click **OK**.

Closing a Report

To close a report, use one of the following methods.

Using Menu Commands

Select **File** → **Close**.

If the report has been previously saved, the window closes. If it has not been saved, the Save As dialog box appears; see the "Saving a Report" section for the procedure to save a report.

Using the Mouse

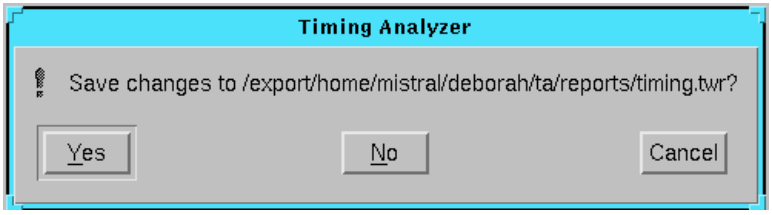
Make sure the report that you want to close is the active window by clicking on it. The active window will have a colored border.

1. Click on the horizontal bar in the upper left-hand corner of the report pop-up window.

   A pop-up menu appears.

2. Select **Close** from the menu.

   The following prompt box appears.



3. Click **Yes** to save the report window.

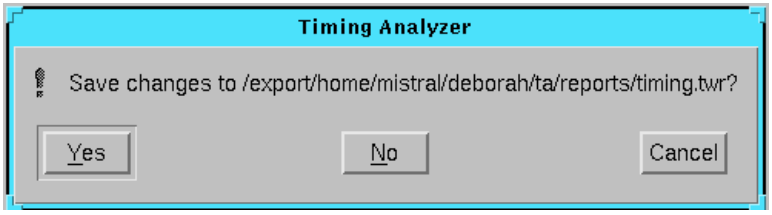
   The Save As dialog box appears; see the "Saving a Report" section for the procedure to save a report. If you click No, the dialog box and report window both close without saving. If you click Cancel, the dialog box closes and the report window remains open.

Using the Keyboard

Make sure the report that you want to close is the active window by clicking on it. The active window will have a colored border.

1. Type **Ctrl F4** from the keyboard.

   The following prompt box appears.



2. Click **Yes** to save the report.

   The Save As dialog box appears; see the "Saving a Report" section for the procedure to save a report. If you click No, the dialog box and report window both close without saving. If you click Cancel, the dialog box closes and the report window remains open.

Opening a Saved Report

You can open a previously saved report to view or print by following these steps.

1. Select **File** → **Open**.

The Open dialog box appears, as shown in the "Open Dialog Box" figure of the "Menu Commands" chapter.

2. In the Look in / Directories list box, click on the directory containing the report file to load.
3. In the List Files of Type field, select Timing Analysis Reports (*.twr) is selected. The default is Timing Analysis Macros (*.xtm).

   All the available report files are displayed in the list box (below the File Name field).
4. Select a report file from the list box, or type the name in the field below File Name after backspacing over the asterisk. If you do not specify a file extension, the Timing Analyzer loads an XTM (macro) file by default.
5. Click **OK**.

Specifying Report Appearance and Content

By default, the Timing Analyzer analyzes and reports on all paths in a design. However, you can determine the appearance and the content of the reports that the Timing Analyzer generates.

Perform the steps described in the following sections to customize generated reports. Each section describes a report output option you can specify.

1. Select **Options** → **Report Options**.

   The Timing Analyzer displays the Report Options dialog box, shown in the "Report Options Dialog Box" figure of the "Menu Commands" chapter.

   The following table lists each option in the dialog box and indicates if the option is available for FPGA or CPLD designs.

Option	FPGA	CPLD
Summary Only	Yes	No
No Limit	Yes	Yes
Limit Report To	Yes	Yes
Report Delays Less Than	No	Yes
Report Delays Greater Than	No	Yes

Option	FPGA	CPLD
Sort On	No	Yes
Report Only Longest Paths Between Points	No	Yes
Wide Report	Yes	Yes

2. After specifying all desired report options, click **OK**.

   The Report Options dialog box closes. You can now select additional filtering commands or generate a Timing Analysis report, as described in the "Timing Constraints Analysis" section.

Creating a Summary Report

Note: The Summary Only option only applies to FPGAs; it is disabled if a CPLD design is open.

To generate a summary report, select Summary Only in the Report Options dialog box. A summary report contains only the path source and end point. It lists one delay path per line and does not display cumulative delays.

Setting the Maximum Number of Paths Per Timing Constraint

To limit the total number of paths per timing constraint that the Timing Analyzer reports, select the Limit Report To radio button and enter a value in the Limit Report To field.

You can use this option with the criterion you specify in the Sort On field when generating an Custom Analysis report. For example, if you enter 10 in the Maximum Number of Paths per Timing Constraint field and set the Sort On option to Descending Delay, the Timing Analyzer reports the 10 paths with the longest delay.

You can optionally use a keyboard command to set this option.

1. Select **View** → **Console**.
2. In the field at the bottom of the Console window, type the following.

   MaxPathsPerTimingConstraint *number_of_paths*

   You can use this keyboard command in a macro.

Reporting Delays Less Than a Value

Note: This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

To instruct the Timing Analyzer to report only those paths that have a delay less than or equal to the specified value, enter a value, in nanoseconds in the Report Delays Less Than field of the Report Options dialog box. Make the field blank to include paths regardless of how large the delays are.

Reporting Delays Greater Than a Value

Note: This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

You can instruct the Timing Analyzer to report only those paths that have a delay greater than or equal to the specified value. To do so, enter a value, in nanoseconds, in the Report Delays Greater Than, field of the Report Options dialog box.

Sorting Path Report Order

Note: This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

You can specify how the Timing Analyzer sorts path types when they are reported. To specify how paths are sorted, click on the down arrow next to the Sort On field in the Report Options dialog box, and select a path type. See the "Report Options (Options Menu)" section of the "Menu Commands" chapter for descriptions of these delay path types.

- Ascending Delay
- Descending Delay
- Source Net
- Destination Net
- Source Clock Net
- Destination Clock Net

Reporting Only Longest Paths Between Points

Note: This option only supports analysis of CPLD designs; it is disabled if an FPGA design is open.

If there is more than one path between two end points, you can direct the Timing Analyzer to report only the path with the longest delay. Select Report Only Longest Paths Between Points in the Report Options dialog box.

Generating Wide Reports

By default, the Timing Analyzer generates a report formatted with 80 characters per line. To generate a wide report, select Wide Report. Wide reports have 132 characters per line. They help reduce the number of truncated net names, since names are truncated to 132 characters instead of 80 characters as in a default report.

Changing the Speed Grade

The speed grade is usually set during the design implementation process. Changing the speed grade helps you determine if you need to target a faster device to meet your timing requirements, or if using a slower speed grade still meets timing constraints.

Changing the speed grade may affect the worst case and range of values available in the Prorating Options dialog box.

Note: Changing the speed grade with the Timing Analyzer only affects analysis. The speed grade in the design file is not changed.

To change the speed grade for timing analysis, perform the following steps.

1. Select **`Options`** → **`Speed Grade`**.

   The Speed Grade dialog box appears, as shown in the “Speed Grade Dialog Box” figure of the “Menu Commands” chapter.

2. Select a speed grade from the list of available speed grades using one of the following methods. For families that support minimum speed grades, a Min selection is available in the speed grade list.

   - Using the mouse, click on the down arrow and select a speed grade from the pull-down list.

- Using the keyboard, tab until the speed grade is highlighted, and press the up or down arrow keys until the desired speed grade appears.

3. Click **OK**.

   The Speed Grade dialog box closes. You can now select additional filtering commands or generate a report.

Using Path Filtering Commands

By default, the Custom Analysis reports the path delays for all paths in the design. However, you can instruct the Timing Analyzer to analyze and report on a subset of paths by using commands in the Path Filters menu and it submenus.

The Path Filters menu consists of the Reset All Path Filters command and the Timing Constraint Filters, Custom Filters, and Common Filters submenus.

The types of commands contained in these submenus are described in the “Path Filtering Commands” section of the “Introduction” chapter. Also, see the “Specifying Report Appearance and Content” section for information on report format and general content customizing.

After using these commands to specify specific paths and to apply filters, you can generate reports using the commands in the Analyze menu. Refer to the “Creating Reports” section for more information on report generation.

The procedures in the following sections often direct you to specify a filter in a dialog box or to move items between list boxes. Refer to the “Using Filters with Commands” section and the “Moving Items in List Boxes” section of the “Getting Started” chapter for detailed instructions on specifying a filter and on selecting and moving items between list boxes.

Timing Constraint Filters

The Timing Constraints Filters submenu contains the Disable Timing Constraints command which you can use to prevent the Timing Analyzer from analyzing specific timing constraints. These commands function only if a design is loaded. They do not alter the Advanced Design Analysis report or the Custom Analysis report.

To prevent the Timing Analyzer from analyzing specified timing constraints, perform the following steps.

1. Select **Path Filters** → **Timing Constraint Filters** → **Disable Timing Constraints**.

   The Disable Timing Constraints dialog box appears, as shown in the "Disable Timing Constraints Dialog Box" figure of the "Menu Commands" chapter.

Note: If an FPGA design is open, the Include PCF Entered Constraints radio button is selected by default. Click the Omit PCF Entered Constraints radio button, if you want to include user constraints during analysis. User constraints are contained in the "USER" section of the PCF. These two buttons and their functions are only visible and available for FPGAs.

2. If you would like to display a subset of timing constraints, enter a filter string in the Filter field and click **Apply**.

   The subset of timing constraints is displayed in the Enabled Constraints list box. See the "Using Filters with Commands" section of the "Getting Started" chapter for valid filter inputs.

3. Select the timing constraints you want to exclude from the Timing Constraints Analysis report in the Enabled Constraints list box and move specific ones or all of them to the Disabled Constraints list box.

   See the "Moving Items in List Boxes" section of the "Getting Started" chapter for instructions on moving items between list boxes.

4. Click **OK**.

   The Disable Timing Constraints dialog box closes. You can now select another command or generate a Timing Constraints Analysis report.

Custom Filters

You can select starting points and ending points using commands described in this section to specify the scope of path analysis information reported in the Custom Analysis report. These commands are in the Custom Filters submenu of the Path Filters menu. By default, the

Timing Analyzer selects all sources and all destinations for path analysis.

Selecting Sources

To select specific sources for path analysis, follow these steps.

1. Select **Path Filters** → **Custom Filters** → **Select Sources**.

   The Select Sources dialog box appears, as shown in the "Select Sources Dialog Box" figure of the "Menu Commands" chapter.

2. Select the source type by clicking the down arrow of the Source Element Type pull-down list box to display the list of sources, then highlight it. The default is Flip-Flops.

   FPGA source types can be flip-flops, RAMs, latches, pads, nets, pins, CLBs, clocks or timegroups. CPLD source types can be flip-flops, pads, nets, macrocells, or clocks.

   If an element type is not used in the design, the type will not appear in the pull-down list.

   Element in the Filter field and the Source *Element* list box changes to match the source type you select.

3. If you select Clocks, specify the type of clock edge by clicking the down arrow and highlighting the selection in the Clock Edge field. Clocks are only supported for FPGA designs. These are the Clock Edge options.

   - Rising or Falling (either clock edge)
   - Rising
   - Falling

4. Enter some text in the Filter field to display a subset of the specified source type, if desired, and click **Apply**. See the "Using Filters with Commands" section of the "Getting Started" chapter for valid filter inputs.

5. Select the sources you want to include in Timing Analysis from the Source *Element* list box and move specific ones or all of them to the Selected Sources list box.

   See the "Moving Items in List Boxes" section of the "Getting Started" chapter for instructions on moving items between list boxes. The Select Sources dialog box utilizes a special way of

representing nets in the Source *element_type* and Selected Sources list boxes. The list boxes contain *All* or *All* [*element_type*] to represent all the nets in a category. For example, if you select *All* in the Source Flip-Flops list box and move it to the Selected Sources list box, it appears as *All* [Flip-Flops] to indicate that all the Flip-Flops are selected. You get the same result if you individually move all the Flip-Flop nets from the Source Flip-Flops to the Selected Sources list box.

6. Repeat steps 2 through 5 until you have moved all the desired types of elements to the Selected Sources list box.
7. Click **OK**.

   The Select Sources dialog box closes. You can now select another path filtering command or generate a timing report.

Selecting Destinations

To select specific destinations for path analysis, follow this procedure.

1. Select **Path Filters** → **Custom Filters** → **Select Destinations**.

   The Select Destinations dialog box appears, as the "Select Destinations Dialog Box" figure of the "Menu Commands" chapter illustrates.

2. Select the ending point type by clicking the down arrow of the Destination Element Type pull-down list box to display the list of destinations, then highlight it. The default is Flip-Flops.

   FPGA destination types can be flip-flops, RAMs, latches, pads, nets, pins, CLBs, clocks, or timegroups. CPLD destination types can be flip-flops, pads, nets, macrocells, or clocks.

   If an element type is not used in the design, the type will not appear in the pull-down list.

   Element in the Destination *Element* list box changes to match the destination type you select.

3. If you select Clocks, specify the type of clock edge by clicking the down arrow and highlighting the selection in the Clock Edge field. Clocks are only supported for FPGA designs. These are the Clock Edge options.

   - Rising or Falling (either clock edge)

- Rising
- Falling

4. Enter some text in the Filter field to display a subset of the specified source type, if desired, and click **Apply**. See the "Using Filters with Commands" section of the "Getting Started" chapter for valid filter inputs.
5. Select the destinations you want to include in Path Analysis from the Destination *Element* list box and move specific ones or all of them to the Selected Destinations list box.

   See the "Moving Items in List Boxes" section of the "Getting Started" chapter for instructions on moving items between list boxes. The Select Destinations dialog box utilizes a special way of representing nets in the Destination *element_type* and Selected Destinations list boxes. The list boxes contain *All* or *All* [*element_type*] to represent all the nets in a category. For example, if you select *All* in the Destination Flip-Flops list box and move it to the Selected Destinations list box, it appears as *All* [Flip-Flops] to indicate that all the Flip-Flops are selected. You get the same result if you individually move all the Flip-Flop nets from the Destination Flip-Flops to the Selected Destinations list box.
6. Repeat steps 2 through 5 until you have moved all the desired types of elements to the Selected Destinations list box.
7. Click **OK**.

   The Select Destinations dialog box closes. You can now select another path filtering command or generate a timing report.

Common Filters

You can include or exclude paths with nets or control path tracing using commands described in this section to specify the scope of timing analysis. These commands exist in the Common Filters submenu of the Path Analysis menu.

Although the Include Paths with Nets and Exclude Paths with Nets commands in the Common Filters submenu appear to be similar, they are not mutually exclusive. For example, you might want to exclude any path that goes through the synchronous Reset net of the counter but include all paths that go through bit 1 of the counter. By using the Exclude Paths with Nets command to exclude the synchronous Reset,

and the Include Paths with Nets command to include paths through the bit 1, you can include or exclude specific nets that are attached to the counter.

After using the path filtering commands in the Common Filters submenu, you can generate a Timing Constraints Analysis, Advanced Design Analysis, or Custom Analysis report.

Including Paths with Nets

Use the Include Paths with Nets command to limit analysis to paths that contain specified nets. If a net is not selected, paths through that net are not analyzed. However, if no nets are selected, which is the default, all paths, except those subject to other filtering commands, are analyzed. To select nets to be included for analysis, use this procedure.

1. Select **Path Filters** → **Common Filters** → **Include Paths with Nets**.

   The Include Paths with Nets dialog box appears, as shown in the "Include Paths with Nets Dialog Box" figure of the "Menu Commands" chapter.

2. Enter some text in the Filter field to display a subset in the Available Nets list box, if desired, and click **Apply**.

   See the "Using Filters with Commands" section of the "Getting Started" chapter for valid filter inputs.

3. Select the nets that you want to include in your timing analysis from the Available Nets list box and move specific ones or all of them to the Selected Nets list box.

   See the "Moving Items in List Boxes" section of the "Getting Started" chapter for instructions on moving items between list boxes.

4. Click **OK**.

   The Include Paths with Nets dialog box closes. You can now select another path filtering command or generate a timing report.

Excluding Paths with Nets

Use the Exclude Paths with Nets command to exclude paths containing specific nets from analysis, regardless of which paths are specified in the Include Paths with Nets command or other filters. If a net is selected, paths through that net are not analyzed. The default does not exclude any nets from analysis. To exclude specific nets from analysis, use this procedure.

1. Select **Path Filters** → **Common Filters** → **Exclude Paths With Nets**.

   The Exclude Paths with Nets dialog box appears, as shown in the "Exclude Paths with Nets Dialog Box" figure of the "Menu Commands" chapter.

2. Enter some text in the Filter field to display a subset in the Available Nets list box, if desired, and click **Apply**.

   See the "Using Filters with Commands" section of the "Getting Started" chapter for valid filter inputs.

3. Select the nets that you want to exclude from your timing analysis from the Available Nets list box and move specific ones or all of them to the Selected Nets list box.

   See the "Moving Items in List Boxes" section of the "Getting Started" chapter for instructions on moving items between list boxes.

4. Click **OK**.

   The Exclude Paths with Nets dialog box closes. You can now select another path filtering command or generate a timing report.

Controlling Path Tracing

Use the Control Path Tracing command to enable or disable path analysis through delay path types for specific components, such as latches, RAMs, and TBUFs. These paths may be irrelevant to your analysis.

Note: This command only applies to FPGAs; it is disabled if a CPLD design is open. (CPLD path timing analysis ignores paths through Set/Reset logic and breaks paths at bidirectional I/O pins.)

After specifying which path types to control through which components, you can generate a Timing Constraints Analysis, Advanced Design Analysis, or Custom Analysis report. Use the following procedure to specify path types through components for path analysis.

1. Select **Path Filters** → **Common Filters** → **Control Path Tracing**.

   The Timing Analyzer displays the Control Path Tracing dialog box, illustrated in the "Control Path Tracing Dialog Box" figure of the "Menu Commands" chapter.

2. Select the path type that you want to control from the Path Type pull-down list box. Click on the down arrow, then highlight one of the path types. The following types are available; see the "Control Path Tracing (Path Filters Menu)" section of the "Menu Commands" chapter for details on these path types.

   - Asynchronous Set/Reset to Output
   - Data to Output for Transparent Latch
   - RAM Data to Output
   - RAM WE (Write Enable) to Output
   - TBUF Tristate Control to Output
   - TBUF Input to Output
   - I/O Pad to Input
   - I/O Tristate Control to Pad
   - Bidirectional Tristate I/O Output to Input
   - I/O Output to Pad

   The Timing Analyzer displays all components that use the specified path type in the Enabled Components or Disabled Components list box, corresponding with the default of that path type. The path type default is the state when you initially open a design or use the Reset All Path Filters command.

3. Enter some text in the Filter field to display a subset of components of the specified type, if desired, and click **Apply**.

   The Filter changes to match the default state of the path type. See the "Using Filters with Commands" section of the "Getting Started" chapter for valid filter inputs.

4. Select the components that you want to enable or disable by moving them from the Enabled Components to the Disabled Components list box or vice versa.

   See the "Moving Items in List Boxes" section of the "Getting Started" chapter for instructions on moving items between list boxes.

5. Click **OK**.

   The Control Path Tracing dialog box closes. You can now select another filtering command or generate any timing report.

Resetting Path Filters to Defaults

You can reset all of the path filters to the design default settings. After opening a design, select **Path Filters** → **Reset All Path Filters**. To then view the default settings, select **View** → **Settings**.

Using the Console Window

The Console window records all the commands that you have used in a Timing Analyzer session. You can use these commands to form macros, as described in the "Creating a Macro" section. In addition, it provides an alternative to using some menu commands by allowing you to enter commands from the keyboard.

Executing a Command

To execute a command in the Console window, follow these steps.

1. To open the Console window, select **View** → **Console**.

   The Console window appears, as shown in the "Console Window" figure of the "Menu Commands" chapter.

Note: You cannot delete text from within the Console window.

2. You can add a command manually by typing it in the field at the bottom of the window below the Show Command Status box. Use the syntax given for the command in the "Command Line Syntax" chapter. After you enter the command and press the Return key, the command is executed and is reflected in the Console window.

Re-Executing Commands

If you want to re-execute a command shown in the Console window, you can use one of the following three methods in the field at the bottom of the window below the Show Command Status box.

- Type two exclamation points (!!) to repeat the last command.
- Type an exclamation point (!) and the number of the command that appears to the left of the command in the Console window.
- Type in an exclamation point (!) and the first letter or first few letters of the command.
- Use the up or down arrow keys to move to the command, select it, and press the Return key.

With all these methods, the Timing Analyzer starts the search from the bottom of the command list.

To see if the system issued a response to the command, such as an error or warning message, click the **Show Command Status** box.

Using Macros

A macro command is a script file for running Timing Analyzer commands and options. You can create a macro, save it in a new file, the same file, or another existing file, and run it in the Console window. The Timing Analyzer records all commands executed during the current session.

Creating a Macro

To create a macro, perform the following steps.

1. Select **View** → **Console** to open the Console window.

   Alternatively, you can create or edit a macro manually or create one by entering keyboard commands in a text file.

2. From the menus, select the commands that will constitute the macro or type keyboard commands in the field at the bottom of the window.

   These commands are recorded in the Console window numerically. See the “Command Line Syntax” chapter for listings,

descriptions, syntax, abbreviations, and examples of keyboard commands.

3. Select **`File`** → **`New Macro`** or click the New Macro button.

A New Macro window appears.

4. In the Console window, hold down the left mouse button and highlight the sequence of commands that will constitute the macro.
5. Click the Copy Button.

6. Position the cursor in the New Macro window and click the Paste Button.

The lines from the Console window are pasted into the New Macro window.

You can also highlight, copy, and paste individual lines from the Console window to the New Macro window.

You can add text in the New Macro window by inserting the cursor and typing. Delete text by pressing the backspace key or by highlighting and pressing the Delete key.

7. Save the new macro by following the instructions in the “Saving a New Macro” section.

Saving a New Macro

To save a new macro, follow these steps.

1. Make sure the macro that you want to save is the active window by clicking on it. The active window has a colored border.
2. Select **File** → **Save**, or click the Save button.

The Save As dialog box, appears as shown in the "Save As Dialog Box" figure of the "Menu Commands" chapter.

3. In the Look in / Directories list box, select the directory in which you want to save the macro.
4. In the List Files of Type field, make sure that Timing Analysis macros (*.xtm) is selected. (File names of that format appear in the list box below the File Name field).

   A default name corresponding with the type of information contained in the window (timing constraints, clocks, and so forth), with an .xtm extension appears in the File Name field.
5. In the File Name field, type in a name for your new macro.

   You must save the macro in a file with an .xtm extension.
6. Click **OK**.

   The Save As dialog box closes. You can use word processor applications to open and edit the report file.

Running a Macro

Follow these instructions to run an existing macro.

1. Select **File** → **Run Macro**.

   The Run Macro dialog box appears as shown in the "Run Macro Dialog Box" figure of the "Menu Commands" chapter.
2. In the Look in / Directories list box, select the directory in which the macro file is located. All macro files with an XTM extension are listed in the list box.
3. Click on the macro file in the list box that you want to run.
4. Click **Open**.

To run a macro already displayed in an editor window, follow these instructions.

1. Click on the window to make it the active window.
2. Click the Run Macro toolbar button.

Editing a Macro

You can also edit an existing macro.

1. Select **File** → **Open**.

   The Open dialog box appears and is shown in the "Open Dialog Box" figure of the "Menu Commands" chapter.

2. In the Look in / Directories list box, select the directory in which the macro file is located.
3. In the List Files of Type field, select Timing Analysis Macros (*.xtm) from the pull-down list box.
4. In the File Name field, type in the name of the macro file that you want to open. Alternatively, click on the name of the XTM file in the list box above the File Name field.
5. Click **OK**.

   The Open dialog box closes, and the macro window opens and remains active.

6. Edit the macro, using the information in the "Creating a Macro" section to add, delete, copy, and paste commands in the macro window.
7. If you want to save the edited macro in the same file, select **File** → **Save**, or click the Save button.

If you have saved the macro once, the Save command saves the macro in the existing file without activating the Save As dialog box.

If you want to save the edited macro to another file, follow the instructions in the "Saving an Edited Macro to a New File" section.

Overwriting an Existing Macro

If you want to save an edited macro in the same file, follow these steps.

1. Make sure the macro that you want to save is the active window by clicking on it or opening the macro file.
2. Select **File** → **Save**, or click the Save button.

   The Save As dialog box appears as shown in the "Save As Dialog Box" figure of the "Menu Commands" chapter.
3. In the Look in / Directories list box, select the directory in which the existing macro is located.
4. In the List Files of Type field, make sure that Timing Analysis macros (*.xtm) is selected. (File names of that format appear in the list box below the File Name field).
5. In the File Name field, type in a name of the existing macro, or click on that file name in the list box below the File Name field.
6. Click **OK**.

   The Timing Analyzer displays a prompt box asking if you want to overwrite the existing file, as shown in the following figure.

Saving an Edited Macro to a New File

Follow this procedure to save an edited macro to another file.

1. Make sure the macro that you want to save is the active window by clicking on it or opening the macro file.
2. Select **File** → **Save**, or click the Save button.

   The Save As dialog box appears, as shown earlier in “Save As Dialog Box” figure of the “Menu Commands” chapter.
3. In the Look in / Directories list box, select the directory in which you want to save the macro.
4. In the List Files of Type field, make sure that Timing Analysis macros (*.xtm) is selected. (File names of that format appear in the list box below the File Name field).

   A default name corresponding with the type of information contained in the window (timing constraints, clocks, and so forth), with an .xtm extension appears in the File Name field.
5. In the File Name field, type in a name for new macro.

   You must save the macro in a file with an .xtm extension.
6. Click **OK**.

   The Save As dialog box closes. You can use word processor applications to open and edit the report file.

Suppressing Informational Messages

When you run a macro, the commands in the macro file can generate informational, confirmational, and error messages. However, you can suppress the informational and confirmational messages by using the following procedure. You cannot suppress these messages while executing menu commands. This command does not have an equivalent menu command.

1. Open a design, as described in the "Opening a Design" section.
2. Select **View** → **Console**.

   The Console window appears.
3. In the field at the bottom of the Console window, below Show Command Status, type the following command.

   SetForce on
4. If you are creating a new macro or editing an existing one, follow the procedure in the "Creating a Macro" section, inserting the **SetForce on** command when you want to suppress messages. (For example, after opening a design.)
5. Select **File** → **Run Macro**, or click the Run Macro Button.

   
6. To restore the informational and confirmational messages, type the following command in the Console window.

   SetForce off

Chapter 5

Menu Commands

This chapter lists and describes the commands available in the Timing Analyzer menus. This chapter contains these main sections.

- “Menus”
- “Commands”
- “Toolbar”

Menus

This section provides an overview of the Timing Analyzer menus.

File Menu

The File menu contains commands that load designs, physical constraints files, and macros. Commands that save and print reports on designs, and exit the Timing Analyzer. The commands on the File menu are the following.

New Macro	Creates new macro
Open Design	Loads design (NCD for FPGA, VM6 for CPLD) and default physical constraints file (FPGA only) for timing analysis
Open Physical Constraints	Loads file (PCF)
Open	Loads report (TWR), macro (XTM) or other text files
Close	Closes active file
Save	Saves report, macro, or other text files
Save As	Saves file in active window to another file

Run Macro	Runs specified macro
Print	Sends file in active window to default printer
Recent Design	Lists last four opened design files
Recent Physical Constraints	Lists last four opened physical constraints files
Recent Macro	Lists last four opened Timing Analyzer macros
Recent Report	Lists last four opened Timing Analyzer reports
Recent File	Lists last four opened files
Exit	Exits the Timing Analyzer

Edit Menu

The Edit menu is visible and enabled only if a design, macro, or report window is open.

Cut	Cuts selected text
Copy	Copies selected text
Paste	Pastes cut or copied text
Find	Finds specified text
Find Next	Finds next occurrence of specified text

View Menu

The View menu contains commands that control the appearance of Timing Analyzer window.

Toolbar	Displays or hides toolbar
Status Bar	Displays or hides status bar
Console	Displays or hides Console window
Clocks	Displays or hides clocks in the active design

Settings	Displays or hides current command settings
Font	Specifies the font used for displaying clocks, settings, and reports

Analyze Menu

The Analyze menu contains commands that generate timing analysis reports according to current Timing Analyzer commands and option settings.

Timing Constraints → Report Paths in Timing Constraints	Generates a timing constraints analysis report for all paths covered by timing constraints
Timing Constraints → Report Paths Failing Timing Constraints	Generates a timing constraints analysis report only for paths failing timing constraints
Timing Constraints → Report Paths Not Covered by Timing Constraints	Generates a timing constraints analysis report for all paths covered and not covered by timing constraints
Advanced Design	Generates a report that indicates the overall design performance by clock
Custom	Generates a detailed report of the delay paths specified using custom and common filters
Query	Displays timing information about net delays or time groups

Path Filters Menu

The Path Filters menu contains commands that enable you to select a subset of information when generating a timing report.

Timing Constraint Filters → Disable Timing Constraints	Specifies timing constraints to be ignored
Custom Filters → Select Sources	Defines path starting points

Custom Filters → Select Destinations	Defines path ending points
Common Filters → Include Paths with Nets	Includes specific paths in analysis
Common Filters → Exclude Paths with Nets	Excludes specific paths from analysis
Common Filters → Control Path Tracing	Controls tracing through specified components
Reset All Path Filters	Resets all path filters to default settings

Options Menu

The Options menu contains commands that you can use to change the speed grade for analysis and report options.

Speed Grade	Changes speed grade for analysis
Prorating Options	Controls voltage and temperature prorating
Report Options	Determines format and content of reports
Do Hold / Race Check	Checks for race conditions and does a rigorous clock skew analysis on the design

Window Menu

The Window menu contains commands that control the placement of the windows on the main screen.

Cascade	Arranges open windows diagonally
Tile	Arranges open windows in rows
Arrange Icons	Arranges icons in row at bottom of the Timing Analyzer window
Recent Window	Expands and / or brings to the front view the window that you select from a list of recently used active windows

Help Menu

The Help menu contains commands that enable you to access online help for the Timing Analyzer.

Help Topics	Lists online help topics
Online Documentation	Opens a browser window that points to the software manuals on the Web
About Timing Analyzer	Shows current software version

Commands

This section describes in alphabetical order all the Timing Analyzer menu commands.

About Timing Analyzer (Help Menu)

The About Timing Analyzer command displays a pop-up window that displays the version number of the Timing Analyzer software.

Advanced Design (Analyze Menu)

The Advanced Design command generates the Advanced Design Analysis report which provides a set of summary statistics for the paths from the timing requirements submitted for analysis. This report is essentially an error report that displays a summary header for each constraint whether it passes or not and lists paths in error for constraints that are violated.

For FPGAs, this report displays the results of analyzing the constraints specified in the constraints file. If no constraints are specified, this report displays the maximum clock frequencies for all clocks in the design and the worst-case timing for all clock paths. For CPLDs, this report displays all external pad-to-pad (tPD), clock pad-to-output pad (tCO), setup-to-clock-the-pad delays (tSU), and internal clock-to-setup (tCYC) delays.

You can use the following path filtering commands to modify the scope of this report.

- Include Paths with Nets (Path Filters Menu)
- Exclude Paths with Nets (Path Filters Menu)

- Control Path Tracing (Path Filters Menu)

Arrange Icons (Window Menu)

The Arrange Icons command arranges the Timing Analyzer window icons in a row along the bottom of the window.

Cascade (Window Menu)

The Cascade command arranges the open windows diagonally down the screen so that they overlap one another, as shown in the next figure. The active window is on top.

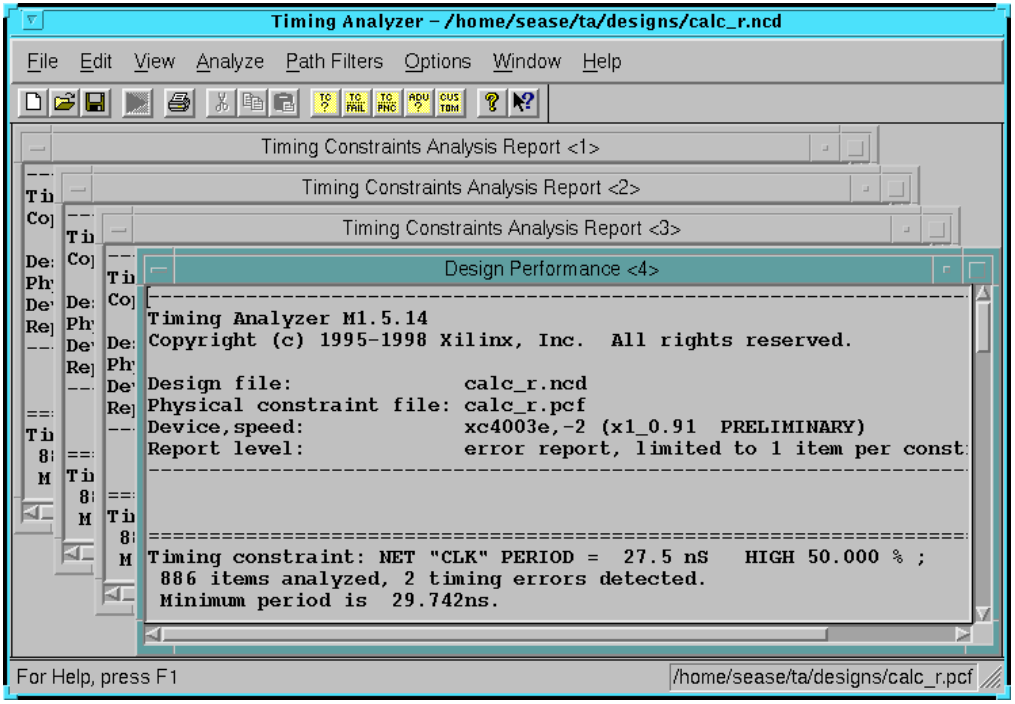


Figure 5-1 Cascaded Windows

Clocks (View Menu)

The Clocks command creates the Clocks report, which lists the names of all clocks in the design.

Close (File Menu)

The Close command closes the active report, macro, or design file.

Common Filters Submenu (Path Filters Menu)

Common Filters is a submenu in the Path Filters menu, which contains the following filtering commands that can be used to generate Timing Analysis, Design Performance, and All Paths reports.

- Include Paths with Nets (Path Filters Menu)
- Exclude Paths with Nets (Path Filters Menu)
- Control Path Tracing (Path Filters Menu)

Refer to the alphabetical listings of these commands for an explanation of their functions.

Console (View Menu)

The Console command displays the Console window, shown in the next figure, which records all the commands that you have used in a Timing Analyzer session.

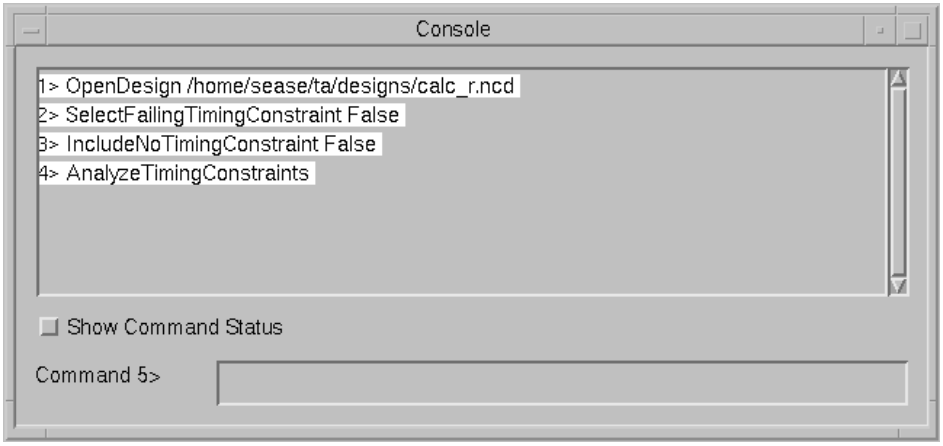


Figure 5-2 Console Window

Note: You cannot delete text from the Console window.

You can add a command manually by typing it in the field at the bottom of the window, below the Show Command Status box. Use the syntax for the command listed in the "Command Line Syntax" chapter of this manual. After you enter the command and press the Return key, the command is executed and is reflected in the Console window.

If you want to re-execute a command shown in the Console window, you can use one of the following four methods in the field at the bottom of the window.

- Use the up or down arrow keys to move to the command, and press the Return key.
- Type an exclamation point (!) and the number of the command.
- Type an exclamation point (!) and the first letter or first few letters of the command name.
- Type two exclamation points (!!) repeats the last command.

With all of these methods, the Timing Analyzer starts the search for the command from the last executed command in the list.

When you click on the Show Command Status box, the Timing Analyzer displays any responses to a command, such as an error or warning message.

Control Path Tracing (Path Filters Menu)

The Control Path Tracing command controls path tracing through RAM, tristate buffers, input and output pins, and Set/Reset logic. These paths may be irrelevant to your analysis. This command appears in the Common Filters submenu.

Note: This command only applies to FPGAs; it is disabled if a CPLD design is open. (CPLD path timing analysis ignores paths through Set/Reset logic and breaks paths at bidirectional I/O pins.)

Use this command in conjunction with any of the following reports.

- Timing Constraints Analysis report, which compares the implementation of the design to the constraints
- Advanced Design Analysis report, which indicates overall design performance

- Custom Analysis report, which contains detailed timing information for all paths in the design

The Control Path Tracing command displays the Control Path Tracing dialog box, shown in the next figure.

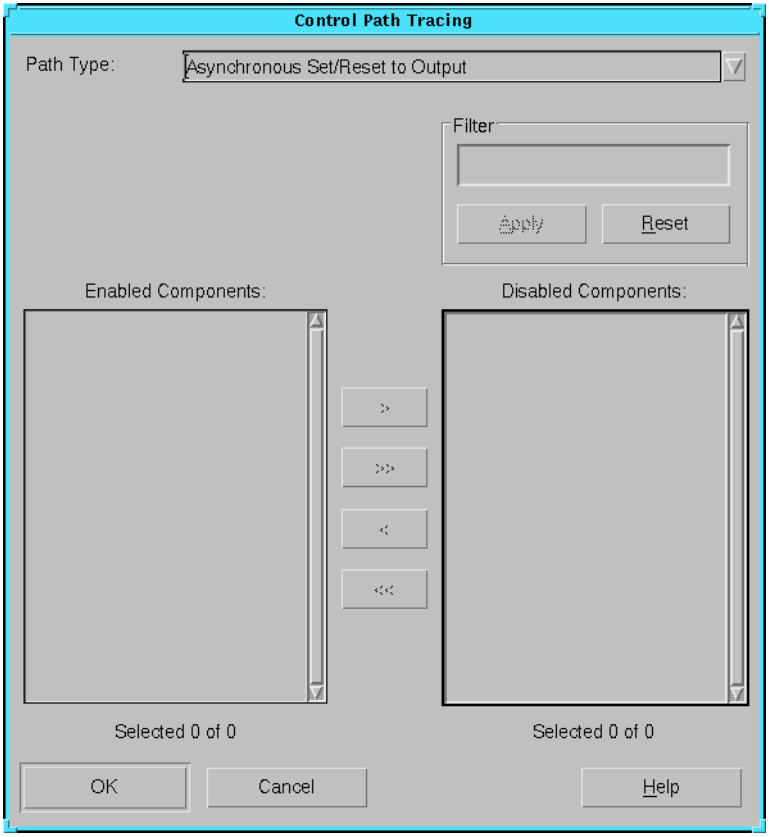


Figure 5-3 Control Path Tracing Dialog Box

This dialog box contains these fields.

- Path Type specifies paths that the Timing Analyzer can trace. The paths can be the following.
  - Asynchronous Set / Reset to Output enables path tracing through CLB flip-flop asynchronous Set or Reset outputs. By default, the Timing Analyzer does not analyze these paths.

- Data to Output for Transparent Latch enables path tracing from the latch D input to the Q output. By default, the Timing Analyzer does not analyze these paths.
- RAM Data to Output enables path tracing through the data inputs of a CLB RAM. By default, the Timing Analyzer does not analyze these paths.
- RAM WE to Output disables path tracing through the write-enable input of a CLB RAM. By default, the Timing Analyzer analyzes these paths.
- TBUF Tristate Control to Output disables tracing of paths that pass through a T pin to the O pin. By default, the Timing Analyzer analyzes these paths.
- TBUF Input to Output disables path tracing from the input pin to the output pin of a TBUF. By default, the Timing Analyzer analyzes these paths.
- I/O Pad to Input disables path tracing from the pad pin to the input pin of an IOB. By default, the Timing Analyzer analyzes these paths.
- I/O Tristate Control to Pad disables path tracing from the tristate control pin of an IOB to the pad, or if the architecture supports it, the path through the data input to output of the tri-state enable latch. By default, the Timing Analyzer analyzes these paths.
- Bidirectional Tristate I/O Output to Input disables tracing of paths that pass from the IOB O pin to the pad and back into the chip through the IOB I pin. By default, the Timing Analyzer analyzes these paths, but is disabled for tristate IOBs.
- I/O Output to Pad disables path tracing from the output pin of an IOB to the pad pin. By default, the Timing Analyzer analyzes these paths.

If you select a path type, the Timing Analyzer displays all components of that type in the Enabled Components or the Disabled Components list box, depending on the default state of that path type. In the following table, the Abbreviation column lists path type abbreviations as they appear in the Physical Constraints File

(PCF). The Path Type column textually describes the path type. The Default column refers to the default state of the path type.

Table 5-1 Control Path Tracing Path Types

Abbreviation	Path Type	Default
reg_sr_q	Asynchronous Set/Reset to Output	Disabled
lat_d_q	Data to output for transparent latch	Disabled
ram_d_o	RAM data to output	Disabled
ram_we_o	RAM WE to output	Disabled
tbuf_t_o	TBUF tristate control to output	Enabled
tbuf_i_o	TBUF input to output	Enabled
io_pad_i	I/O pad to input	Enabled
io_t_pad	I/O tristate control to pad	Enabled
io_o_i	Bidirectional tristate I/O output to input	Enabled
io_o_pad	I/O output to pad	Enabled

- Filter — filters the components that the Timing Analyzer traces paths through to those you specify. The location of the Filter and associated Apply and Reset buttons are either on the left or the right side of the Control Path Tracing dialog box depending on the Path Type you have selected in the Path Type pull-down menu.
  - Apply removes the components that do not match the filter from the list box located directly below the Filter.
  - Reset deletes the filter and redisplays all components with the Path Type default state in the list box located below the filter except those displayed in the other list box.
- Enabled Components — if you have not applied a filter, Enabled Components lists all the components for which tracing of the selected path type is enabled. If you applied a filter, this “filtered” list displays components that have path tracing enabled. However, some of the enabled components may be hidden when the filter was applied.
- Disabled Components — if you have not applied a filter, Disabled Components lists all the components for which tracing of the selected path type is disabled. If you applied a filter, this

"filtered" list displays components that have path tracing disabled; however, some of the disabled components may be hidden when the filter was applied.

- Add (>) moves the selected component from the Enabled Components list box to the Disabled Components list box.
- Add All (>>) moves all the listed components from the Enabled Components list box to the Disabled Components list box.
- Remove (<) moves the selected component from the Disabled Components list box to the Enabled Components list box.
- Remove All (<<) moves all listed components from the Disabled Components list box to the Enabled Components list box.

Copy (Edit Menu)

The Copy command functions like the standard Copy command; it copies highlighted text to the clipboard. The Edit menu is visible and enabled only if a design, macro, or report window is open.

Custom Filters Submenu (Path Filters Menu)

Custom Filters is a submenu in the Path Filters menu, which contains the following commands that allow you to the define paths you want to analyze.

- Select Sources (Path Filters Menu)
- Select Destinations (Path Filters Menu)

These commands apply to the Custom command in the Analyze menu that produces the Custom Analysis report. Refer to the alphabetical listings of these commands for an explanation of their functions.

Custom (Analyze Menu)

The Custom command generates the Custom Analysis report, which contains a detailed analysis of all specified paths. Filters from the Custom Filters and Common Filters submenus are applied during analysis to generate this report.

You can use the following path filtering commands to modify the scope of this report.

- Select Sources (Path Filters Menu)
- Select Destinations (Path Filters Menu)
- Include Paths with Nets (Path Filters Menu)
- Exclude Paths with Nets (Path Filters Menu)
- Control Path Tracing (Path Filters Menu)

Cut (Edit Menu)

The Cut command functions like the standard Cut command; it cuts highlighted text and moves it to the clipboard. The Edit menu is visible and enabled only if a design, macro, or report window is open.

Disable Timing Constraints (Path Filters Menu)

The Disable Timing Constraints command omits selected timing constraints from analysis. This command appears in the Timing Constraint Filters submenu.

Use this path filtering command in conjunction with the Timing Constraints Analysis report, which compares the implementation of the design to the constraints. And with the Advanced Design Analysis report, which provides a set of summary statistics for the paths from the timing requirements specified for analysis.

This command displays the Disable Timing Constraints dialog box, shown in the following figure.

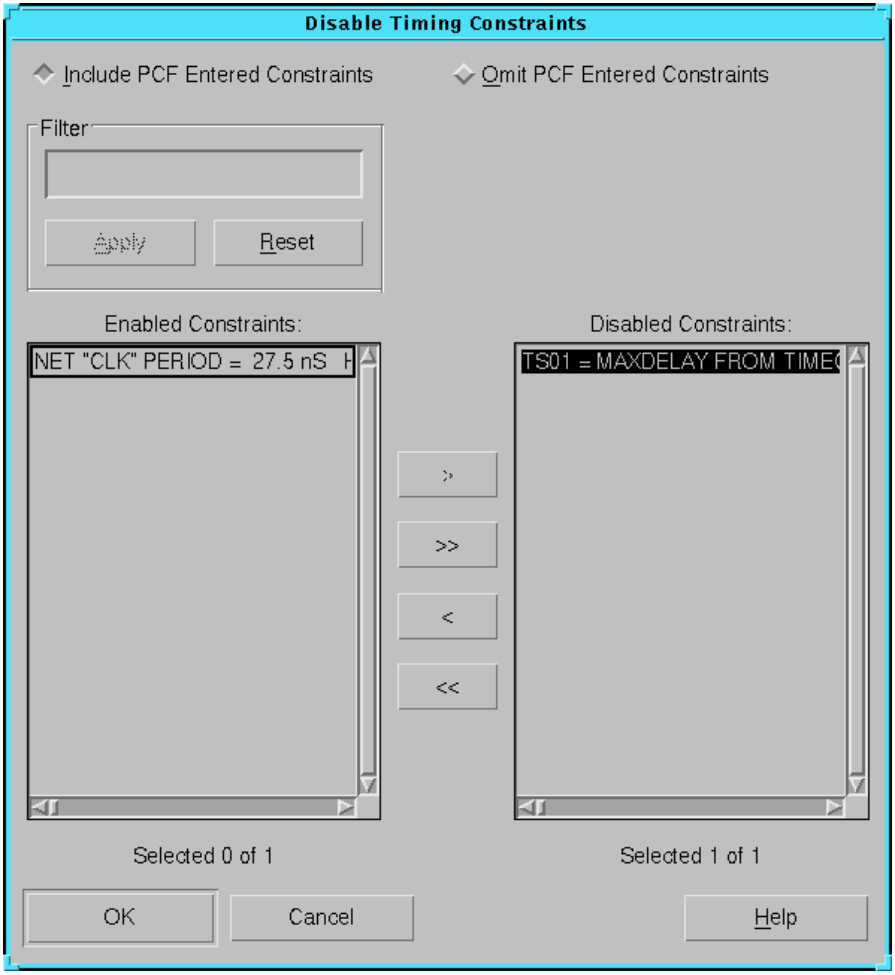


Figure 5-4 Disable Timing Constraints Dialog Box

The dialog box contains these buttons and fields.

- Include PCF Entered Constraints — this radio button is automatically selected because the Timing Analyzer, by default, analyzes all constraints. This radio button enables all of the timing constraints from the “USER” section of the Physical Constraints File (PCF). The “USER” section of the PCF file consists of the constraints entered into the PCF file after the “SCHEMATIC END” statement. The order of the timing constraints in the PCF

file is reflected by the Timing Analyzer. This option is only available for FPGAs. CPLD timing constraint information is contained in the design file (VM6) itself.

- Omit PCF Entered Constraints — this radio button disables all of the timing constraints from the "USER" section of the Physical Constraints File (PCF). This option is only available for FPGAs.
- Filter limits the timing constraints displayed in the Enabled Constraints list box to those you specify. You can include a "?" or an "*" wildcard in the component name for the filter to use in searches. The "?" represents a single character; the "*" represents zero or more characters.
  - Apply executes the filter indicated in the Filter field and displays the subset in the Enabled Constraints list box.
  - Reset deletes the filter and redisplays all the enabled timing constraints in the Enabled Constraints list box.
- Enabled Constraints lists the timing constraints to be included in the timing analysis, except those that you specified in the Filter field. If you do not specify a filter, it lists all the timing constraints in the design except those displayed in the Disabled Constraints list box.
- Disabled Constraints lists all the timing constraints to be ignored in the current timing analysis.
- Add (>) moves the selected timing constraint from the Enabled Constraints list box to the Disabled Constraints list box.
- Add All (>>) moves all listed timing constraints from the Enabled Constraints list box to the Disabled Constraints list box.
- Remove (<) moves the selected timing constraint from the Disabled Constraints list box to the Enabled Constraints list box.
- Remove All (<<) moves all listed timing constraints in the Disabled Constraints list box to the Enabled Constraints list box.

Do Hold/Race Check (Options Menu)

The Do Hold / Race Check command is a check box (toggle) item in the Options menu. When enabled, it checks for race conditions and does a rigorous clock skew analysis on the design.

Note: The command is only enabled for FPGA designs.

Exclude Paths with Nets (Path Filters Menu)

The Exclude Paths with Nets command excludes paths containing specified nets from timing analysis, regardless of what paths are specified in the Include Paths with Nets command or other path filtering commands. If a net is selected, paths through that net are not analyzed. The default does not exclude any nets from analysis. This command appears in the Common Filters submenu.

Use this path filtering command in conjunction with any of the following reports.

- Timing Constraints Analysis report, which compares the implementation of the design to the constraints
- Advanced Design Analysis report, which indicates overall design performance
- Custom Analysis report, which contains detailed timing information for all paths in the design

This command displays the Exclude Paths with Nets dialog box, shown in the next figure.

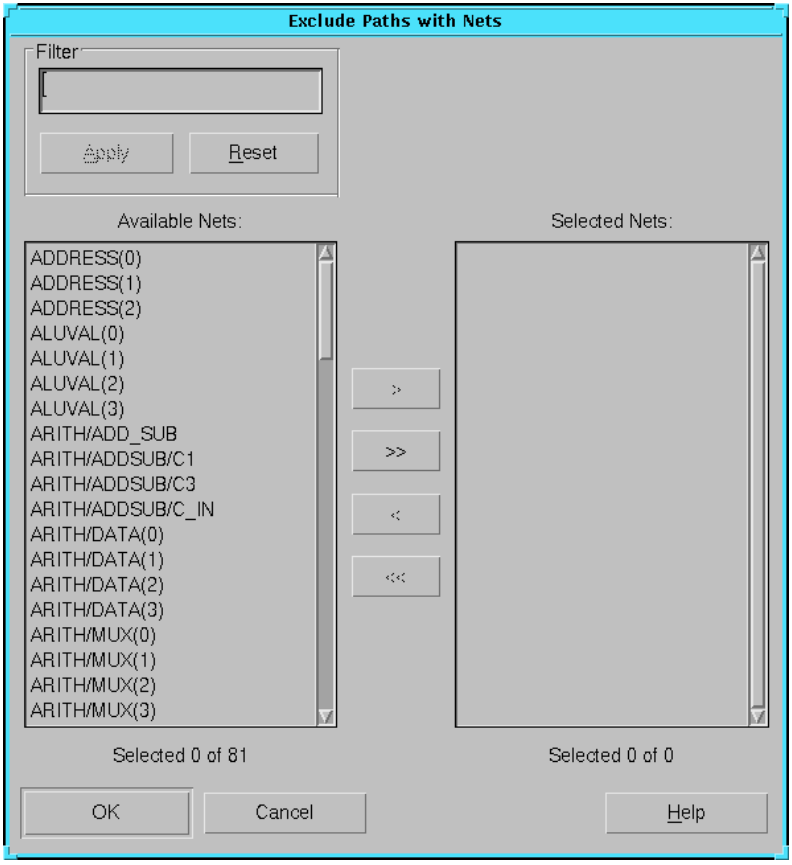


Figure 5-5 Exclude Paths with Nets Dialog Box

This dialog box includes the following fields and buttons.

- Filter limits the nets displayed in the Available Nets list box to those you specify. You can include a “?” or an “*” wildcard in the net name for the filter to use in searches. The “?” represents a single character; the “*” represents zero or more characters.
    - Apply executes the filter specified in the Filter field, which hides all nets in the Available Nets list box that do not match the filter.

- Reset deletes the filter and displays all the nets, except those that have been moved to the Selected Nets list box, in the Available Nets list box.

- Available Nets lists the nets that are available to be excluded from timing analysis. These are all the nets in the design except those that are hidden after applying a filter in Filter list box or those you move to the Selected Nets list box.
- Selected Nets lists the net to be excluded from timing analysis.
- Add (>) moves selected nets from the Available Nets list box to the Selected Nets list box.
- Add All (>>) moves all the listed nets from the Available Nets list box to the Selected Nets list box.
- Remove (<) moves selected nets from the Selected Nets list box to the Available Nets list box.
- Remove All (<<) moves all listed nets from the Selected Nets list box to the Available Nets list box.

Exit (File Menu)

The Exit command exits the Timing Analyzer. If you have unsaved reports or macros open, the following prompt box appears, so you can save them.

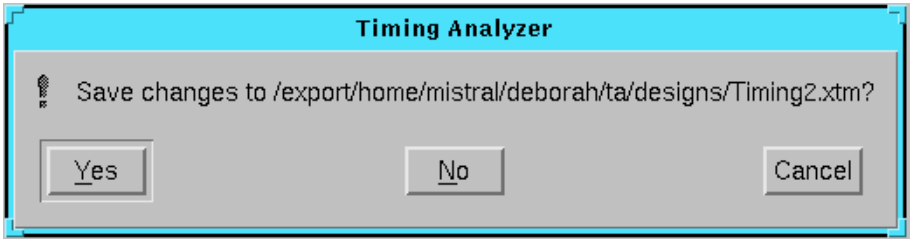


Figure 5-6 Exit Dialog Box

The three options in this prompt box are the following.

- Yes — If unsaved reports or macros are open, displays the Save As dialog box, shown in the “Save As Dialog Box” figure, so you can specify a file name.
- No — Exits the Timing Analyzer without saving the file.

- Cancel — Cancels the exit operation.

Find (Edit Menu)

The Edit menu is visible and enabled only if a design, macro, or report window is open. The Find command displays the Find dialog box, shown in the next figure. It enables you to search for a text string within a Timing Analyzer report.

Figure 5-7 Find Dialog Box

The Find dialog box contains these fields.

- Find What is the field in which you type the text string to find.
- Match Case finds only instances that have the same case as the text string. By default, it ignores the case of the text.
- Direction indicates the direction to search.
  - Up searches backwards from the present location of the cursor to the beginning of the report. It stops at the beginning of the report.
  - Down searches forward from the present location of the cursor to the end of the report. It stops at the end of the report. This direction is the default.
- Find Next finds the next instance of the text string you are searching for.

Find Next (Edit Menu)

The Find Next command finds the next instance of the text string you are searching for with the same parameters as the previous search

with Timing Analyzer reports or macros. It is available for the Console window. The Edit menu is visible and enabled only if a design, macro, or report window is open.

Font (View Menu)

Use this command to specify the font type and font size for the text displayed in clocks, settings, and report windows. This command opens the font dialog box, as shown in the following figure.

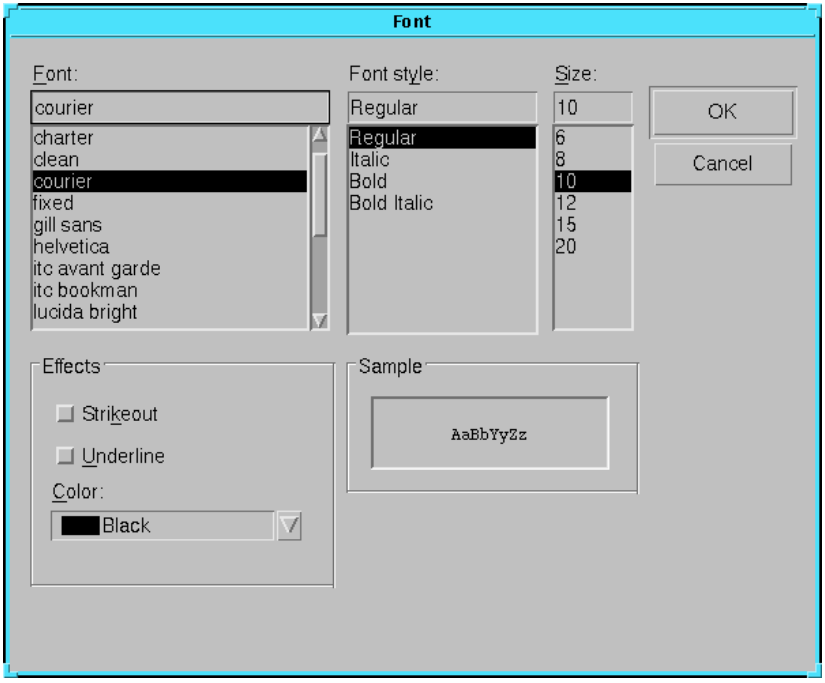


Figure 5-8 Font Dialog Box

You can select from a wide range of fonts in the Font dialog box, but be aware that variable width fonts may not be good for viewing timing reports.

Help Topics (Help Menu)

The Contents command lists the online help topics available for the Timing Analyzer. From the opening screen, you can jump to command information or step-by-step instructions for using the

Timing Analyzer. After you open help, you can click the Contents button (first button on the left) in the Timing Analyzer Help window when you want to return to the help topic list.

Pressing the F1 key is the same as selecting the Help Topics command, if no dialog boxes are displayed.

Include Paths with Nets (Path Filters Menu)

The Include Paths with Nets command limits analysis to paths that contain specified nets. If a net is not specified, paths through that net are not analyzed. However, if no nets are selected, which is the default, all nets, except those you exclude with other path filtering commands, are analyzed. This command appears in the Common Filters submenu.

Use this path filtering command in conjunction with any of the following reports.

- Timing Constraints Analysis report, which compares the implementation of the design to the constraints
- Advanced Design Analysis report, which indicates overall design performance
- Custom Analysis report, which contains detailed timing information for all paths in the design

This command displays the Include Paths with Nets dialog box, shown in the following figure.

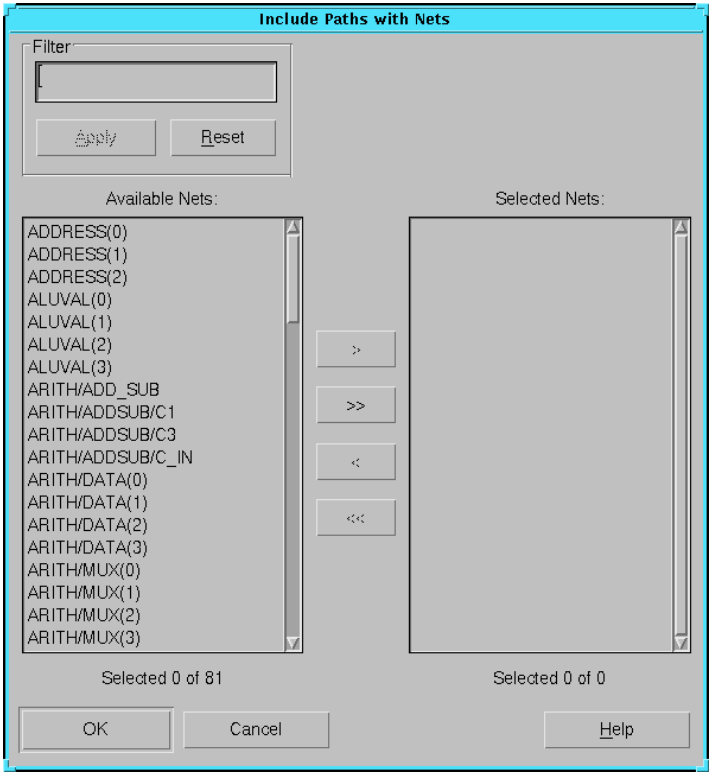


Figure 5-9 Include Paths with Nets Dialog Box

This dialog box includes these buttons and fields.

- Filter limits the nets displayed in the Available Nets list box to those you specify. You can include a “?” or an “*” wildcard in the net name for the filter to use in searches. The “?” represents a single character; the “*” represents zero or more characters.
    - Apply executes the filter in the Filter field, which hides all nets in the Available Nets list box that do not match the filter.
    - Reset deletes the filter and displays in the Available Nets list box, all nets except those that have been moved to the Selected Nets list box.
- Available Nets lists the nets to be excluded from timing analysis, except those that are hidden after applying a filter in the Filter field or those you move to the Selected Nets list box. If no nets are

moved to the Selected Nets list box, which is the default, all nets except those you include with other filters or commands are analyzed.

- Selected Nets lists the nets to be included in timing analysis.
- Add (>) moves selected nets from the Available Nets list box to the Selected Nets list box.
- Add All (>>) moves all the listed nets from the Available Nets list box to the Selected Nets list box.
- Remove (<) moves selected nets from the Selected Nets list box to the Available Nets list box.
- Remove All (<<) moves all listed nets from the Selected Nets list box to the Available Nets list box.

New Macro (File Menu)

The New Macro command opens a new Timing Analyzer macro document window, in which you can perform text editing to create a macro. You can also copy or cut a sequence of commands from the Console window and paste it in a New Macro window. The macro is saved to an XTM file, which is the only document type you create directly in the Timing Analyzer.

Online Documentation (Help Menu)

The Online Documentation command opens the software manuals on the Web. If you do not have Web access, you can still access the documentation, either from the copy you installed on your local hard drive or from the CD. The manuals are opened in the default Web browser. You can set your default browser using the Preferences command.

Open (File Menu)

The Open command opens existing timing report (TWR) or timing analysis macro (XTM) files. It displays the Open dialog box, shown in the next figure.

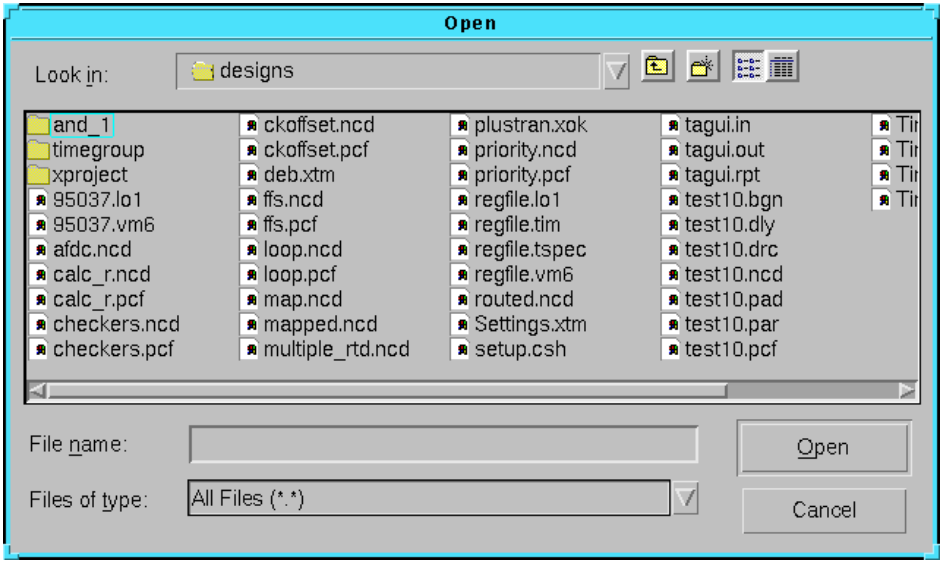


Figure 5-10 Open Dialog Box

This dialog box contains the following fields.

- File Name specifies the name of the macro, report, or other file to load. The default is a report (TWR) file. (Backspace over the asterisk.) You can also click on the file name in the list box just below this field.
- Directories (workstation) / Look in (PC) lists the directories (for the specified drive on PCs) so you can select the directory that contains the file that you want to load.
- List Files of Type (workstation) / Files of type (PC) lists the categories of files to open. It can be a macro (XTM), a report (TWR), or all files. Report (TWR) files is the default.

Open Design (File Menu)

The Open Design command opens a mapped NCD (FPGA) or a completed placed and routed VM6 (CPLD) file. The mapped FPGA design can be partially or completely placed, routed, or both. For FPGAs, a physical constraints file (PCF) is also need for timing analysis for specific constraints. By default, the Timing Analyzer opens the PCF file with the same name and in the same directory as the

design file. You can analyze the same design with different PCF files. The command displays the Open Design dialog box, shown in the following figure.

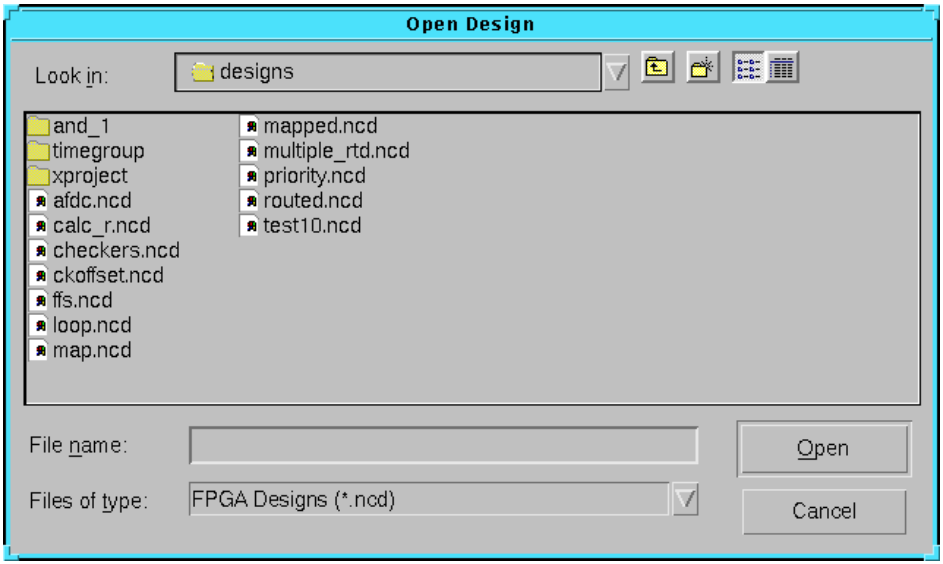


Figure 5-11 Open Design Dialog Box

This dialog box contains the following fields.

- File Name specifies the name of the NCD (FPGA) or VM6 (CPLD) design file to load. (Backspace over the asterisk.) You can also click on the design file name in the list box just below this field.
- Directories (workstation) / Look in (PC) lists the directories (for the specified drive on PCs) so you can select the directory that contains the design file you want to load.
- List Files of Type (workstation) / Files of type (PC) specifies whether the file to load is an NCD (FPGA) or VM6 (CPLD) design file. The default is an NCD file.

Open Physical Constraints (File Menu)

The Open Physical Constraints command displays the Open Physical Constraints dialog box that you use to load an existing physical constraints file (PCF) other than the default. The default PCF file has

the same name and exists in the same directory as the (NCD) design file.

Loading a new physical constraints file causes the Prorating Options to be reset to the values specified in the last PCF file you loaded. If the PCF file does not contain Prorating Options preferences, the worst case values are used.

Note: This command only supports FPGAs; CPLD physical constraint information exists in the (VM6) design file itself. The order of the constraints in the PCF file is reflected by the Timing Analyzer.

The Open Physical Constraints command displays the dialog box shown in the next figure.

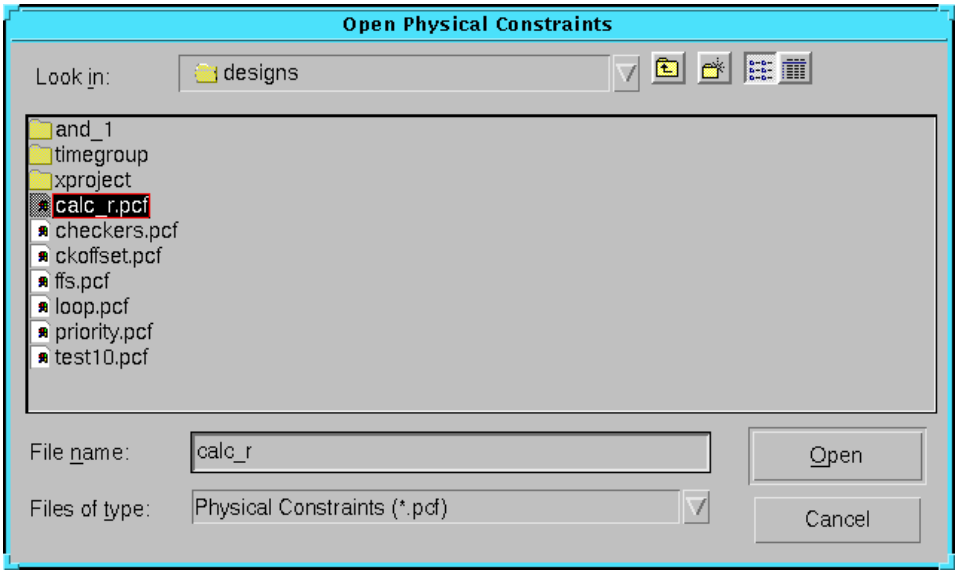


Figure 5-12 Open Physical Constraints Dialog Box

The dialog box contains the following fields.

- File Name specifies the physical constraints file (PCF) to load. (Backspace over the asterisk.) You can also click on the PCF file name in the list box just below this field.
- Directories (workstation)/Look in (PC) lists the directories (for the specified drive on PCs) so you can select the directory that contains the physical constraints file that you want to load.

- List Files of Type (workstation) / Files of type (PC) lists physical constraints files (PCF).

Paste (Edit Menu)

The Paste command functions like the standard Paste command; it pastes text last copied to the clipboard. The Edit menu is visible and enabled only if a design, macro, or report window is open.

Print (File Menu)

The Print command displays the Print dialog box, which sends the file that is displayed in the active window to the default printer. It also enables you to indicate how many copies to print, to send the file to a printer other than the default, or to change printer options. The Print dialog box is shown in the following figure.

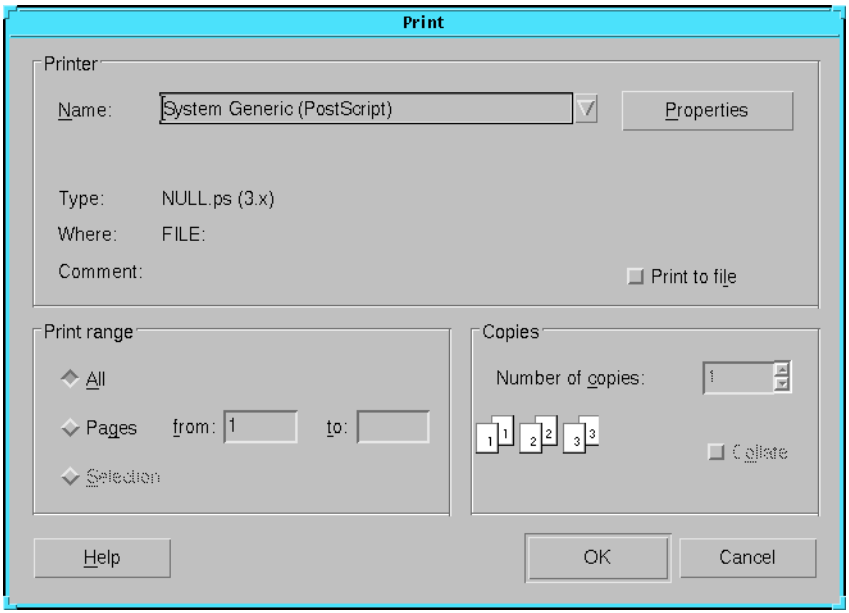


Figure 5-13 Print Dialog Box

Print dialog boxes vary between workstations and PCs. Four basic options in this dialog box follow.

- Print Range

- All prints the entire file
- Pages From is the field in which you enter the beginning of the range of pages to print.
- Pages To is the field where you enter the end of the range of pages to print.

- Copies is the field in which you enter the number of copies you want to print.
- Print to File is the box to select to print to a file.

Prorating Options (Options Menu)

The Prorating Options command controls voltage and temperature prorating. The command is only enabled when temperature or voltage prorating data is available for the current device and speed grade. The Prorating Options dialog box is shown in the following figure.

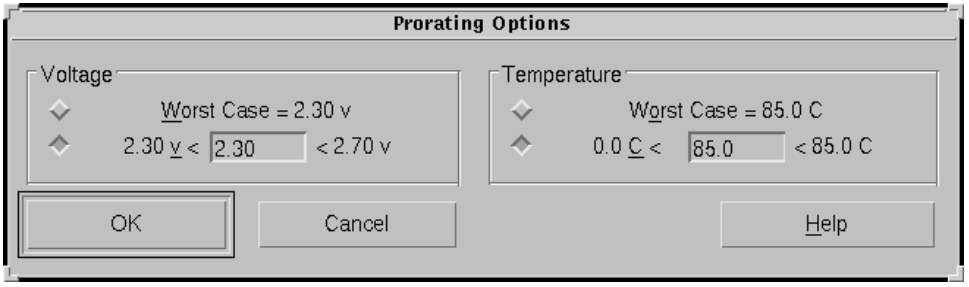


Figure 5-14 Prorating Options Dialog Box

The Prorating Options dialog box contains the following fields.

- Voltage sets the voltage prorating. Choose between the Worst Case value or setting a range of values.
- Temperature sets the temperature prorating. Choose between the Worst Case value or setting a range of values. The temperature is given in degrees Celsius.

Query (Analyze Menu)

The Query command generates a report containing timing information of particular nets or members of a time group. It displays the Query dialog box, shown in next figure.

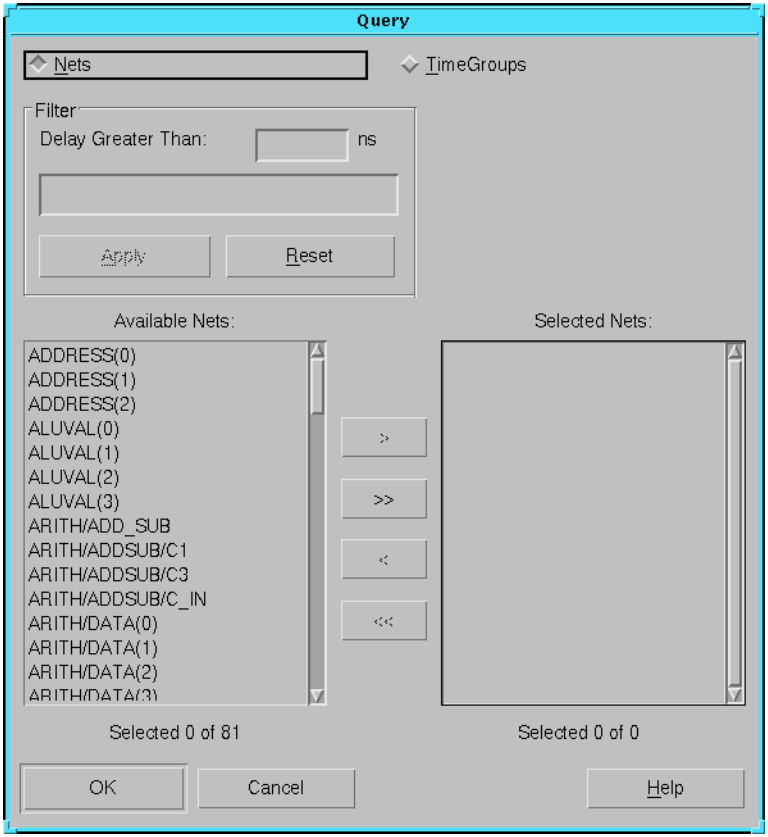


Figure 5-15 Query Dialog Box

Note: This command only supports FPGAs. It is disabled if a CPLD design is open.

The Query dialog box contains the following buttons and fields.

- Nets displays timing information of particular nets. When you select this button, the Query Nets Report shows the fanout, the timing from the source CLB to each of the destination CLBs, and the CLB names.

- TimeGroups displays members of time groups. The Query Time Groups report lists the elements in the specified timing groups.
- Filter limits the elements displayed in the Available *Nets* / *Timegroups* list box to those you specify. The filter display alternates between *Nets* and *TimeGroups* with the button you select.
    - Field in which to specify a filter to display a subset of nets or time groups. You can include a "?" or an "*" wildcard. The "?" represents a single character; the "*" represents zero or more characters.
    - Delay Greater Than specifies a minimum delay in nanoseconds. The Timing Analyzer displays only those paths that have a delay greater than or equal to the specified value. You can enter a value in this field only when you select Nets. If you enter a value in both the Delay Greater Than and the filter field, the Timing Analyzer lists the nets that meet both criteria.
    - Apply executes the filter in the Filter field and displays the subset in the Available *Nets* / *TimeGroups* list box.
    - Reset deletes the filter and redisplays all the nets or time groups in the Available *Nets* / *TimeGroups* list box.
- Available *Nets* / *TimeGroups* displays all the available net or timing group elements on which you can obtain information.
- Selected *Nets* / *TimeGroups* displays only the net or timing group elements that you selected.
- Add (>) moves selected elements from the Available *Nets* / *TimeGroups* list box to the Selected *Nets* / *TimeGroups* list box.
- Add All (>>) moves all the listed elements from the Available *Nets* / *TimeGroups* list box to the Selected *Nets* / *TimeGroups* list box.
- Remove (<) moves selected elements from the Selected *Nets* / *TimeGroups* list box to the Available *Nets* / *TimeGroups* list box.
- Remove All (<<) moves all the listed elements from the Selected *Nets* / *TimeGroups* list box to the Available *Nets* / *TimeGroups* list box.

Recent Design (File Menu)

The Recent Design command lists up to the last four design files (NCD for FPGA or VM6 for CPLD) that you opened. The design you select (and for FPGAs, its default physical constraints file) are automatically loaded as the current design.

Recent File (File Menu)

The Recent File command lists up to the last four files that you opened. The file you select is automatically opened.

Recent Macro (File Menu)

The Recent Macro command lists up to the last four macro files that you opened. The macro you select is automatically loaded and run.

Recent Physical Constraints (File Menu)

The Recent Physical Constraints command lists up to the last four physical constraints files that you opened. The file you select is automatically loaded as the current physical constraints file.

Recent Report (File Menu)

The Recent Report command lists up to the last four reports that you opened. The report you select is automatically opened.

Recent Window (Window Menu)

The Recent Window command lists the active windows, whether they are open or iconized. Select a window from the Recent Window list to expand it if it is iconized and bring it to the front view.

Report Options (Options Menu)

The Report Options command determines the appearance of a report and the information that it contains. It displays the Report Options dialog box, shown in the following figure, so you can customize the Timing Analyzer reports.

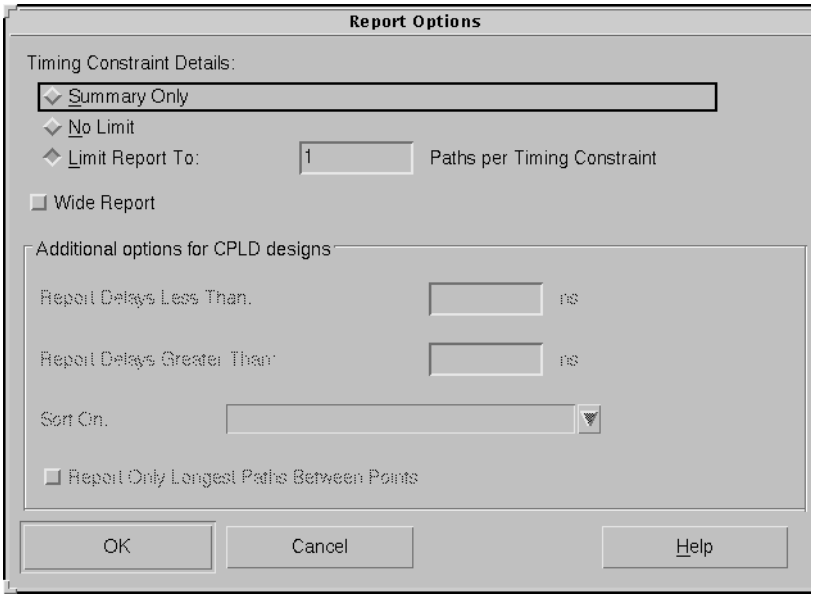


Figure 5-16 Report Options Dialog Box

The following table lists each option in the dialog box and indicates if the option supports FPGA or CPLD designs.

Option	FPGA	CPLD
Summary Only	Yes	No
No Limit	Yes	Yes
Limit Report To	Yes	Yes
Report Delays Less Than	No	Yes
Report Delays Greater Than	No	Yes
Sort On	No	Yes
Report Only Longest Paths Between Points	No	Yes
Wide Report	Yes	Yes

- Summary Only generates a report containing only the path source and end point. This report lists one delay path per line and does not display cumulative delays through CLBs. Applies only to FPGAs.

- No Limit generates a report containing an unlimited number of paths reported per timing constraint.
- Limit Report To sets the limit for the number of paths reported per timing constraint. This option can be useful, because it limits the size of report files.
- Report Delays Less Than (CPLD only) reports only those paths that have a delay less than or equal to the specified value. Not specifying a value is equivalent to "no limit" and the option is turned Off.
- Report Delays Greater Than (CPLD only) reports only those paths that have a delay greater than or equal to the specified value. The default is zero, which reports all paths, regardless of their delay.
- Sort On (CPLD only) specifies how paths are sorted when they are reported. The pull-down list box has the following six options.
    - Ascending Delay lists paths in order from shortest to longest delays.
    - Descending Delay lists paths in order from longest to shortest delays.
    - Source Net sorts path delays by the source net name, which is useful when trying to determine the worst-case delay from a given component.
    - Destination Net sorts path delays by the destination net name, which can help determine the worst-case path to each component.
    - Source Clock Net sorts path delays by the clock name that sources the first element in a path, which separates delay information for two or more clock nets in a design.
    - Destination Clock Net sorts path delays by the clock name that sources the last element in a path.
- Report Only Longest Paths Between Points (CPLD only) reports only the path with the longest delay if there is more than one path between two end points.
- Wide Report creates a report formatted with 132 characters per line instead of 80 characters per line as in a default report. This

helps prevent truncating long component and net names since they are truncated to 132 characters instead of 80 characters.

Report Paths in Timing Constraints (Analyze Menu)

The Report Paths in Timing Constraints command generates a Timing Constraints Analysis report for all paths covered by timing constraints. However, the number of paths reported is affected by the Limit Report To setting in the Report Options dialog box which you access with the **Options** → **Report Options** command.

When you invoke most Timing Analyzer menu commands, a corresponding macro command is issued and appears in the Console window. However, when you invoke the Report Paths in Timing Constraints command, the following three macro commands are issued:

```
SelectFailingTimingConstraint False
IncludeNoTimingConstraint False
AnalyzeTimingConstraints
```

Report Paths Failing Timing Constraints (Analyze Menu)

The Report Paths Failing Timing Constraints command generates a Timing Constraints Analysis report for only the paths that do not meet the timing constraints. However, the number of paths reported is affected by the Limit Report To setting in the Report Options dialog box which you access with the **Options** → **Report Options** command.

When you invoke most Timing Analyzer menu commands, a corresponding macro command is issued and appears in the Console window. However, when you invoke the Report Paths Failing Timing Constraints command, the following three macro commands are issued:

```
SelectFailingTimingConstraint True
IncludeNoTimingConstraint False
AnalyzeTimingConstraints
```

Report Paths Not Covered by Timing Constraints (Analyze Menu)

The Report Paths Not Covered by Timing Constraints command generates a Timing Constraints Analysis report for paths covered by timing constraints and for paths not covered by timing constraints. However, the number of paths reported is affected by the Limit Report To setting in the Report Options dialog box which you access with the **Options** → **Report Options** command.

When you invoke most Timing Analyzer menu commands, a corresponding macro command is issued and appears in the Console window. However, when you invoke the Report Paths Not Covered by Timing Constraints command, the following three macro commands are issued:

```
SelectFailingTimingConstraint False
IncludeNoTimingConstraint True
AnalyzeTimingConstraints
```

Reset All Path Filters (Path Filters Menu)

The Reset All Path Filters command resets path filters to default settings. To display path filter settings, see the Settings (View Menu) command.

Run Macro (File Menu)

The Run Macro command displays the Run Macro dialog box, which allows you to select a specific macro file to be executed. A macro is a script file that contains Timing Analyzer commands, filters, report options, or all three. The Run Macro dialog box is shown in the following figure.

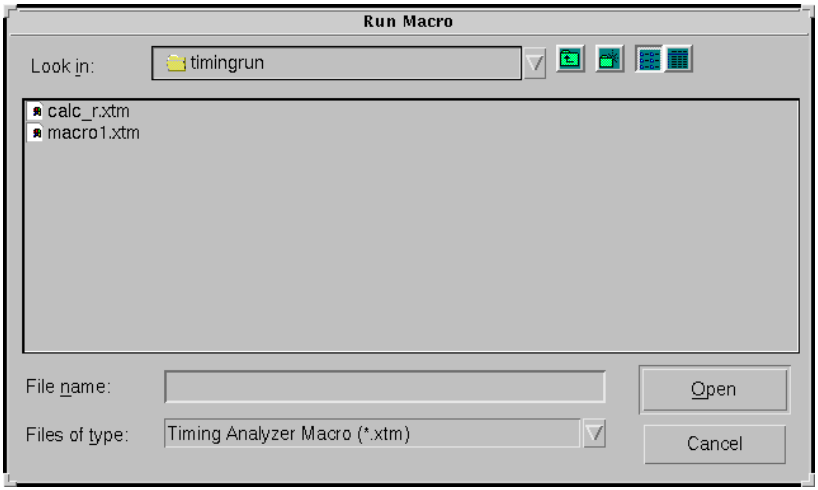


Figure 5-17 Run Macro Dialog Box

This dialog box contains the following fields.

- Look in lists the directories. Select the directory that contains the macro you want to run.
- File Name specifies the name of the macro you want to run. You can either type in the name of the macro or click on the file name in the list box just above this field.
- Files of type lists the categories of files to open. Timing Analyzer Macro (*.xtm) is the default.

The File menu MRU list shows macros that have been opened for editing or run. The toolbar button just runs the macro in the active window.

Save (File Menu)

The Save command saves reports in the active window to a specified file. It also saves macros created with the New Macro command. By default, the Timing Analyzer saves reports as TWR files and macros as XTM files. This command displays the Save As dialog box which you can use to save reports and macros as different files. It is shown in “Save As Dialog Box” figure. If you saved the report or macro once, the Save command saves the document in the existing file without activating the Save As dialog box.

Save As (File Menu)

The Save As command saves the edited report or macro to another file. It displays the Save As dialog box, which is the same dialog box activated by the Save command. This dialog box is displayed in the following figure.

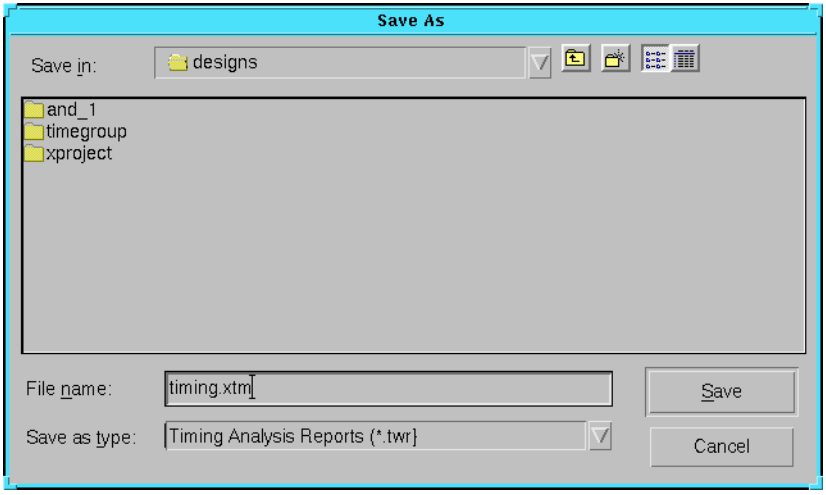


Figure 5-18 Save As Dialog Box

The Save As dialog box contains the following fields.

- File Name specifies the name of the file in which to save the report or macro. (Backspace over the asterisk.) You can also click on the file name in the list box just below this field.
- Save In lists the directories so you can select the directory in which to save the report or macro file.
- Save As Type lists categories of file types from which you select to display in the File Name field and list box. You do not have to save the file as a TWR or an XTM file, but the Timing Analyzer saves reports as TWR or macros as XTM files by default. Additionally, the Timing Analyzer only reads XTM files, that is, files with an .xtm extension.

Select Destinations (Path Filters Menu)

The Select Destinations command defines the ending points of paths you want to analyze. This command appears in the Custom Filters submenu.

Use this path filtering command in conjunction with the Advanced Design Analysis report, which indicates overall design performance. Or with the Custom Analysis report, which contains detailed timing information for all paths in the design.

This command displays the Select Destinations dialog box, shown in the following figure.

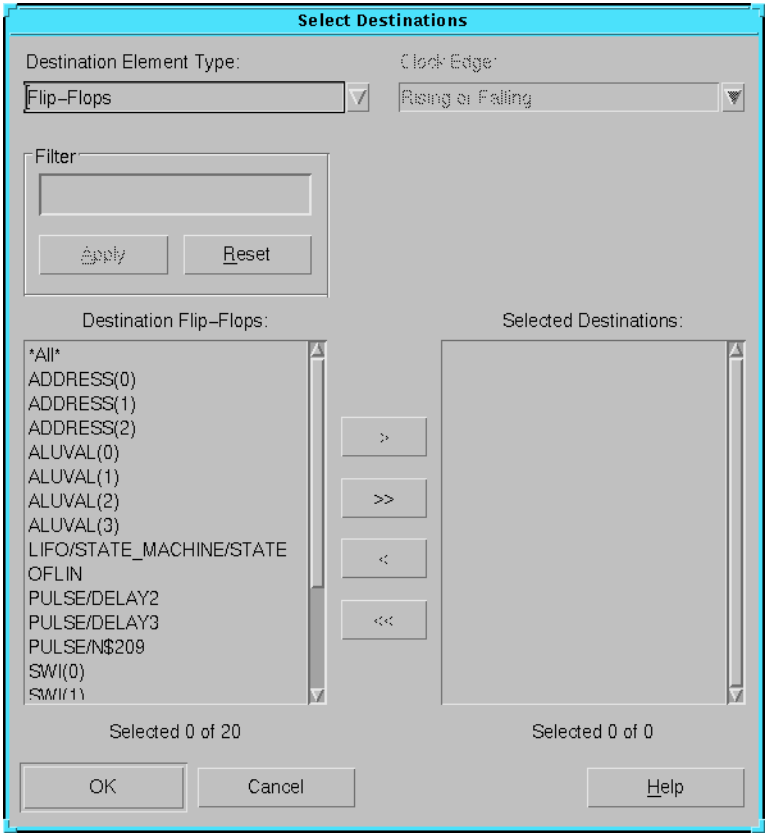


Figure 5-19 Select Destinations Dialog Box

This dialog box contains the following buttons and fields.

- Destination Element Type is a pull-down list box that lists the destination elements. The default is flip-flops.

  FPGA destination types are: flip-flops, pads, nets, pins, CLBs, RAMs, latches, clocks, or timegroups. CPLD destination types are: flip-flops, pads, nets, macrocells, or clocks.

  If an element type is not used in the design, the type will not appear in the pull-down list.

- Clock Edge determines whether the destination is a clock's rising or falling edge, or either edge. This option is available only for FPGAs when you select Clocks in the Destination Element Type field.

- Filter limits the destination to a particular element or elements within the specified category and displayed in the Destination *Element* list box. The *Element* changes with the element you select in the Destination Element Type. You can include a "?" or an "*" wildcard in the element type for the filter to use in searches. The "?" represents a single character; the "*" represents zero or more characters.

  - Apply executes the filter in the Filter field and displays the subset in the Destination *Element* list box.

  - Reset deletes the filter and redisplays all the element destinations in the Destination *Element* list box.

- Destination *Element* lists all the individual destinations that you specify in the Destination *Element* Type. You can display a subset of this list by applying a filter in the Filter field.

- Selected Destinations displays the individual destinations that you selected.

- Add (>) moves selected elements from the Destination *Element* list box to the Selected Destinations list box.

- Add All (>>) moves all the listed elements from the Destination *Element* list box to the Selected Destinations list box.

- Remove (<) removes selected elements from the Selected Destinations list box.

- Remove All (<<) removes all listed elements from the Selected Destinations list box.

Select Sources (Path Filters Menu)

The Select Sources command defines the starting points of paths you want to analyze. This command appears in the Custom Filters submenu.

Use this path filtering command in conjunction with the Custom Analysis report, which contains detailed timing information for all paths in the design.

This command displays the Select Sources dialog box, shown in the following figure.

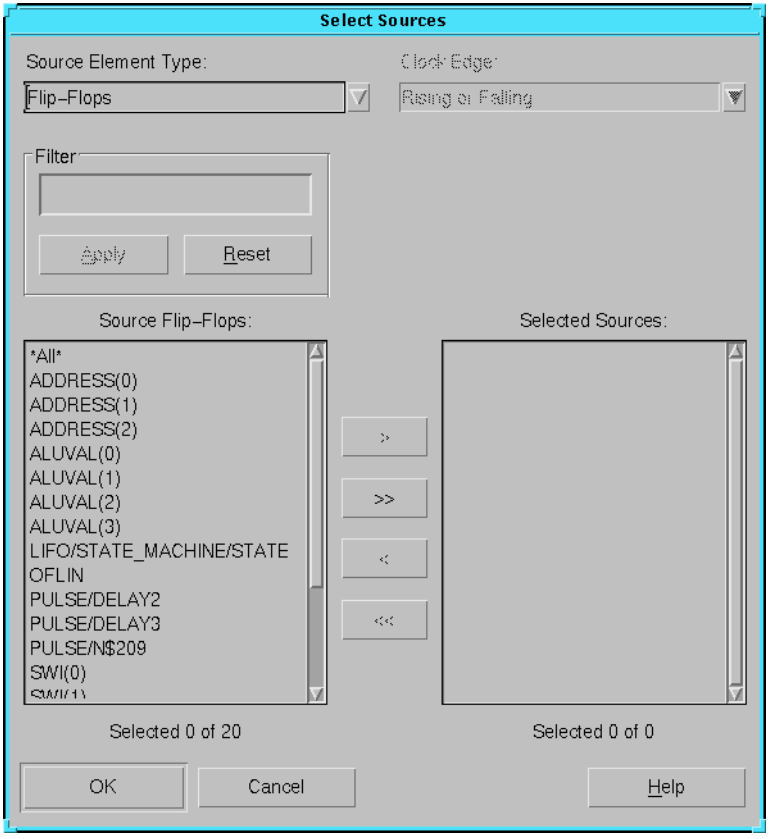


Figure 5-20 Select Sources Dialog Box

This dialog box displays the following buttons and fields.

- Source Element Type is a pull-down list box that lists the source elements. The default is flip-flops.

  FPGA source types are: flip-flops, pads, nets, pins, CLBs, RAMs, latches, clocks, or timegroups. CPLD source types are: flip-flops, pads, nets, macrocells, or clocks.

  If an element type is not used in the design, the type will not appear in the pull-down list.

- Clock Edge determines whether the source is a clock's rising edge or falling edge, or either edge. This option is available only for FPGAs when you select Clocks in the Source Element Type.

- Filter limits the elements displayed in the Source *Element* list box to those you specify. The *Element* changes with the element you select in the Source Element Type. You can include a "?" or an "*" wildcard in the source name for the filter to use in searches. The "?" represents a single character; the "*" represents zero or more characters.

  - Apply executes the filter in the Filter and displays the subset in the Source *Element* list box.

  - Reset deletes the filter and redisplays all the sources of the specified type in the Source *Element* list box.

- Source *Element* list box lists all the individual sources that you specify in the Source Element Type field. You can display a subset by applying a filter in the Filter field.

- Selected Sources displays all the individual sources that you selected for the specified source type.

- Add (>) moves selected elements from the Source *Element* list box to the Selected Sources list box.

- Add All (>>) moves all the listed elements from the Source *Element* list box to the Selected Sources list box.

- Remove (<) moves selected elements from the Selected Sources list box to the Source *Element* list box.

- Remove All (<<) moves all listed elements from the Selected Sources list box to the Source *Element* list box.

Settings (View Menu)

The Settings command lists the current settings of Timing Analyzer options specified with the commands in the Path Filters and Options menus in a pop-up window. The “Settings Window” figure of the “Using the Timing Analyzer” chapter gives an example of the window and the information it displays when you select this command.

You can save the settings as a macro (.xtm) file to return the system to the same state as when the settings were saved. See the “Saving a New Macro” section and the “Running a Macro” section of the “Using the Timing Analyzer” chapter for more information. You can also save the contents of the window to a .twr file. TWR files are listed as Timing Analysis Reports (*.twr) under List Files of Type in File menu command dialog boxes. See the “Saving a Report” section of the “Using the Timing Analyzer” chapter for the procedure to save a report.

The settings apply to both FPGAs and CPLDs unless specified. The default settings are as follows.

Table 5-2 Default Settings of Timing Analyzer Options

Setting	Description
OpenPCF *file_name*	Displays the current physical constraints file (PCF).
Speed *speed_grade*	Sets the speed grade for analysis. See Speed Grade (Options Menu).
IncludeNets	If no arguments specified, includes all nets during analysis. See Include Paths with Nets (Path Filters Menu).
ExcludeNets	If no arguments specified, includes all nets during analysis, no nets are excluded. Default is no nets are excluded. See Exclude Paths with Nets (Path Filters Menu).
SelectFailingTimeConstraint *True* / *False*	If set to *True*, reports only paths that do not meet timing constraints. The default is *False*. See “SelectFailingTimingConstraint” section of the “Command Line Syntax” chapter.

Table 5-2 Default Settings of Timing Analyzer Options

Setting	Description
IncludeNoTimeConstraint *True* / *False*	If set to *True*, reports paths without timing constraints, in addition to paths with timing constraint. Default is *False* for FPGAs, *True* for CPLDs. See "IncludeNoTimingConstraint" section of the "Command Line Syntax" chapter.
Report *Normal* | *Wide*	The default is *Normal.* A *Normal* report is 80 characters per line. A *Wide* report is 132 characters per line.
MaxPathsPerTimingConstraint *number*	Displays maximum number of paths per timing constraint. Set in the Report Options (Options Menu) dialog box.
DelayLessThan *delay_value*	Optional command that only supports analysis of CPLD designs. If not specified, there is "no upper limit." Change the *delay_value* in the Report Options (Options Menu) dialog box.
DelayGreaterThan *0.000*	Only supports analysis of CPLD designs. Default is *0*, which includes all paths. Change this *number* in the Report Options (Options Menu) dialog box.
OnlyLongestPaths *False*	Only supports analysis of CPLD designs. If set to *True*, reports only the path with the longest delay, if there is more than one path between two end points. Change this setting in the Report Options (Options Menu) dialog box.
SortOn *Ascend*	Only supports analysis of CPLD designs. Specifies how paths are sorted when reported. Corresponds with the Sort On pull-down list box in the Report Options (Options Menu) dialog box.
DefineEndpoints *ToAll*	Corresponds with the Select Destinations (Path Filters Menu) command.
DefineEndpoints *FromAll*	Corresponds with the Select Sources (Path Filters Menu) command.

Table 5-2 Default Settings of Timing Analyzer Options

Setting	Description
OmitUserConstraints *False*	Only supports analysis of FPGA designs. If set to *True*, disables timing constraints in "USER" section of the PCF. If set to *False*, enables timing constraints in "USER" section.
DropTimingConstraint	Corresponds with the Disable Timing Constraints (Path Filters Menu) command.

Speed Grade (Options Menu)

The Speed Grade command changes the speed grade for timing analysis only. The speed grade you set in the NCD or VM6 design file is not affected. This command displays the Speed Grade dialog box, shown in the following figure.

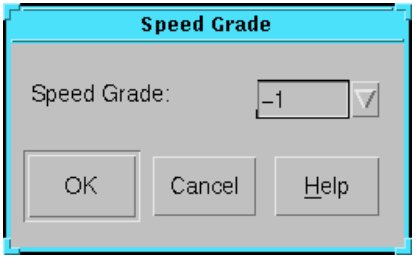


Figure 5-21 Speed Grade Dialog Box

In the dialog box, Speed Grade is a pull-down list box that lists the available speed grades for the target device. For families that support minimum speed grades, a Min selection is available in the Speed Grade menu.

Changing the speed grade may affect the worst case and range of values available in the Prorating Options dialog box.

Status Bar (View Menu)

The Status Bar command controls whether or not the status bar is displayed. It is displayed by default. The status bar displays a brief description of the current menu item under the cursor, which command is being executed, the open PCF file name, and Timing Analyzer messages.

Tile (Window Menu)

The Tile command arranges the open windows in rows across the Timing Analyzer screen. The windows are fitted into all available screen space without overlapping, as the next figure illustrates.

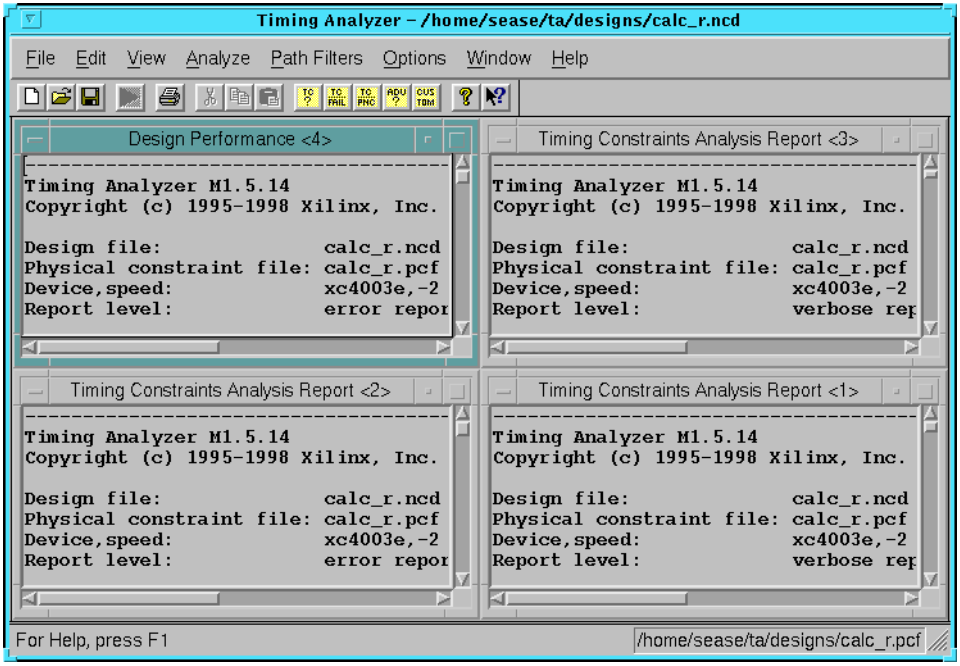


Figure 5-22 Tiled Windows

Timing Constraints Submenu (Analyze Menu)

Timing Constraints is a submenu in the Analyze menu which contains the following commands that allow you to specify how the Timing Analyzer generates the Timing Constraints Analysis report:

- Report Paths in Timing Constraints (Analyze Menu)
- Report Paths Failing Timing Constraints (Analyze Menu)
- Report Paths Not Covered by Timing Constraints (Analyze Menu)

In addition to the above commands, you can use the following path filter commands to modify the scope of the Timing Constraints Analysis report.

- Disable Timing Constraints (Path Filters Menu)
- Include Paths with Nets (Path Filters Menu)
- Exclude Paths with Nets (Path Filters Menu)
- Control Path Tracing (Path Filters Menu)

Timing Constraint Filters Submenu (Path Filters Menu)

The Timing Constraint Filters submenu contains the Disable Timing Constraints (Path Filters Menu) command, which allows you to specify paths to exclude from the Timing Constraints Analysis report.

Toolbar (View Menu)

The Toolbar command controls whether or not the toolbar is displayed. It is displayed by default. See the “Toolbar” section, following, for a description of the buttons on the toolbar.

Figure 5-23 Timing Analyzer Toolbar

Toolbar

The toolbar provides button access to frequently used menu commands. Textual labels for the buttons appear when you move the cursor over a button. This feature is called a tool tip. Every toolbar button has a tool tip; a longer description appears in the status bar. The Cut, Copy, Paste, and Run Macro buttons appear only when you click on the New Macro command. The Timing Analyzer window displays the following buttons, which are discussed in the order that they appear on the toolbar.

New Macro

New Macro opens a new Timing Analyzer macro document window. It is equivalent to the New Macro (File Menu) command.

Open Design

Open Design button opens an existing design for timing analysis. It is equivalent to the Open Design (File Menu) command.

Save

The Save button saves the active macro or report window to a specified file. It is equivalent to the Save (File Menu) command.

Print

The Print button displays the Print dialog box and sends the contents displayed in the active window to the default printer. It is equivalent to the Print (File Menu) command.

Run Macro

The Run Macro button runs an existing macro, which you open with the Open command on the File menu. It is enabled when a macro file is active.

Cut

The Cut button cuts the selected text from a macro window and moves the text to the clipboard. It is enabled when a macro window is open and text is selected. (The Console and report windows are read-only.) The Cut button is equivalent to the Cut (Edit Menu) command.

Copy

The Copy button, copies the highlighted commands in the Console window or selected text in a macro or report window to the clipboard, so that you can paste them into a macro window to form a new macro or edit an existing one. It is enabled when the Console window is open and commands are highlighted or a macro or report window is open and text is selected. The Copy button performs the same function as the Copy (Edit Menu) command.

Paste

The Paste button replaces the currently selected text in the macro window with the contents of the clipboard. If no text is selected, the

contents of the clipboard are inserted at the cursor position in the macro window. The Paste button functions the same as the Paste (Edit Menu) command.

Report Paths in Timing Constraints

The Report Paths in Timing Constraints button generates a Timing Constraints Analysis report for all paths covered by timing constraints. This button is equivalent to the Report Paths in Timing Constraints (Analyze Menu) command.

Report Paths Failing Timing Constraints

The Report Paths Failing Timing Constraints command generates a Timing Constraints Analysis report for only the paths that do not meet the timing constraints. This button is equivalent to the Report Paths Failing Timing Constraints (Analyze Menu) command.

Report Paths Not Covered by Timing Constraints

The Report Paths Not Covered by Timing Constraints command generates a Timing Constraints Analysis report for paths covered by timing constraints and for paths not covered by timing constraints. This button is equivalent to the Report Paths Not Covered by Timing Constraints (Analyze Menu) command.

Advanced Design

The Advanced Design button generates the Advanced Design Analysis report. The report indicates overall design performance. It is equivalent to the Advanced Design (Analyze Menu) command.

Custom

The Custom button generates the Custom Analysis report, which contains worst-case path delays for all paths in the design. It is equivalent to the Custom (Analyze Menu) command.

About

The About button displays program and copyright information about the Timing Analyzer. It is equivalent to the About Timing Analyzer (Help Menu) command.

Help

Help displays information about a menu command or option when you click on it. The information is displayed in a pop-up window. See the “Obtaining Help” section of the “Getting Started” chapter.

Chapter 6

Command Line Syntax

This chapter describes the commands you can enter in the Timing Analyzer's Console or New Macro window.

The syntax of these commands is case-insensitive; capitalization is used for easy reading. Parameters in the "Abbreviation" sections have the same respective meanings as the parameters in the longer form of the syntax.

If # (pound sign) is the first non-white space character on a line, that line is treated as a comment (ignored). If \ (backslash) is the last character on a line, the next line of text is treated as a continuation of the line before it. You can use the backslash in this way to make a single command span more than one line.

For more information on issuing commands through the Console window, see the "Using the Console Window" section of the "Using the Timing Analyzer" chapter. For instructions on using these commands to build macros, see the "Using Macros" section of the same chapter.

The commands are listed in alphabetical order in the following sections.

- “DelayLessThan”
- “DoHoldRaceCheck”
- “DropTimingConstraint”
- “ExcludeNets”
- “Exit”
- “IncludeNets”
- “IncludeNoTimingConstraint”
- “MaxPathsPerTimingConstraint”
- “OmitUserConstraints”
- “OnlyLongestPaths”
- “OpenDesign”
- “OpenPCF”
- “ProratingOptions”
- “Query”
- “Report”
- “ResetAllPathFilters”
- “RunMacro”
- “SelectFailingTimingConstraint”
- “SetForce”
- “ShowClockNets”
- “ShowSettings”
- “SortOn”
- “Speed”

Command Summary

Table 6-1 Command Line Summary

Command	Syntax	Description
AnalyzeAdvancedDesign	aad [save *file_name*.twr]	Generates report indicating overall design performance
AnalyzeCustom	ac [save *file_name*.twr]	Generates report containing worst-case path delays for paths in design, except those suppressed by filtering commands
AnalyzeTimingConstraints	atc [save *file_name*.twr]	Generates report indicating whether design meets timing constraints
ControlPathTracing	cpt {Enable | Disable} {reg_sr_q | lat_d_q | ram_d_o | ram_we_o | tbuf_t_o | tbuf_i_o | io_pad_i | io_t_pad | io_o_i | io_o_pad | io_t_i} *component_name...*	Controls path tracing through components
DefineEndPoints	dep {fall | tall} dep {fpad | tpad} *pad_name* dep {fclb | tclb} *CLB_name* dep {fnet | tnet} *net_name* dep {fpin | tpin} *pin_name* dep {fff | tff} *flip-flop_name* dep {fee | tee} *clock_name* dep {fris | tris} *clock_name* dep {fmc | tmc} *macrocell_name* dep {ffal | tfal} *clock_name* dep {fram | tram} *RAM_name* dep {fl | tl} *latch_name* dep {ftg | ttg} *timegroup_name*	Defines path starting and ending points
DelayGreaterThan	dg *delay_value*	Specifies minimum delay. Only supports analysis of CPLD designs

Table 6-1 Command Line Summary

Command	Syntax	Description
DelayLessThan	dl *delay_value*	Specifies maximum delay. Optional CPLD-only command
DoHoldRaceCheck	dhrc {true | false}	Do hold / race checking when analyzing the design
DropTimingConstraint	dtc [*time_constraint1 time_constraint2* ...]	Omits specified timing constraints from analysis
ExcludeNets	exnet [*net_name1 net_name2* ...]	Prohibits analysis of specified nets
Exit	exit	Exits the Timing Analyzer
IncludeNets	incnet [*net_name1 net_name2* ...]	Limits analysis to paths containing specified nets
IncludeNoTimingConstraint	intc {true | false}	Forces reporting of paths with no timing constraints
MaxPathsPerTimingConstraint	mpptc *number_of_paths*	Limits the total number of paths reported per timing constraint
OmitUserConstraints	ouc {true | false}	Enables or disables user-specified constraints in the PCF file
OnlyLongestPaths	olp {true | false}	Reports only path with longest delay for each constraint. Only supports analysis of CPLD designs
OpenDesign	od {*design_name*.ncd | *design_name*.vm6}	Loads a design for timing analysis
OpenPCF	op *file_name*.pcf	Opens an existing physical constraints file
ProratingOptions	po {T {*degrees_celsius*}} {V {*voltage*}}	Controls temperature and voltage prorating
Query	qy {Net | TimeGroup} *element_name*	Displays timing information about groups of elements

Table 6-1 Command Line Summary

Command	Syntax	Description
Report	r {wide | normal}	Determines format of reports
ResetAllPathFilters	rapf	Causes path filters to revert to default
RunMacro	runm *file_name*.xtm	Runs macro
SelectFailingTiming-Constraint	sftc {true | false}	Limits reporting to paths that do not meet timing constraints
SetForce	sf {on | off}	Suppresses messages when macro is run
ShowClockNets	scn [save *file_name*]	Show or hide the window showing the clock nets
ShowSettings	ss [save *file_name*]	Show or hide the window displaying current settings of filters and command option settings
SortOn	sort {Ascend | Descend | SourceNet | DestNet | Source-ClkNet | DestClkNet}	Specifies how paths are sorted when they are reported. Only supports analysis of CPLD designs
Speed	sp *speed_grade*	Changes speed grade during analysis

AnalyzeAdvancedDesign

The AnalyzeAdvancedDesign command generates an Advanced Design Analysis report. This report provides a set of summary statistics for the paths from the timing requirements specified for analysis.

For FPGAs, this report displays the results of analyzing the constraints specified in the constraints file. If no constraints are specified, this report displays the maximum clock frequencies for all clocks in the design and the worst-case timing for all clock paths. For CPLDs, the Design Performance report lists all external Pad to Pad

(tPD), Clock Pad to Output Pad (tCO), Setup to Clock at the Pad (tSU) and delays, and internal Clock to Setup (tCYC) delays.

This command is equivalent to the **Analyze** → **Advanced Design** menu command.

Note: The AnalyzeAdvancedDesign command was previously named AnalyzeDesignPerformance and had the abbreviation adp. You can still use AnalyzeDesignPerformance and adp for this release of the software, but they will be phased out in a subsequent release.

Syntax

The syntax of the AnalyzeDesignPerformance command is the following.

AnalyzeAdvancedDesign [save *file_name*.**twr]**

- **Save** indicates that you can optionally save the Advanced Design Analysis report in a file. If this option is not specified, the report appears in a window.
- *File_name* is the name of the file in which the Design Performance report is saved. TWR is the extension for report files.

Abbreviation

Abbreviate the AnalyzeAdvancedDesign command syntax as follows.

aap [s *file_name.***twr]**

Example

The following is an example of the AnalyzeAdvancedDesign command.

```
analyzeadvanceddesign save shelby.twr
```

AnalyzeCustom

The AnalyzeCustom command creates the Custom Analysis report, a long report that displays a detailed analysis of all specified paths.

This command is equivalent to the **Analyze** → **Custom** menu command.

Note: The AnalyzeCustom command was previously named AnalyzeAllPaths and had the abbreviation aap. You can still use AnalyzeAllPaths and aap for this release of the software, but they will be phased out in a subsequent release.

Syntax

The syntax of the AnalyzeCustom command is the following.

`AnalyzeCustom [save` *file_name.***`twr]`**

- **`Save`** indicates that you can optionally save the Custom Analysis report in a file. If this option is not specified, the report appears in a window.
- *File_name* is the name of the file in which the Custom Analysis report is saved. TWR is the extension for report files.

Abbreviation

Abbreviate the AnalyzeCustom command syntax as follows.

`ac [s` *file_name.***`twr]`**

Example

Following is an example of the AnalyzeCustom command.

```
analyzecustom save xredesign.twr
```

AnalyzeTimingConstraints

The AnalyzeTimingConstraints command generates the Timing Analysis report, which compares design performance to the timing constraints.

There is no single menu command equivalent for AnalyzeTiming-Constraints. The following three menu commands are associated with AnalyzeTimingConstraints:

- Report Paths in Timing Constraints (Analyze Menu)
- Report Paths Failing Timing Constraints (Analyze Menu)
- Report Paths Not Covered by Timing Constraints (Analyze Menu)

Syntax

The following is the syntax for the AnalyzeTimingConstraints command.

`AnalyzeTimingConstraints [save` *file_name*.**`twr]`**

- **`Save`** indicates that you can optionally save the Timing Analysis report in a file. If this option is not specified, the report appears in a window.
- *File_name* is the name of the file in which the Timing Analysis report is saved.

Abbreviation

Abbreviate the AnalyzeTimingConstraints command syntax as follows.

`atc [s` *file_name*.**`twr]`**

Example

The following is an example of the AnalyzeTimingConstraints command.

```
analyzetimingconstraints save nikko.twr
```

ControlPathTracing

The ControlPathTracing command controls path tracing through RAMs, tristate buffers, input and output pins, components, and Set/Reset logic. These paths may be irrelevant to your analysis.

Note: This command only applies to FPGAs; it does not function if a CPLD design is open. (CPLD path timing analysis ignores paths through Set/Reset logic and breaks paths at bidirectional I/O pins.)

This command is equivalent to the **`Path Filters`** → **`Common Filters`** → **`Control Path Tracing`** menu command.

Syntax

The syntax of the ControlPathTracing command is the following.

ControlPathTracing {Enable|Disable} {reg_sr_q|lat_d_q|ram_d_o|ram_we_o|tbuf_t_o|tbuf_i_o|io_pad_i|io_t_pad|io_o_i|io_o_pad}
component_name component_name...

- **reg_sr_q** enables path tracing through CLB flip-flop asynchronous Set or Reset outputs. By default, this path is disabled; the Timing Analyzer does not analyze these paths.
- **lat_d_q** enables path tracing from the latch D input to the Q output. By default, this path is disabled; the Timing Analyzer does not analyze these paths.
- **ram_d_o** enables path tracing through the data inputs of a CLB RAM. By default, this path is disabled; the Timing Analyzer does not analyze these paths.
- **ram_we_o** disables path tracing through the write-enable input of a CLB RAM. By default, this path is enabled; the Timing Analyzer analyzes these paths.
- **tbuf_t_o** disables path tracing of paths that pass through a T pin to the O pin. By default, this path is enabled; the Timing Analyzer analyzes these paths.
- **tbuf_i_o** disables path tracing from the input pin to the output pin of a TBUF. By default, this path tracing is enabled; the Timing Analyzer analyzes these paths.
- **io_pad_i** disables path tracing from the pad pin to the input pin of an IOB. By default, this path tracing is enabled; the Timing Analyzer analyzes these paths.
- **io_t_pad** disables path tracing from the tristate control pin of an IOB to the pad, or if the architecture supports it, the path through the data input to output of the tri-state enable latch. By default, this path tracing is enabled; the Timing Analyzer analyzes these paths.
- **io_o_i** disables path tracing of paths from the IOB O pin to the I pin. By default, this path is enabled but is disabled for tristate IOBs; the Timing Analyzer analyzes these paths.
- **io_o_pad** disables path tracing from the output pin of an IOB to the pad pin. By default, this path tracing is enabled; the Timing Analyzer analyzes these paths.

- *Component_name* is the name(s) of the CLBs, IOBs, or TBUFs that the path goes through.

Abbreviation

Abbreviate the ControlPathTracing command syntax as follows.

cpt {Enable|Disable}
{reg_sr_q|lat_d_q|ram_d_o|ram_we_o|tbuf_t_o|tbuf_i_o|io_pad_i|io_t_pad|io_o_i|io_o_pad}
component_name component_name...

Example

Following is an example of the ControlPathTracing command.

```
controlpathtracing ram_we_o CLB_R4C4
```

DefineEndPoints

The DefineEndPoints command selects the starting and ending points of the paths that you want to analyze.

This command is equivalent to the **Path Filters** → **Custom Filters** → **Select Sources** and the **Path Filters** → **Custom Filters** → **Select Destinations** menu commands.

FPGA starting and ending points are: flip-flops, pads, nets, pins, CLBs, RAMs, latches, clocks, or timegroups. CPLD starting and ending points are: flip-flops, pads, nets, macrocells, or clocks.

Syntax

The syntax of the DefineEndPoints command is the following.

DefineEndPoints {FromAll|ToAll}
DefineEndPoints {FromPad|ToPad} *pad_name*
DefineEndPoints {FromCLB|ToCLB} *CLB_name*
DefineEndPoints {FromNet|ToNet} *net_name*
DefineEndPoints {FromPin|ToPin} *pin_name*
DefineEndPoints {FromFF|ToFF} *flip-flop_name*
DefineEndPoints {FromEitherEdge|ToEitherEdge} *clock_name*
DefineEndPoints {FromRising|ToRising} *clock_name*
DefineEndPoints {FromMacrocell|ToMacrocell}

macrocell_name
DefineEndPoints {FromFalling|ToFalling} *clock_name*
DefineEndPoints {FromRAM|ToRAM} *RAM_name*
DefineEndPoints {FromLatch|ToLatch} *latch_name*
DefineEndPoints {FromTimeGroups|ToTimeGroups} *timegroup_name*

- **FromAll** selects paths that begin at any path source.
- **ToAll** selects paths that end at any path destination.
- **FromPad** selects pads as starting points for the path to be analyzed.
- **ToPad** selects pads as ending points for the path to be analyzed.
- **FromCLB** selects CLBs as starting points for the path to be analyzed.
- **ToCLB** selects CLBs as ending points for the path to be analyzed.
- **FromNet** selects nets as starting points for the path to be analyzed.
- **ToNet** selects nets as ending points for the path to be analyzed.
- **FromPin** selects pins as starting points for the path to be analyzed.
- **ToPin** selects pins as the ending points for the path to be analyzed.
- **FromFF** selects flip-flops as starting points for the path to be analyzed.
- **ToFF** selects flip-flops as ending points for the path to be analyzed.
- **FromEitherEdge** selects either clock edge as starting points for the path to be analyzed
- **ToEitherEdge** selects either clock edge as ending points for the path to be analyzed.
- **FromRising** selects rising clock edges as starting points for the path to be analyzed.
- **ToRising** selects rising clock edges as ending points for the path to be analyzed.

- **FromMacrocell** selects macrocells as starting points for the path to be analyzed.
- **ToMacrocell** selects macrocells as ending points for the path to be analyzed.
- **FromFalling** selects falling clock edges as starting points for the path to be analyzed.
- **ToFalling** selects falling clock edges as ending points for the path to be analyzed.
- **FromRAM** selects RAMs as starting points for the path to be analyzed.
- **ToRAM** selects RAMs as ending points for the path to be analyzed.
- **FromLatch** selects latches as starting points for the path to be analyzed.
- **ToLatch** selects latches as ending points for the path to be analyzed.
- **FromTimeGroups** selects timegroups as starting points for the path to be analyzed.
- **ToTimeGroups** selects timegroups as ending points for the path to be analyzed.
- *Pad_name* is the name of the PAD that is the starting or ending point of the path to be analyzed.
- *CLB_name* is the name of the CLB that is the starting or ending point of the path to be analyzed.
- *Net_name* is the name of the net that is the starting or ending point of the path to be analyzed.
- *Pin_name* is the name of the pin that is the starting or ending point of the path to be analyzed.
- *Flip-Flop_name* is the name of the flip-flop that is the starting or ending point of the path to be analyzed.
- *Clock_name* is the name of the clock that is the starting or ending point of the path to be analyzed.
- *Macrocell_name* is the name of the macrocell that is the starting or ending point of the path to be analyzed.

- *RAM_name* is the name of the RAM that is the starting or ending point of the path to be analyzed.
- *Latch_name* is the name of the latch that is the starting or ending point of the path to be analyzed.
- *Timegroup_name* is the name of the timegroup that is the starting or ending point of the path to be analyzed.

The defaults are FromAll and ToAll.

In the DefineEndPoints command syntax, you can enter * for *pad_name*, *CLB_name*, *net_name*, *pin_name*, *flip-flop_name*, *clock_name*, *macrocell_name*, or *RAM_name* to specify all the elements of that type.

Abbreviation

Abbreviate the DefineEndPoints command syntax as follows.

dep {fall|tall}
dep {fpad|tpad} *pad_name*
dep {fclb|tclb} *CLB_name*
dep {fnet|tnet} *net_name*
dep {fpin|tpin} *pin_name*
dep {fff|tff} *flip-flop_name*
dep {fee|tee} *clock_name*
dep {fris|tris} *clock_name*
dep {fmc|tmc} *macrocell_name*
dep {ffal|tfal} *clock_name*
dep {fram|tram} *RAM_name*
dep {fl|tl} *latch_name*
dep {ftg|ttg} *timegroup_name*

Example

Following are examples of the DefineEndPoints command.

```
defineendpoints fromff CNT3Q0 CNT3Q1
defineendpoints topad P80 P68
```

DelayGreaterThan

The DelayGreaterThan command specifies a minimum delay in nanoseconds. This command only supports analysis of CPLD designs. The Timing Analyzer reports only those paths that have a

delay greater than or equal to the specified value. By default, *delay_value* is 0, which reports all paths regardless of their delay.

This command is equivalent to the Report Delays Greater Than field in the Report Options dialog box, which is activated by the **Options** → **Report Options** menu command.

Syntax

The syntax of the DelayGreaterThan command is the following.

DelayGreaterThan *delay_value*

Delay_value is the minimum delay in nanoseconds.

Abbreviation

Abbreviate the DelayGreaterThan command syntax as follows.

dg *delay_value*

Example

Following is an example of the DelayGreaterThan command.

```
delaygreaterthan 30
```

DelayLessThan

The DelayLessThan command specifies a maximum delay in nanoseconds. This command only supports analysis of CPLD designs. The Timing Analyzer reports only those paths that have a delay less than or equal to the specified value. By default, the Timing Analyzer reports all paths regardless of their delay.

This command is equivalent to the Report Delays Less Than option in the Report Options dialog box, which is activated by the **Options** → **Report Options** menu command.

Syntax

The syntax of the DelayLessThan command is the following.

DelayLessThan *delay_value*

Delay_value is the maximum delay in nanoseconds. It is optional. If a value is not specified, the limit is turned Off.

Abbreviation

Abbreviate the DelayLessThan command syntax as follows.

dl *delay_value*

Example

Following is an example of the DelayLessThan command.

```
delaylessthan 30
```

DoHoldRaceCheck

The DoHoldRaceCheck command checks for race conditions and does a rigorous clock skew analysis on the design.

This command is equivalent to the **Options** → **Do Hold/Race Check** menu command.

Syntax

The syntax of the DoHoldRaceCheck command is the following.

DoHoldRaceCheck {true|false}

- **True** enables race checking and full skew analysis.
- **False** disables race checking and full skew analysis.

Abbreviation

Abbreviate the DoHoldRaceCheck command syntax as follows.

dhrc {t|f}

Example

Following is an example of the DoHoldRaceCheck command.

```
doholdracecheck true
```

DropTimingConstraint

The DropTimingConstraint command prevents the Timing Analyzer from analyzing the specified timing constraints.

This command is equivalent to the **Path Filters** → **Timing Constraint Filters** → **Disable Timing Constraints** menu command.

Syntax

The syntax of the DropTimingConstraint command is the following.

DropTimingConstraint [*time_constraint1 time_constraint2...*]

Time_constraint1, *time_constraint2*, and so forth are the timing constraints to be ignored. Each can be either the name or the full text of the timing constraint in single quotes.

Abbreviation

Abbreviate the DropTimingConstraint command syntax as follows.

dtc [*time_constraint1 time_constraint2...***]**

Example

Following is an example of the DropTimingConstraint command.

```
droptimingconstraint TS08 TS09 TS10
```

ExcludeNets

The ExcludeNets command excludes paths that contain specified nets from analysis. If a net is selected, paths through that net are not analyzed. However, if no nets are selected, which is the default, all nets, except those you exclude with other path filtering commands, are analyzed.

This command is equivalent to the **Path Filters** → **Common Filters** → **Exclude Paths with Nets** menu command.

Syntax

The syntax of the ExcludeNets command is the following.

ExcludeNets [*net_name1 net_name2...***]**

Net_name1, *net_name2*, and so forth are the names of the nets to be excluded.

Abbreviation

Abbreviate the ExcludeNets command syntax as follows.

exnet [*net_name1 net_name2...***]**

Example

Following is an example of the ExcludeNets command.

```
excludenets $1N95 CNT5 CNT6 CNT7 EXT_CLK1 EXT_CLK2
```

Exit

The Exit command exits the Timing Analyzer.

This command is equivalent to the **File** → **Exit** menu command.

Syntax

The syntax of the Exit command is the following.

exit

Abbreviation

Abbreviate the Exit command syntax as follows.

e

Example

Following is an example of the Exit command.

```
exit
```

IncludeNets

The IncludeNets command limits analysis to paths that contain specified nets. If a net is not specified, paths through that net are not analyzed. However, if no nets are selected, which is the default, all

nets, except those you exclude with other path filtering commands, are analyzed. This command is equivalent to the **Path Filters** → **Common Filters** → **Include Paths with Nets** menu command.

Syntax

The syntax of the IncludeNets command is the following.

IncludeNets [*net_name1 net_name2...***]**

Net_name1, *net_name2*, and so forth are the selected nets.

Abbreviation

Abbreviate the IncludeNets command syntax as follows.

incnet [*net_name1 net_name2...***]**

Example

Following is an example of the IncludeNets command.

```
includenets in2_1 in2_2
```

IncludeNoTimingConstraint

The IncludeNoTimingConstraint command includes paths without timing constraints, in addition to paths with timing constraints, in analysis.

There is no direct equivalent menu command for IncludeNoTiming-Constraint. The following three menu commands are associated with IncludeNoTimingConstraint:

- Report Paths in Timing Constraints (Analyze Menu)
- Report Paths Failing Timing Constraints (Analyze Menu)
- Report Paths Not Covered by Timing Constraints (Analyze Menu)

Syntax

The syntax of the IncludeNoTimingConstraint command is the following.

IncludeNoTimingConstraint {true|false}

- **True** reports paths with no timing concurrents (as well the paths with timing constraints). It is the default setting when opening a CPLD design.
- **False** does not report paths with no timing constraints. This argument is the default when opening an FPGA design.

Abbreviation

Abbreviate the IncludeNoTimingConstraint command syntax as follows.

intc {t|f}

Example

Following is an example of the IncludeNoTimingConstraint command.

```
includenotimingconstraint true
```

MaxPathsPerTimingConstraint

The MaxPathsPerTimingConstraint command limits the number of paths reported per timing constraint. For FPGAs, the default is one path per timing constraint. For CPLDs, the default is unlimited. This option can be useful, because it limits the size of report files. By default, the Timing Analyzer reports all paths that satisfy the other settings.

The command is equivalent to the Maximum Paths Per Timing Constraint field in the Report Options dialog box, which is activated by the **Options** → **Report Options** menu command.

Syntax

The syntax of the MaxPathsPerTimingConstraint command is the following.

MaxPathsPerTimingConstraint *number*

Number is the maximum number of paths per timing constraint that the Timing Analyzer reports. It is optional. No *number* turns the limit Off. If *number* is 0, the Timing Analyzer generates a summary report.

Abbreviation

Abbreviate the MaxPathsPerTimingConstraint command syntax as follows.

`mpptc` *number*

Example

Following is an example of the MaxPathsPerTimingConstraint command.

```
maxpathspertimingconstraint 20
```

OmitUserConstraints

The OmitUserConstraints command enables or disables timing constraints in the "USER" section of the Physical Constraints File (PCF). The order of the timing constraints in the PCF file is reflected by the Timing Analyzer. It only supports analysis of FPGA designs.

This command is equivalent to the Omit PCF Entered Constraints radio button in the Disable Timing Constraints dialog box, which is activated by the **`Path Filters`** → **`Timing Constraint Filters`** → **`Disable Timing Constraints`** menu command.

Syntax

The syntax for the OmitUserConstraints command is the following.

`OmitUserConstraints {true|false}`

- **`True`** disables the "USER" timing constraints in the PCF file.
- **`False`** enables the "USER" timing constraints in the PCF file.

Abbreviation

Abbreviate the OmitUserConstraints command syntax as follows.

`ouc {t|f}`

Example

Following is an example the OmitUserConstraints command.

```
omituserconstraints false
```

OnlyLongestPaths

The OnlyLongestPaths command restricts the Timing Analyzer to reporting only the path with the longest delay, if there is more than one path between two end points. It only supports analysis of CPLD designs. By default, the Timing Analyzer reports all paths.

This command is equivalent to the Report Only Longest Paths Between Points check box in the Report Options dialog box, which is activated by the **Options** → **Report Options** menu command.

Syntax

The syntax of the OnlyLongestPaths command is the following.

```
OnlyLongestPaths {true|false}
```

- **True** includes only the longest paths; it is the default when you generate the Advanced Design Analysis report.
- **False** includes all paths; it is the default when you generate any report except the Advanced Design Analysis report.

Abbreviation

Abbreviate the OnlyLongestPaths command syntax as follows.

```
olp {t|f}
```

Example

Following is an example of the OnlyLongestPaths command.

```
onlylongestpaths false
```

OpenDesign

The OpenDesign command opens a mapped NCD (FPGA) or a completely placed and routed VM6 (CPLD) design file for timing analysis. The mapped FPGA design can be partially or completely placed, routed, or both.

This command is equivalent to the **File** → **Open Design** menu command.

Syntax

The syntax of the OpenDesign command is the following.

OpenDesign {*design_name*.**ncd|***design_name*.**vm6}**

Design_name is the NCD or VM6 file name, including the path of the directory in which it is located.

This command does not open a report (TWR) file.

Abbreviation

You can abbreviate the OpenDesign command syntax as follows.

od *design_name*.**ncd**

Example

Following is an example of the OpenDesign command.

```
opendesign checkers.ncd
```

OpenPCF

The OpenPCF command opens an existing physical constraints file (PCF). This command applies only to FPGAs. The order of the constraints in the PCF file is reflected by the Timing Analyzer.

Loading a new physical constraints file causes the Prorating Options to be reset to the values specified in the last PCF file you loaded. If the PCF file does not contain Prorating Options preferences, the worst case values are used.

This command is equivalent to the **File** → **Open Physical Constraints** menu command.

Syntax

The syntax of the OpenPCF command is the following.

OpenPCF *file_name*.**pcf**

File_name is the name of the PCF file.

Abbreviation

You can abbreviate the OpenPCF command syntax as follows.

op *file_name*.**pcf**

Example

Following is an example of the OpenPCF command.

```
openpcf checkoffset.pcf
```

ProratingOptions

The ProratingOptions command controls temperature and voltage prorating.

This command is equivalent to the **Options** → **Prorating Options** menu command.

Syntax

The syntax of the ProratingOptions command is the following.

ProratingOptions [**Temp** [*degrees_celsius*]] [**Volts** [*voltage*]]

degrees_celsius is the temperature prorating.

voltage is the voltage prorating.

If no value is specified for the temperature or voltage, the prorating is set to the worst case value.

Abbreviation

You can abbreviate the ProratingOptions command syntax as follows.

po [**T** [*degrees_celsius*]] [**V** [*voltage*]]

Example

Following are examples of the ProratingOptions command.

```
po
po t
po t 80 v 5.2
```

Query

The Query command reports timing information about particular nets and members of time groups. This command applies only to FPGAs. See the "Query (Analyze Menu)" section of the "Menu Commands" chapter for the specific information that this command reports.

This command is equivalent to the **Options** → **Query** menu command.

Syntax

The syntax of the Query command is the following.

query {Net|TimeGroup} *element_name*

- **Net** reports information about nets.
- **TimeGroup** reports information about timing groups.
- *Element_name* can be the following:
  - Net name when you specify the net option.
  - Timing group name when you specify the TimeGroup option.

Abbreviation

Abbreviate the Query command syntax as follows.

qy {n|tg} *element_name*

Example

Following are examples of the Query command.

```
query net ram_d_o
query timegroup 05
```

Report

The Report command determines the format of the report output.

This command is equivalent to the Wide Report option in the Report Options dialog box, which is activated by the **Options** → **Report Options** menu command.

Syntax

The syntax of the Report command is the following.

```
report {wide|normal}
```

- **Wide** sets a format of 132 characters per line, which prevents long component and net names from being truncated.
- **Normal**, the default, displays a detailed list of path delays. The width is 80 characters per line. Because normal is the default, it does not appear as an option for the Report Options menu command.

Abbreviation

You can abbreviate the Report command syntax as follows.

```
r {w|n}
```

Example

Following is an example of the Report command.

```
report wide
```

ResetAllPathFilters

The ResetAllPathFilters command resets the path filtering commands to the system defaults. See the "Settings (View Menu)" section of the "Menu Commands" chapter for a listing of these defaults.

This command is equivalent to the **Path Filters** → **Reset All Path Filters** menu command.

Syntax

The syntax of the ResetAllPathFilters command is the following.

```
ResetAllPathFilters
```

Abbreviation

Abbreviate the ResetAllPathFilters command syntax as follows.

`rapf`

Example

Following is an example of the ResetAllPathFilters command.

```
resetallpathfilters
```

RunMacro

The RunMacro command runs an existing macro.

This command is equivalent to the **`File`** → **`Run Macro`** menu command.

Syntax

The syntax of the RunMacro command is the following.

`RunMacro` *file_name*.**`xtm`**

File_name is the name of the macro file.

Abbreviation

You can abbreviate the RunMacro command syntax as follows.

`runm` *file_name*.**`xtm`**

Example

Following is an example of the RunMacro command.

```
runmacro deb.xtm
```

SelectFailingTimingConstraint

The SelectFailingTimingConstraint command reports only the paths that do not meet timing constraints.

There is no direct equivalent menu command for SelectFailingTimingConstraint. The following three menu commands are associated with SelectFailingTimingConstraint.

- Report Paths in Timing Constraints (Analyze Menu)
- Report Paths Failing Timing Constraints (Analyze Menu)
- Report Paths Not Covered by Timing Constraints (Analyze Menu)

Syntax

The syntax of the SelectFailingTimingConstraint command is the following.

```
SelectFailingTimingConstraint {true|false}
```

- **True** includes only the paths that do not meet your timing constraints.
- **False** includes all paths. This setting is the default.

Abbreviation

Abbreviate the SelectFailingTimingConstraint command syntax as follows.

```
sftc {t|f}
```

Example

Following is an example of the SelectFailingTimingConstraint command.

```
selectfailingtimingconstraint true
```

SetForce

When you run a macro, the commands in the macro file can generate informational, confirmational, and error messages. When the SetForce command is set to On, the Timing Analyzer suppresses the warning and confirmational messages that appear in dialog boxes. Only error messages continue to appear. Macros continue to run until an error is produced. You cannot suppress messages while executing menu commands. SetForce Off restores the appearance of all three types of messages to the Console window.

This command does not have an equivalent menu command.

Syntax

The syntax of the SetForce command is the following.

```
SetForce {on|off}
```

On suppresses the informational and confirmational messages, and **Off** restores them. **On** is the default.

Abbreviation

You can abbreviate the SetForce command syntax as follows.

```
sf {on|off}
```

Example

Following is an example of the SetForce command.

```
setforce on
```

ShowClockNets

The ShowClockNets command creates the Clocks report, which lists the names of all clocks in the design.

This command is equivalent to the **View** → **Clocks** menu command.

Syntax

The syntax of the ShowClockNets command is the following.

ShowClockNets [save *file_name***]**

The report appears in a pop-up window.

- **Save** indicates that you can optionally save the Show Clocks report in a file.
- *File_name* is the name of the saved file. You can add a .twr extension to the *file_name* to list it under Timing Analysis Reports (*.twr) under List Files of Type in File menu command dialog boxes.

Abbreviation

You can abbreviate the ShowClockNets command syntax as follows.

scn [s *file_name*]

Example

Following is an example of the ShowClockNets command.

```
showclocknets save nikkoclocks
```

ShowSettings

The ShowSettings command lists all the current settings for Timing Analyzer options. You can save the contents of the window as a macro or a report.

This command is equivalent to the **View** → **Settings** menu command.

Syntax

The syntax of the ShowSettings command is the following.

ShowSettings [save *file_name*]

The report appears in a pop-up window.

- **Save** indicates that you can optionally save the Show Settings report in a file.
- *File_name* is the name of the saved file. You can add a .xtm extension to the *file_name* to save the settings as a macro to return the system to the same state as when the settings were saved. See the "Saving a New Macro" section and the "Running a Macro" section of the "Using the Timing Analyzer" chapter for more information.

  Optionally, you can add a .twr extension to the *file_name* to save the settings as a report. TWR files are listed as Timing Analysis Reports (*.twr) under List Files of Type in File menu command dialog boxes. See the "Saving a Report" section of the "Using the Timing Analyzer" chapter for the procedure to save a report.

Abbreviation

You can abbreviate the ShowSettings command syntax as follows.

ss [s *file_name*.**xtm]**

Example

Following is an example of the ShowSettings command.

```
showsettings save triad2.xtm
```

SortOn

The SortOn command specifies how paths are sorted when they are reported. It only supports analysis of CPLD designs.

This command is equivalent to the Sort On field in the Report Options dialog box, which is activated by the **Options** → **Report Options** menu command.

Syntax

The syntax of the SortOn command is the following.

SortOn {Ascend|Descend|SourceNet|DestNet|SourceClkNet|DestClkNet}

- **Ascend** lists paths in order from shortest to longest delays.
- **Descend**, the default, lists paths in order from longest to shortest delays.
- **SourceNet** sorts path delays by the source net name, which is useful when trying to determine the worst-case delay from a given net.
- **DestNet** sorts path delays by the destination net name, which can help determine the worst-case path to each net.
- **SourceClkNet** sorts path delays by the clock name that sources the first element in a path, which separates delay information for two or more clock nets in a design.
- **DestClkNet** sorts path delays by the clock name that sources the last element in a path.

Abbreviation

You can abbreviate the SortOn command syntax as follows.

sort {a|d|sn|dn|scn|dcn}

Example

Following is an example of the SortOn command.

```
sorton sourcenet
```

Speed

The Speed command sets the speed grade during analysis. Changing the speed grade helps you determine if you need to target a faster device to meet your timing requirements, or if using a slower speed grade still meets timing constraints. The speed grade is set in the design file, NCD for FPGAs or VM6 for CPLDs. Using this command does not affect the speed grade set in the design file.

Changing the speed grade may affect the worst case and range of values available in the Prorating Options dialog box.

This command is equivalent to the **Options** → **Speed Grade** menu command.

Syntax

The syntax of the Speed command is the following.

speed *speed_grade*

Speed_grade can be any of the speed grades available for the architecture used. You can obtain this information from the Design Manager or the Timing Analyzer's graphical interface.

Abbreviation

You can abbreviate the Speed command syntax as follows.

sp *speed_grade*

Example

Following is an example of the Speed command.

```
speed –3
```

Appendix A

Glossary

This appendix defines the key terms and concepts that you should understand to use the Timing Analyzer effectively. The terms are listed in alphabetical order.

BEL

A Basic ELement. Basic Elements are the building blocks that make up a CLB, IOB, BLOCK RAM, or TBUF—function generators, flip-flops, carry logic, and RAMs.

CLB

The CLB (Configurable Logic Block) constitutes the basic FPGA cell. The FPGA is an array of CLBs organized in columns and rows on the silicon die. CLBs are used to implement macros and other designed functions. They provide the physical support for an implemented and downloaded design. They have inputs on each side, and this versatility makes them flexible for the mapping and partitioning of logic. See *The Programmable Logic Data Book* for each device's CLB.

clock input path

A clock input path is a logic transition, which when applied to a clock pin on a synchronous element, captures data. It starts at either an input or an output of the chip, but can also start at other sequential elements. A clock input path propagates through any number of levels of combinatorial logic and ends at any clock pin on a flip-flip, latch, or synchronous RAM. These paths do not propagate through synchronous elements. The clock input path time is the maximum time required for the signal to arrive at the clock input of the synchronous element.

clock skew

The difference between the time a clock signal arrives at the source flip-flop in a path and the time it arrives at the destination flip-flop.

clock-to-pad path

A path starting at the Q output of a flip-flop or latch and ending at an output of the chip. It includes the clock-to-Q delay of the flip-flop and the path delay from that flip-flop to the chip output. The clock-to-pad path time is the maximum time required for the data to leave the source flip-flop, travel through logic and routing, and arrive at the output.

clock-to-setup path

A path starting at the Q output of a flip-flop or latch and ending at an input to another flip-flop, latch, or RAM, where that pin has a setup requirement before a clocking signal. It includes the clock-to-Q delay of the source flip-flop, the path delay from that flip-flop to the destination flip-flop, and the setup requirement of the destination flip-flop. The clock-to-setup path time is the maximum time required for the data to propagate through the source flip-flop, travel through the logic and routing, and arrive at the destination before the next clock edge occurs.

component

A logical configuration that will, at some point, go into a physical site. Examples of components are CLBs, IOBs, tristate buffers, pull-up resistors, and oscillators.

console log

Record of the commands that you invoked during a session.

critical path

The path within a design that dictates the fastest time at which an entire design can run. This path runs from the source to a sink node such that if any activity on the path is delayed by an amount *t*, then the entire circuit function is delayed by time *t*.

destination

A sink node or stopping point for a timing analysis path, often the data input of a synchronous element or a pad.

endpoints

A node which acts as either the driver to begin a path or a load to end a path.

filter

A set of limitations or options applied to the timing analysis to more specifically target important items of interest.

fitting

The process of putting logic from your design into physical macrocell locations in a CPLD. Routing is performed automatically, and because of the interconnect architecture, all designs are routable.

high-density function block (HDFB)

A group of macrocells in a CPLD that can efficiently perform complex logic such as arithmetic operations.

hold time

The time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

IOB (input/output block)

A collection or grouping of basic elements that implement the input and output functions of FPGA and CPLD devices.

macro

A *physical macro* is a logical function which has been mapped into the components of a specific device family. Physical macros are stored in files with the extension .nmc. In addition to components and nets, the

file can also contain placement, routing, or both kinds of information. A macro can be unplaced, partially placed, or fully placed. It can also be unrouted, partially routed, or fully routed. See the "Working with Physical Macros" chapter of the *FPGA Editor Guide* for information about physical macros.

Specific to the Timing Analyzer, a macro is an ASCII file containing a sequence of Timing Analyzer keyboard commands that are executed in script form.

main window

The background against which windows are displayed.

menu bar

The area located at the top of the main window that provides access to the menus.

net

A logical connection between two or more symbol instance pins. After routing, the abstract concept of a net is transformed to a physical connection called a wire.

offset

Defines the timing relationship between an external clock and its associated data-in or data-out pin.

pad

The physical bonding pad on an Integrated Circuit. All signals on a chip must enter and leave by way of a pad. Pads are connected to package pins in order for signals to enter or leave an Integrated Circuit package.

pad-to-pad path

A path starting at an input of the chip and ending at an output of the chip. The pad-to-pad path time is the maximum time required for the

data to enter the chip, travel through logic and routing, and leave the chip. It is not controlled or affected by any clock signal.

pad-to-setup path

A path starting at an input of the chip and ending at an input to a flip-flop, latch, or RAM—wherever there is a setup time against a control signal. The pad-to-setup path time is the maximum time required for the data to enter the chip, travel through logic and routing, and arrive at the input before the clock or control signal arrives.

path

An ordered set of elements identifying a logic flow pathway through a circuit. A path may consist of a single net or a grouping of related nets and components. There can be multiple paths (consisting of nets and components) between the two pins. When a component is selected as part of a path, both the input pin to the component and the output pin are included in the path. A path stops when it reaches the data input of a synchronous element (flip-flop) or pad. A path usually starts at the output of a synchronous element or pad.

Paths can be defined by using timing specifications. See the “Using Timing Constraints” chapter of the *Development System Reference Guide*. In the “Path Example” figure, there are three paths between Pin A and Pin B. One path travels from Pin A through LB2 and through LB6 to Pin B, another travels from Pin A through LB3 and through LB6 to Pin B, and another travels from Pin A through LB4, LB5, and LB6 to Pin B.

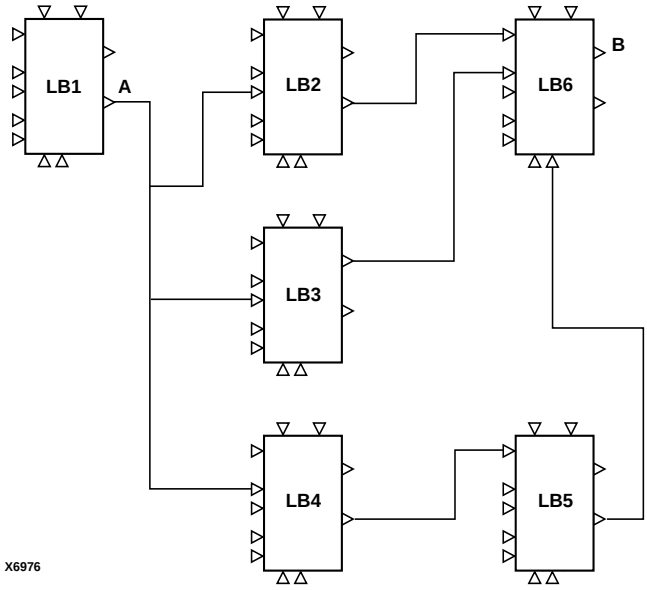


Figure A-1 Path Example

period

The time specified for a clock signal to transition from a state back to the same state. Also, a requirement placed on the clock signal that the place and route software is expected to meet. The period of the clock is affected by the amount of time it takes the output of one sequential element to pass to the next sequential element in a path.

pin

A symbol pin or package pin. A package pin is a physical connector on an Integrated Circuit package that carries signals into and out of an Integrated Circuit.

A symbol pin, also referred to as an instance pin, is the connection point of an instance to a net.

primitive

A logic element that directly corresponds, or maps, to a basic element.

schematic

A hierarchical diagram representing a design in terms of user and library components.

SDF

Standard Delay Format, which is an industry-standard file format for specifying timing information. It is often used for simulation.

sequential element

A flip-flop, synchronous RAM, or Latch.

setup time

The time relative to a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

slack

The difference between the constraint and the analyzed value, with negative slack indicating an error condition.

source

An output pin that drives a path. Sources are input pads and the outputs of synchronous elements.

static timing analysis

A point-to-point delay analysis of a design network with respect to a given set of constraints. It does not include insertion of stimulus vectors.

status bar

An area located at the bottom of an application window that provides information about the commands that you are about to select or that are being processed.

time group

A collection of design elements, including nets, BELs, components, and so forth that can be used to constrain many objects in the same way.

timing constraints

A series of constraints applied to a given set of paths or nets that dictate the desired performance of a design. Constraints may be period, frequency, net skew, maximum delay between end points, or maximum net delay.

toolbar

A group of buttons with graphic icons located under the menu bar in the application window that provide button access to frequently used commands in pull-down menus.

TRACE

The Timing Reporter And Circuit Evaluator provides static timing analysis of a design based on input timing constraints. Its two major functions are timing verification and reporting.

universal interconnect matrix (UIM)

The routing matrix for CPLD devices. This fully populated switching matrix allows any output to be routed to any input, guaranteeing 100 percent routability of all designs. The UIM can also function as a very wide AND gate, which can allow more logic to be placed in macrocells.

verification

In timing, the process of comparing the desired performance of a design using constraints against the expected performance, based on software models of the device speed and routing delays.

VHDL

An acronym for VHSIC Hardware Description Language (VHSIC is an acronym for Very High-Speed Integrated Circuits) or HDL, which can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level.